Genesys Logic, Inc.

GL3321G

USB 3.0 to SATA 6Gb/s
Bridge Controller

Product Overview

Copyright

Ownership and Title

Disclaimer

Genesys Logic, Inc.

12F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,

New Taipei City, Taiwan

Tel : (886-2) 8913-1888

Fax : (886-2) 6629-6168

http://www.genesyslogic.com

GENERAL DESCRIPTION

GL3321G is a high performance USB3.0 to SATA 6Gb/s storage controller for personal storage (external HDD/SSD enclosure), ODD player, media player, and set-top-box applications. It integrates Genesys Logic owned design USB3.0/2.0 PHY and SATA PHY which provides more design flexibility and quality. From system point of view, GL3321G can meet EU Eup regulation on standby power consumption (0.5W) and it also passes Microsoft WHQL1.6 verification program, which can reduce time-to-market efforts for system manufacturers.GL3321G also integrates the voltage regulators to provide minimal active components on RBOM.
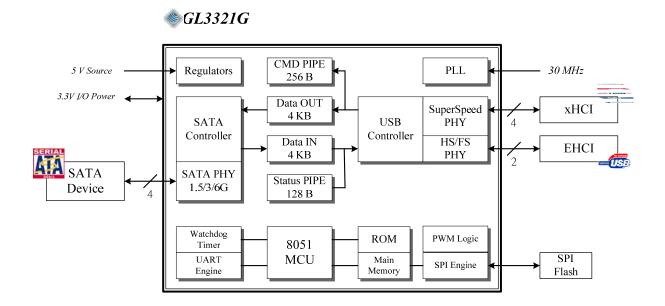
FEATURES

- USB specification compliance
    - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
    - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
    - Comply with USB Mass Storage Class Specification rev. 1.0
    - Support USB Mass Storage Class Bulk-Only Transport (BOT)
    - Support USB Attached SCSI (UAS) and USB Attached SCSI Protocol (UASP)
    - Support 1 device address and up to 6 endpoints: Control (0) / Bulk Data Write Out (1) / Bulk Data Read In (2) / Interrupt In (3) / CMD Out (4) / Status In (5)
    - Support 5 Gbps SuperSpeed, 480 Mbps high-speed, and 12 Mbps full-speed transfer rates
- SATA specification features
    - Comply with Serial ATA Revision 3.0 Specification Gold Revision
    - Support SATA power saving, including partial and slumber modes
    - Support SATA Hot Plug
    - Support Native Command Queuing up to 32 commands
    - Support SATA host/device initiated power management
    - Support SATA BIST host/device initiated eye pattern test
    - Support 6.0 Gbps, 3.0 Gbps and 1.5 Gbps transfer rates
    - Support SATA Device Sleep function (DevSlp)
- Embedded 8051 micro-controller
    - Embedded 64 Kbytes Mask ROM
    - Embedded 16 Kbytes Code SRAM for Cache and 2 Kbytes Data SRAM
- Embedded internal regulators
    - 5 V to 3.3V linear drop-out regulator for whole chip power supply
    - Inductor-type DC-DC for core power, input range from 2.97 V to 3.63 V
- Single clock source, supporting 30 MHz
- Available in 48-pin QFN (6 x 6 mm^2)
- Operating System support
    - Windows 8/Windows 7 32&64/Vista32&64/XP/2000/Me/98/98SE, Mac OS 9.X/10.X, Linux Kernel 2.4.X/2.6.X
- Other Features
    - Support write Protect Function, Password Security (virtual CD ROM), Backup Management
    - Support Trim Command for SSD
    - Support Win8 Windows To Go
    - Support ODD (BD, DVD, CD)
    - Spread Spectrum Clocking (SSC) for EMI reduction
    - On-chip watchdog timer for automatic error recovery
    - SPI interface for firmware update.
    - PWM interfaces for fan control and LED control (2 GPIOs).
    - UART interface for debugging

BLOCK DIAGRAM

GL3321G

GL3321G Block Diagram