NEC

MOS INTEGRATED CIRCUIT

μPD23C256112A

NAND INTERFACE
256M-BIT MASK-PROGRAMMABLE ROM

Description

The μPD23C256112A is a 256 Mbit NAND interface programmable mask read-only memory that operates with a single power supply. The memory organization consists of (512 + 16 (Redundancy)) bytes x 32 pages x 2,048 blocks. The μPD23C256112A is a serial type mask ROM in which addresses and commands are input and data output serially via the I/O pins.

The μPD23C256112A is packed in 48-pin PLASTIC TSOP(I).

Features

- Word organization

  (33,554,432 + 1,048,576[Note]) words by 8 bits

- Page size

  (512 + 16[Note]) by 8 bits

- Block size

  (16,384 + 512[Note]) by 8 bits

Note Underlined parts are redundancy.

Caution Redundancy is not programmable parts and is fixed to all FFH.

- Operation mode

  READ mode (1), READ mode (2), READ mode (3), RESET, STATUS READ, ID READ

- Operating supply voltage : V_{CC} = 3.3 ± 0.3 V

- Access Time

  Memory cell array to starting address : 7 μs (MAX.)

  Read cycle time : 50 ns (MIN.)

  /RE access time : 35 ns (MAX.)

- Operating supply current

  During read : 30 mA (MAX.) (50 ns cycle operation)

  During standby (CMOS) : 100 μA (MAX.)

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

	Part Number	Package
	μPD23C256112AGY-xxx-MJH	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
	μPD23C256112AGY-xxx-MKH	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)
<R>	μPD23C256112AGY-xxx-MJH-A	48-pin PLASTIC TSOP(I) (12x18) (Normal bent)
<R>	μPD23C256112AGY-xxx-MKH-A	48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

Remarks 1. xxx : ROM code suffix No.

<R> **2.** Products with -A at the end of the part number are lead-free products.

Pin Configurations

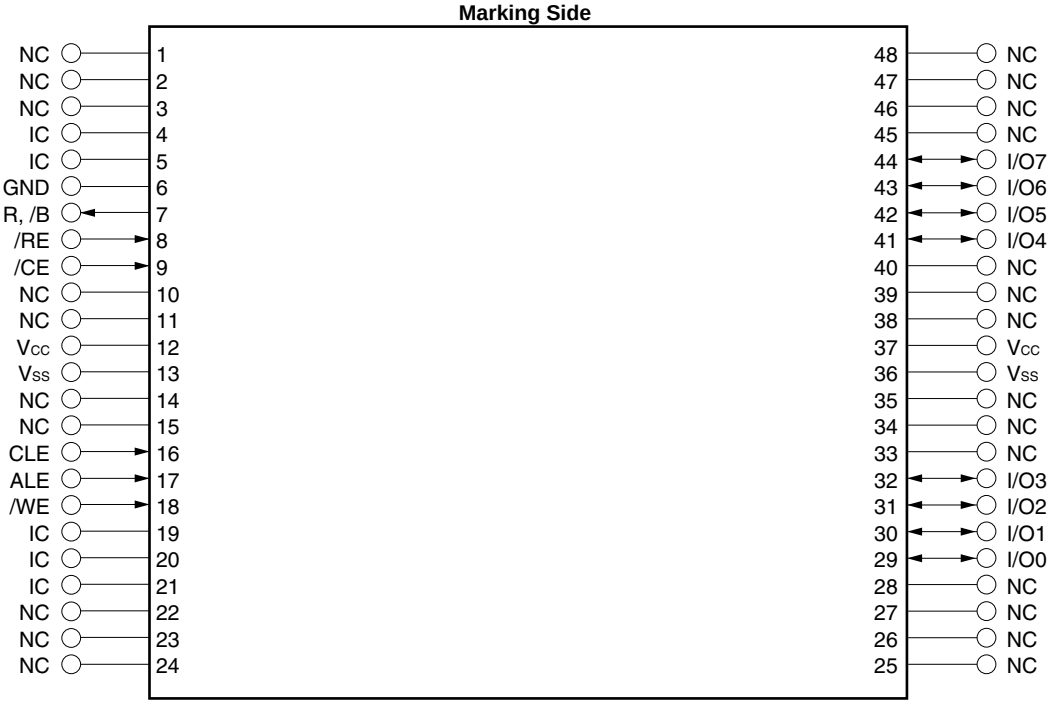
/xxx indicates active low signal.

48-pin PLASTIC TSOP(I) (12x18) (Normal bent)

[μPD23C256112AGY-xxx-MJH]

<R> **[μPD23C256112AGY-xxx-MJH-A]**

Marking Side



I/O0 to I/O7	: Address Inputs / Command Inputs / Data Outputs
CLE	: Command Latch Enable Input
ALE	: Address Latch Enable Input
/WE	: Write Enable Input
/RE	: Read Enable Input
/CE	: Chip Enable Input
R, /B[Note1]	: READY, /BUSY Output
Vcc	: Supply voltage
Vss	: Ground
NC[Note2]	: No connection
IC[Note3]	: Internal connection
GND	: GND

Notes 1. This pin is an open-drain output pin. Therefore, a pull-up resistor is required when using this pin.

2. Some signals can be applied because this pin is not connected to the inside of the chip.

3. Leave this pin unconnected or connected to Vss.

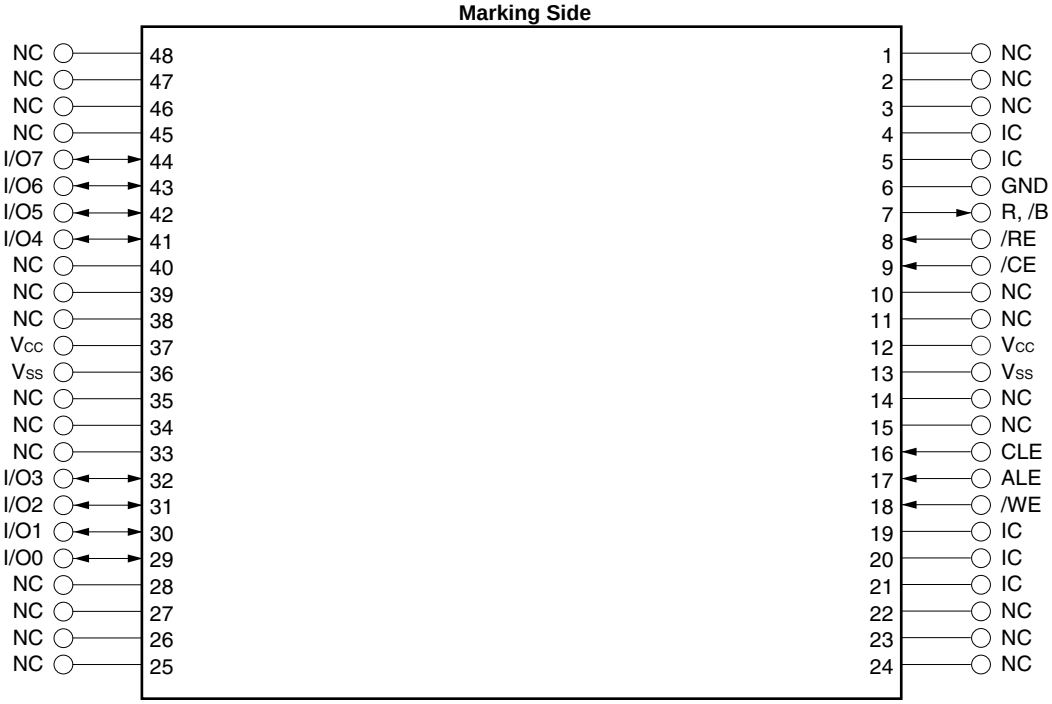
Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

[μPD23C256112AGY-xxx-MKH]

<R> **[μPD23C256112AGY-xxx-MKH-A]**

Marking Side



I/O0 to I/O7	:	Address Inputs / Command Inputs / Data Outputs
CLE	:	Command Latch Enable Input
ALE	:	Address Latch Enable Input
/WE	:	Write Enable Input
/RE	:	Read Enable Input
/CE	:	Chip Enable Input
R, /B[Note1]	:	READY, /BUSY Output
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2. Some signals can be applied because this pin is not connected to the inside of the chip.

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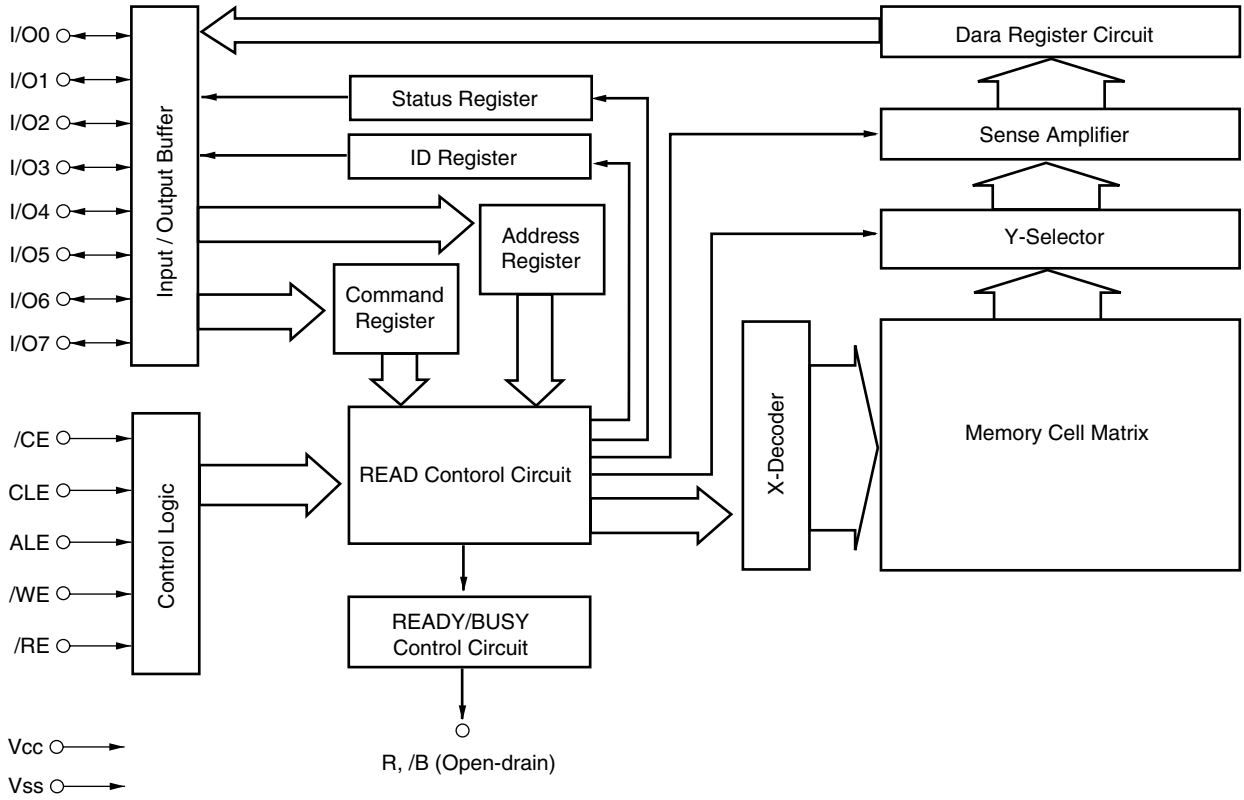
Remark Refer to **Package Drawings** for the 1-pin index mark.

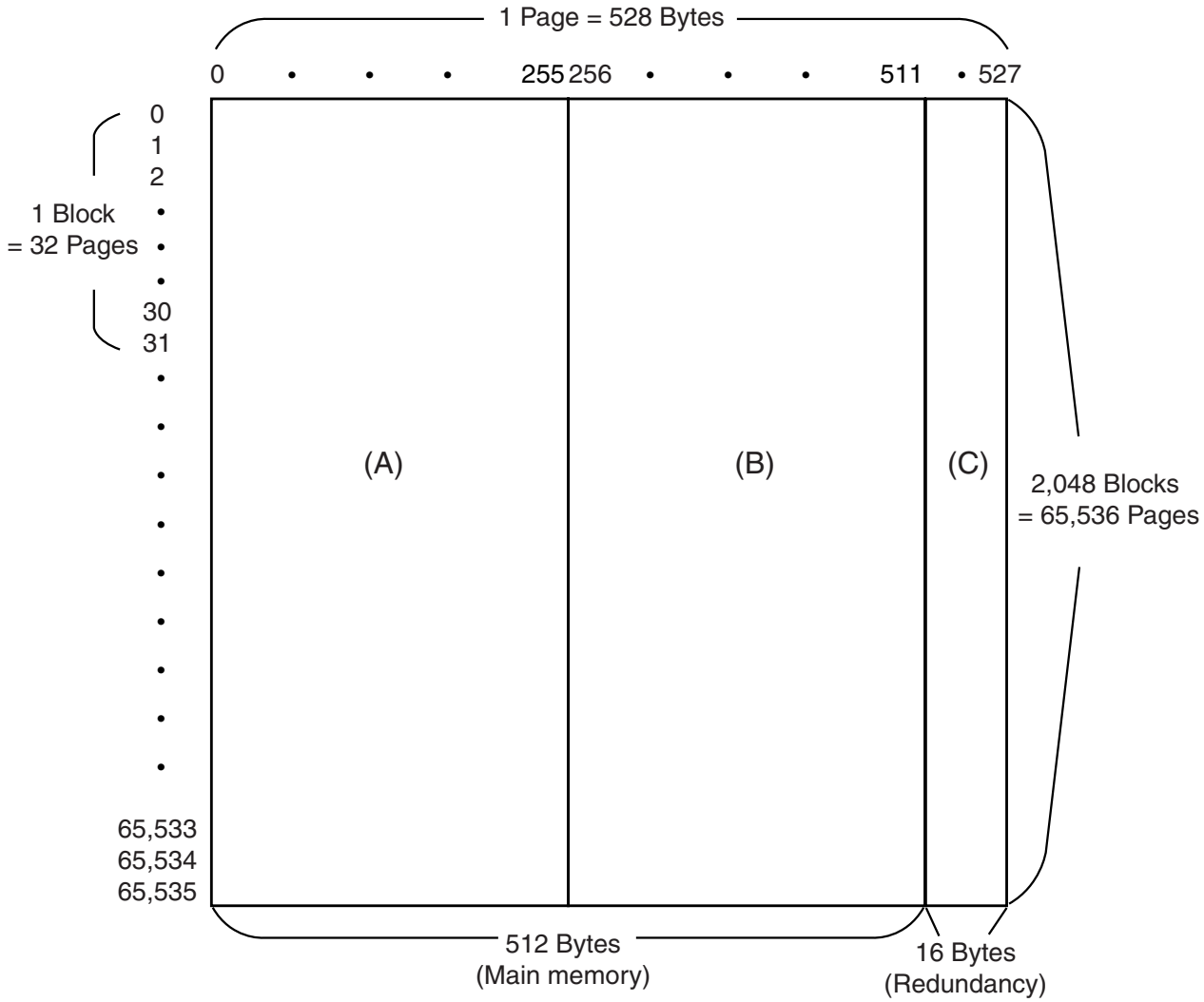
Input / Output Pin Functions

Pin name	Input / Output	Function
I/O0 to I/O7 (Address Inputs / Command Inputs / Data Outputs)	Input, Output	I/O port for address input, command input, and data output. I/O pins.
CLE (Command latch Enable Input)	Input	Input pin for signal for controlling loading of commands to command register in device. By making this signal high level at the rising edge or falling edge of the /WE signal, the data of the I/O0 to I/O7 pins is loaded to the command register as commands.
ALE (Address latch Enable Input)	Input	Input pin for signal for controlling loading of address data to the address register in the device. By making this signal high level at the rising edge or falling edge of the /WE signal, the data of the I/O0 to I/O7 pins is loaded as address.
/WE (Write Enable Input)	Input	Input pin for signal for loading the data from the I/O0 to I/O7 pins inside the device.
/RE (Read Enable Input)	Input	Input pin for signal for serially outputting data. The output data of I/O0 to I/O7 is determined after t_{REA} from the falling edge of the /RE signal, and the internal address counter is incremented by +1 at the rising edge of the /RE signal.
/CE (Chip Enable Input)	Input	Input pin for device selection signal. During read, the standby mode is entered by making this signal high level.
R, /B (READY, /BUSY Output)	Output	Output pin for signal that notifies the internal operating status of the device to external. This is an open-drain output signal. During read, Busy is output during operation (R, /B = low level), and upon completion, Ready (R, /B = high level) is automatically output.

Block Diagram



Memory Area



- The start address (SA) during read operation is specified divided into three areas using three types of read commands.

  In read mode (1), start address (SA) is set in area (A).

  In read mode (2), start address (SA) is set in area (B).

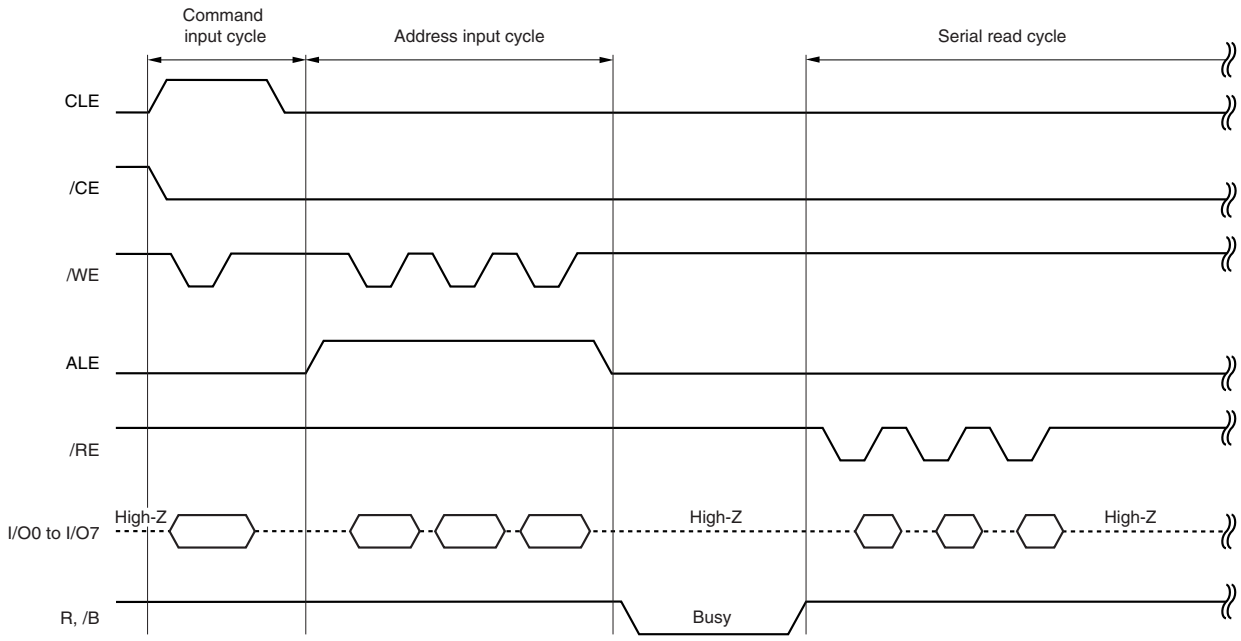
  In read mode (3), start address (SA) is set in area (C).

One page consists of a total of 528 bytes broken down into 512 bytes (main memory) and 16 bytes (redundancy).
One block consists of 32 pages.

Caution The data of area (C) is redundancy. Redundancy is not programmable parts and is fixed to all FFH.

Operation Modes

Command input, address input, and serial read are all performed from I/O pins, and the respective statuses are controlled by the CLE, ALE, /WE, /RE, and /CE signals.



Operation mode

Mode	CLE	ALE	/CE	/WE	/RE
Command input cycle	H	L	L	↑	H
Address input cycle	L	H	L	↑	H
Serial read cycle	L	L	L	H	↓

Operation mode during serial read

Mode	CLE	ALE	/CE	/WE	/RE	I/O0 to I/O7
Data output	L	L	L	H	L	Data output
Output High-Z	L	L	L	H	H	High-Z
Standby	L	L	H	H	×	High-Z

Remark × : V_{IH} or V_{IL}

Operation Commands

The following six operation settings are possible by inputting commands from I/O pins.

Command	HEX	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Command receivable during Busy
Read mode(1)	00H	L	L	L	L	L	L	L	L	
Read mode(2)	01H	L	L	L	L	L	L	L	H	
Read mode(3)Note1	50H	L	H	L	H	L	L	L	L	
ResetNote2	FFH	H	H	H	H	H	H	H	H	○
Status read	70H	L	H	H	H	L	L	L	L	
ID readNote3	90H	H	L	L	H	L	L	L	L	

Notes 1. The data output in read mode (3) is all FFH.

2. The only command that can be executed when the device is Busy is the reset command. Do not set any of the other commands while the device is Busy.

3. For ID read, input “00H” during the first address cycle after setting a command.

I/O Pin Correspondence Table during Address Input Cycle (Address Setting)

(1) When 00H or 01H command is set [Read mode (1), Read mode (2)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	A24	A23	A22	A21	A20	A19	A18	A17

(2) When 50H command is set [Read mode (3)]

Command	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st address cycle	×	×	×	×	A3	A2	A1	A0
2nd address cycle	A16	A15	A14	A13	A12	A11	A10	A9
3rd address cycle	A24	A23	A22	A21	A20	A19	A18	A17

Remarks 1. A0 to A24 are internal addresses.

2. Internal address A8 is set internally with command 00H or 01H.

3. When 50H command is set [read mode (3)], the I/O4, I/O5, I/O6, and I/O7 inputs of the 1st address cycle are V_{IH} or V_{IL}.

Usage Cautions

(1) Rated operation

Operation using timing other than shown in the timing charts is not guaranteed.

(2) Commands that can be input

The only commands that can be input are 00H, 01H, 50H, 70H, 90H, and FFH. Do not input any other commands. If other commands are input, the subsequent operation is not guaranteed.

(3) Command limitations during Busy period

Do not input commands other than the reset command (FFH) during the Busy period. If a command is input during the Busy period, the subsequent operation is not guaranteed.

(4) Cautions regarding /RE clock

- Following the last /RE clock, do not input the /RE clock until the R, /B pin changes from Busy to Ready.
- Do not input the /RE clock other than during data output.

(5) Cautions upon power application

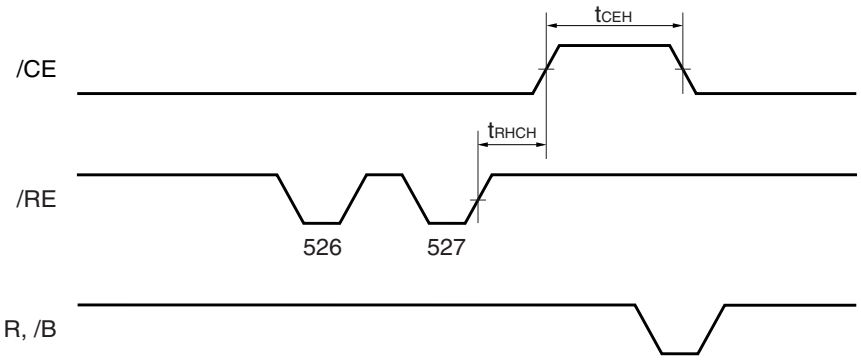
Since the state of the device is undetermined upon power on, input high level to the /CE pin and execute the reset command following power on.

(6) Cautions during read mode

- Perform address input immediately following command input. If address input is done without performing command input first, the correct data cannot be output because the operation mode is undetermined.
- To execute the read mode after the read mode has been stopped with the reset command (FFH) and /CE, input again a command and address.

(7) Busy output following access of last address in page in read mode

After the access to the last address in a page, if the delay (t_{RHCH}) from /RE to /CE is 30 ns or less, the Ready status is maintained and Busy is not output by keeping /CE high level for a set period (t_{CEH}).



Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Input / Output voltage	$V_{I/O}$		–0.3 to V_{CC}+0.3 (≤ 4.6)	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25°C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				10	pF

DC Characteristics (T_A = 0 to 70°C, V_{CC} = 3.3 ± 0.3 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH}	I_{OH} = –400 μA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}			±10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}			±10	μA
Power supply current in read	I_{CCO1}	/CE = V_{IL}, I_{OUT} = 0 mA, t_{CYCLE} = 50 ns			30	mA
Power supply current in command input	I_{CCO3}	t_{CYCLE} = 50 ns			30	mA
Power supply current in address input	I_{CCO5}	t_{CYCLE} = 50 ns			30	mA
Standby current (TTL)	I_{CCS1}	/CE = V_{IH}			1	mA
Standby current (CMOS)	I_{CCS2}	/CE = V_{CC} – 0.2 V			100	μA
(R, /B) pin output current	$I_{OL(R, /B)}$	V_{OL} = 0.4 V		8		mA

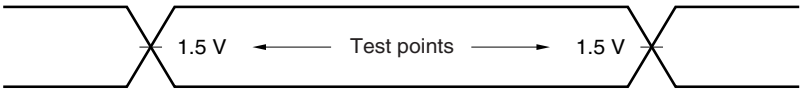
AC Characteristics (T_A = 0 to 70°C, V_{CC} = 3.3 ± 0.3 V)

Parameter	Symbol	MIN	TYP.	MAX.	Unit
CLE setup time	t_{CLS}	0			ns
CLE hold time	t_{CLH}	10			ns
/CE setup time	t_{CS}	0			ns
/CE hold time	t_{CH}	10			ns
Write pulse width	t_{WP}	25			ns
ALE setup time	t_{ALS}	0			ns
ALE hold time	t_{ALH}	10			ns
Data setup time	t_{DS}	20			ns
Data hold time	t_{DH}	10			ns
Write cycle time	t_{WC}	50			ns
/WE high hold time	t_{WH}	15			ns
Ready to /RE falling edge	t_{RR}	20			ns
Read pulse width	t_{RP}	35			ns
Read cycle time	t_{RC}	50			ns
/RE access time (serial data access)	t_{REA}			35	ns
/CE high hold time for last address in serial read cycle	t_{CEH}	100			ns
/RE access time (ID read)	t_{REAID}			35	ns
/RE high to output High-Z	t_{RHZ}	10		30	ns
/CE high to output High-Z	t_{CHZ}			20	ns
/RE high hold time	t_{REH}	15			ns
Output High-Z to /RE falling edge	t_{IR}	0			ns
/RE access time (status read)	t_{RSTO}			35	ns
/CE access time (status read)	t_{CSTO}			45	ns
/WE high to /CE low	t_{WHC}	30			ns
/WE high to /RE low	t_{WHR}	30			ns
ALE low to /RE low (ID read)	t_{AR1}	100			ns
/CE low to /RE low (ID read)	t_{CR}	100			ns
Memory cell array to starting address	t_R			7	μs
/WE high to Busy	t_{WB}			200	ns
ALE low to /RE low (read cycle)	t_{AR2}	50			ns
/RE last clock rising edge to Busy (in sequential read)	t_{RB}			200	ns
/CE high to Ready (when interrupted by /CE in read mode)	t_{CRY} Note			1	μs
Device reset time	t_{RST}			6	μs

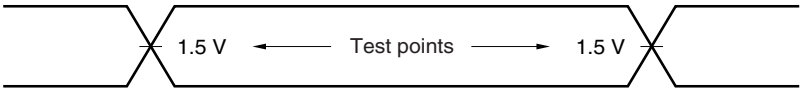
Note t_{CRY} (time from /CE high to Ready) depends on the pull-up resister of the R, /B output pin.

AC Test Conditions

Input waveform (Rise / Fall Time ≤ 5 ns)



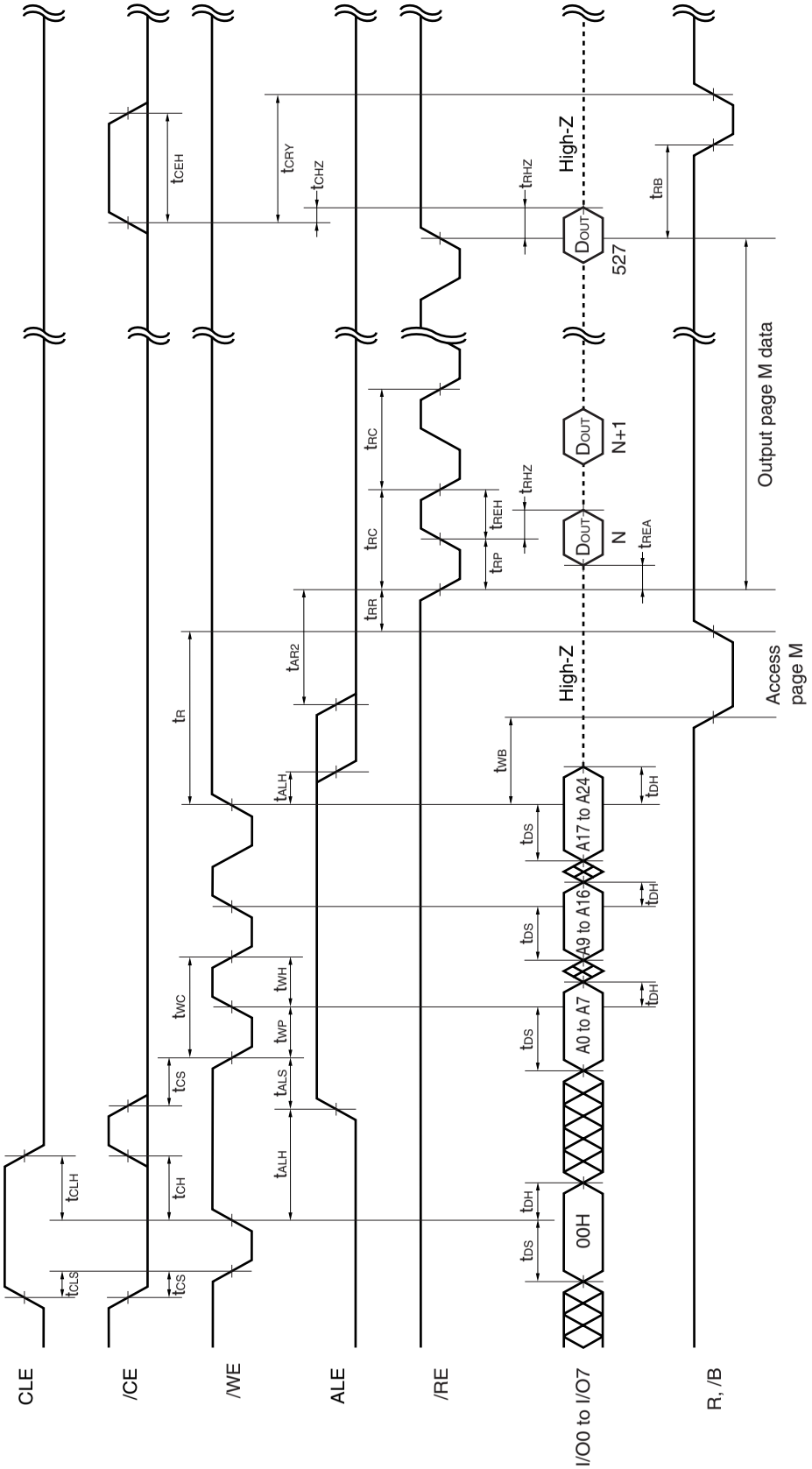
Output waveform



Output load

1 TTL + 100 pF

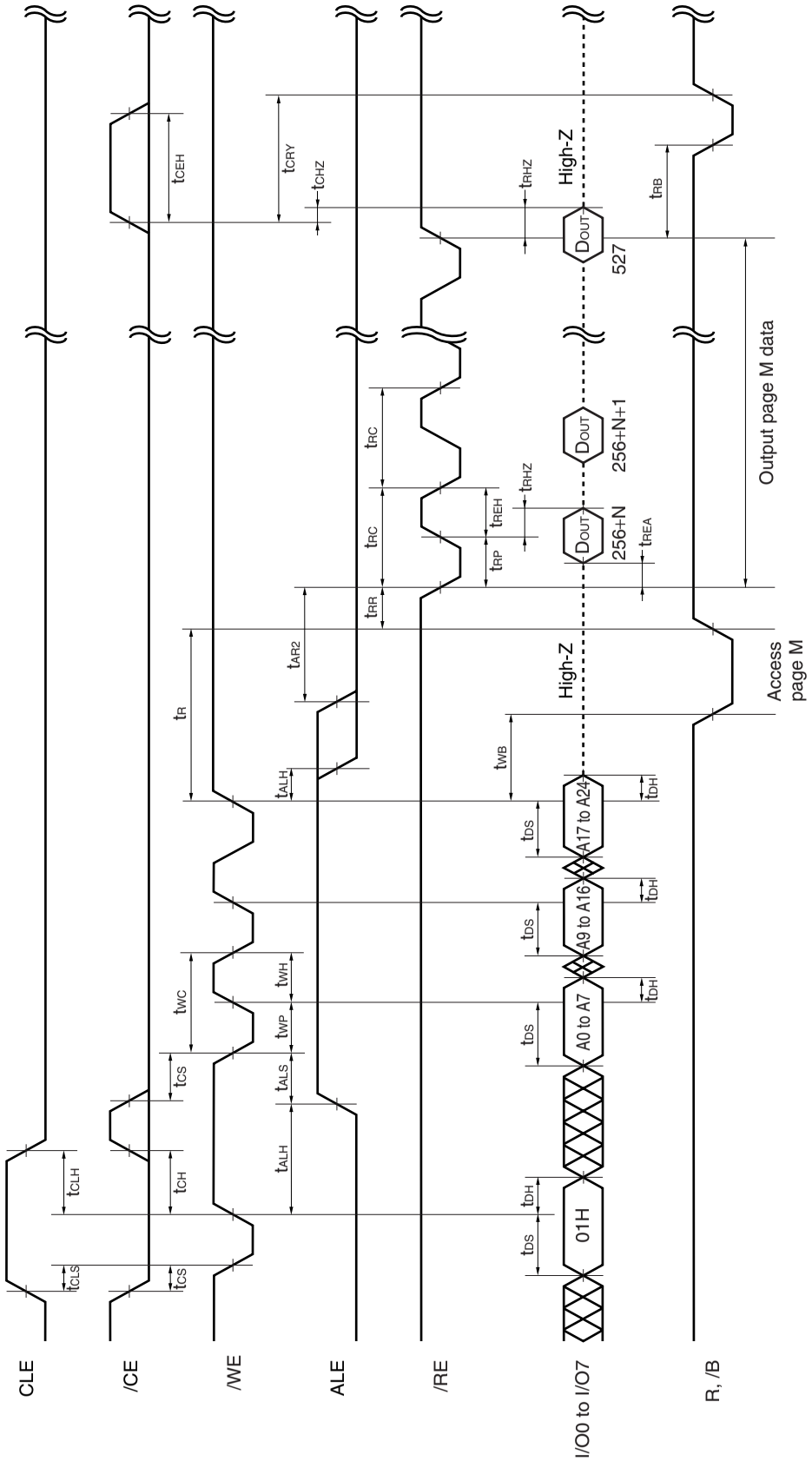
Read Cycle Timing Chart (1)
(In case of read mode (1))



Remarks 1. Start address (SA) specification when read is performed with command 00H. N: 0 to 255

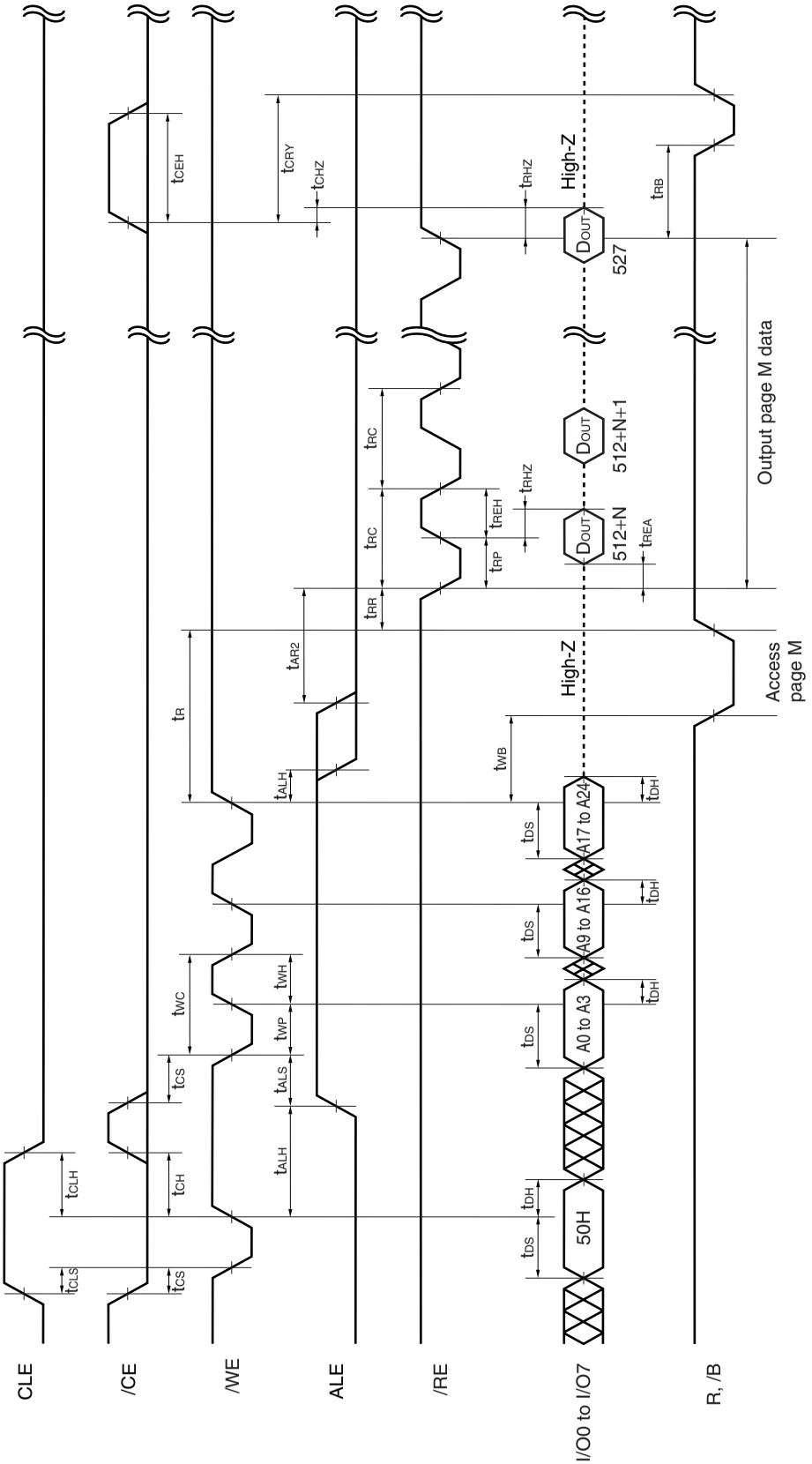
2. Then time (t_{CRY}) from /CE high to Ready is cancelled depends on the pull-up register of the R,/B output pin.

Read Cycle Timing Chart (2)
(In case of read mode (2))



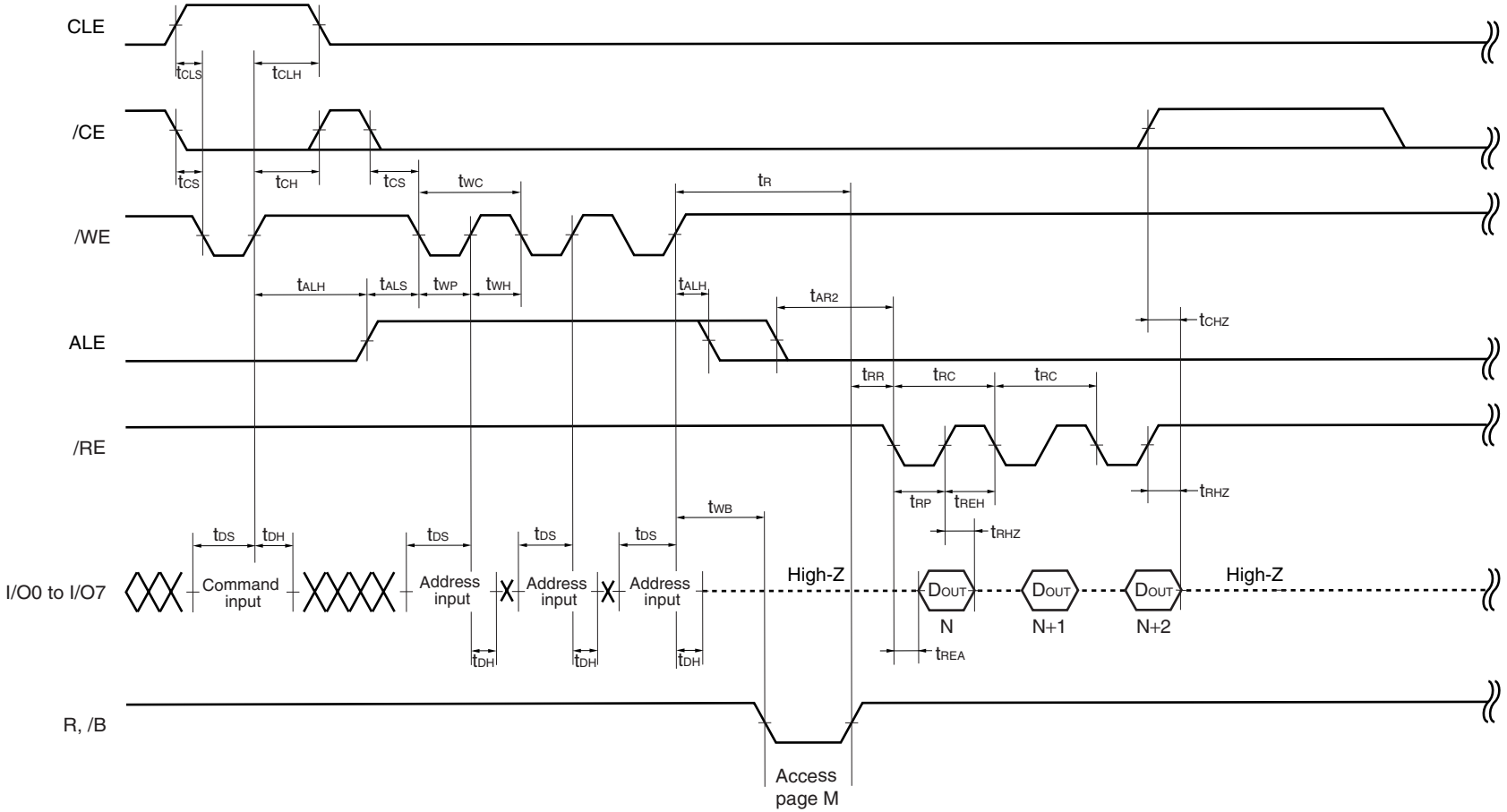
Remarks 1. Start address (SA) specification when read is performed with command 01H. N: 0 to 255
2. Then time (t_{CRY}) from /CE high to Ready is cancelled depends on the pull-up register of the R, /B output pin.

Read Cycle Timing Chart (3)
(In case of read mode (3))



Remarks 1. Start address (SA) specification when read is performed with command 50H. N: 0 to 15
2. The start address of area C (redundancy data) is specified with A0 to A3 during the 1st address cycle. At this time, A4 to A7 are Don't Care.
3. The time (t_{CRY}) from /CE high to Ready is cancelled depends on the pull-up register of the R, /B output pin.
4. The data that is output is FFH.

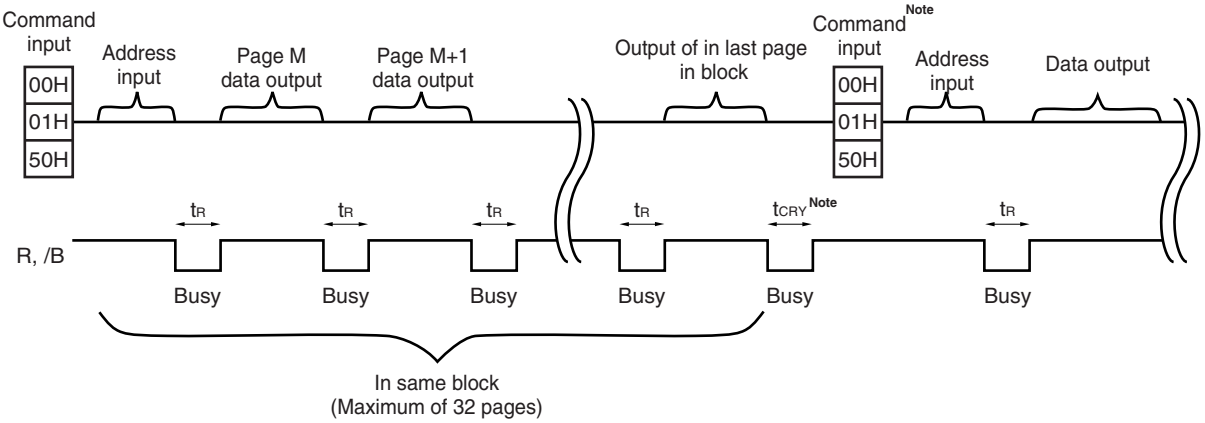
Read Cycle Timing Chart (4)
(When /CE is made high level in the read mode)



Remark If /CE is made high level during the read cycle, the read operation until that time is cancelled. Therefore, to perform read again, execute a new command and new address input.

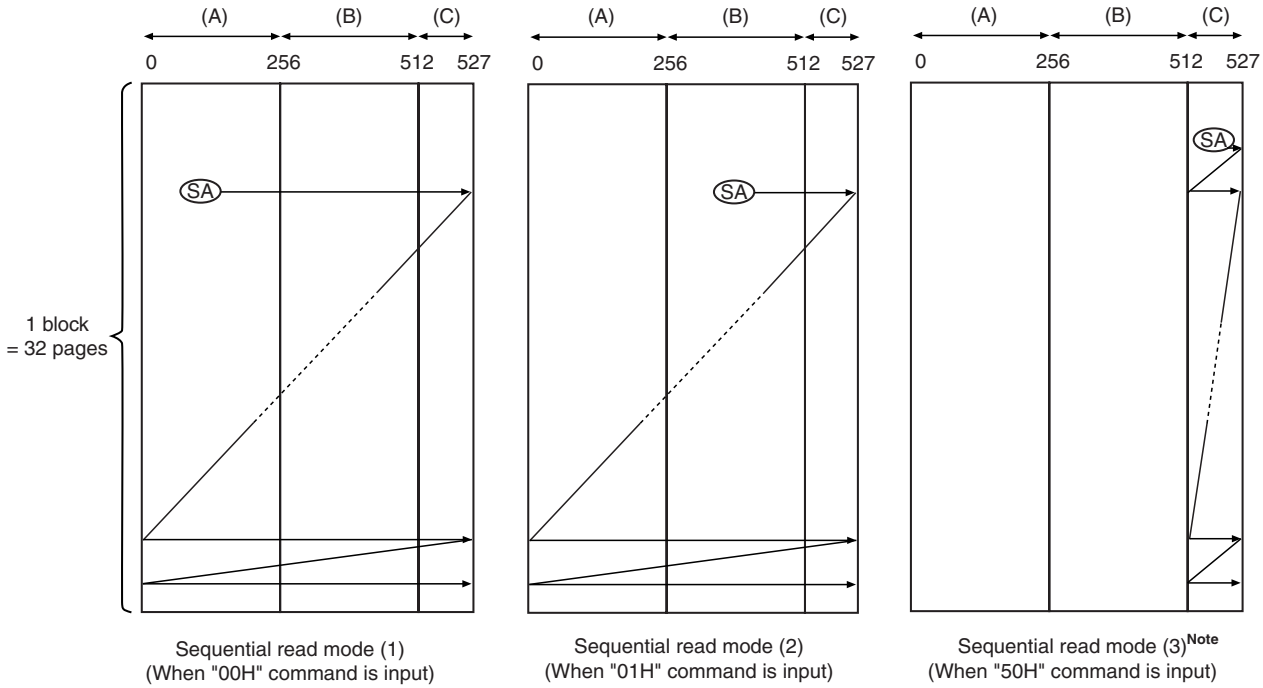
Sequential Read

In read modes (1), (2), and (3), when a command (00H, 01H, 50H) is input and an address specified, if it is in the block that includes the address that was specified first, the address is automatically incremented and the read operation is continuously performed until the last address in the same block, by inputting the /RE clock. At this time, a Busy period (t_R) occurs after the last address is accessed in a page.



Note To perform read again after reading the 527th byte of data of the last page of block, stop the read operation once, and then restart the read operation by inputting again the read command and an address.

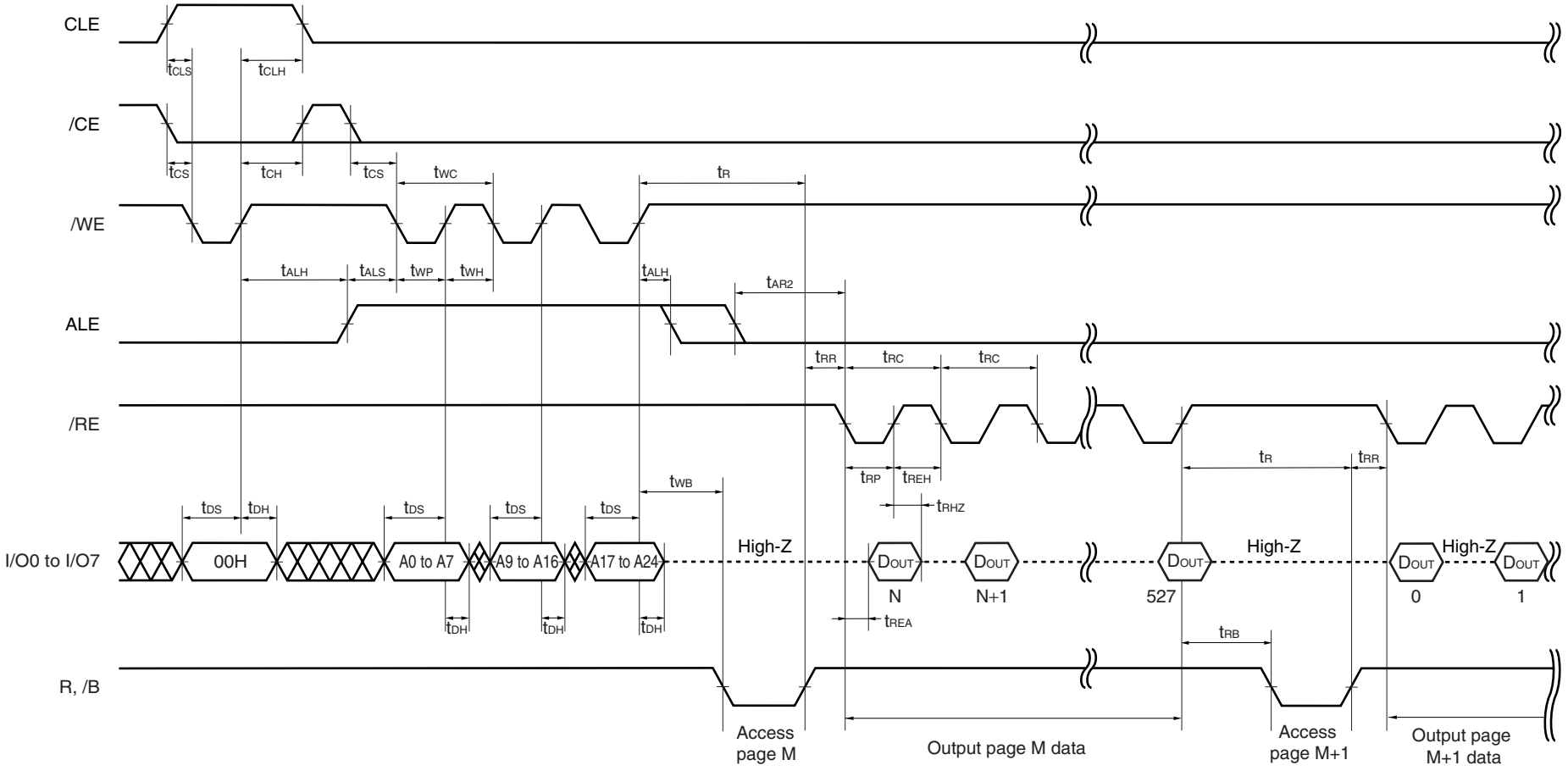
Relationship Between Command and Start Address (SA) during Sequential Read



Note When the "50H" command is set, only the (C) area (redundancy data part) is continuously read.

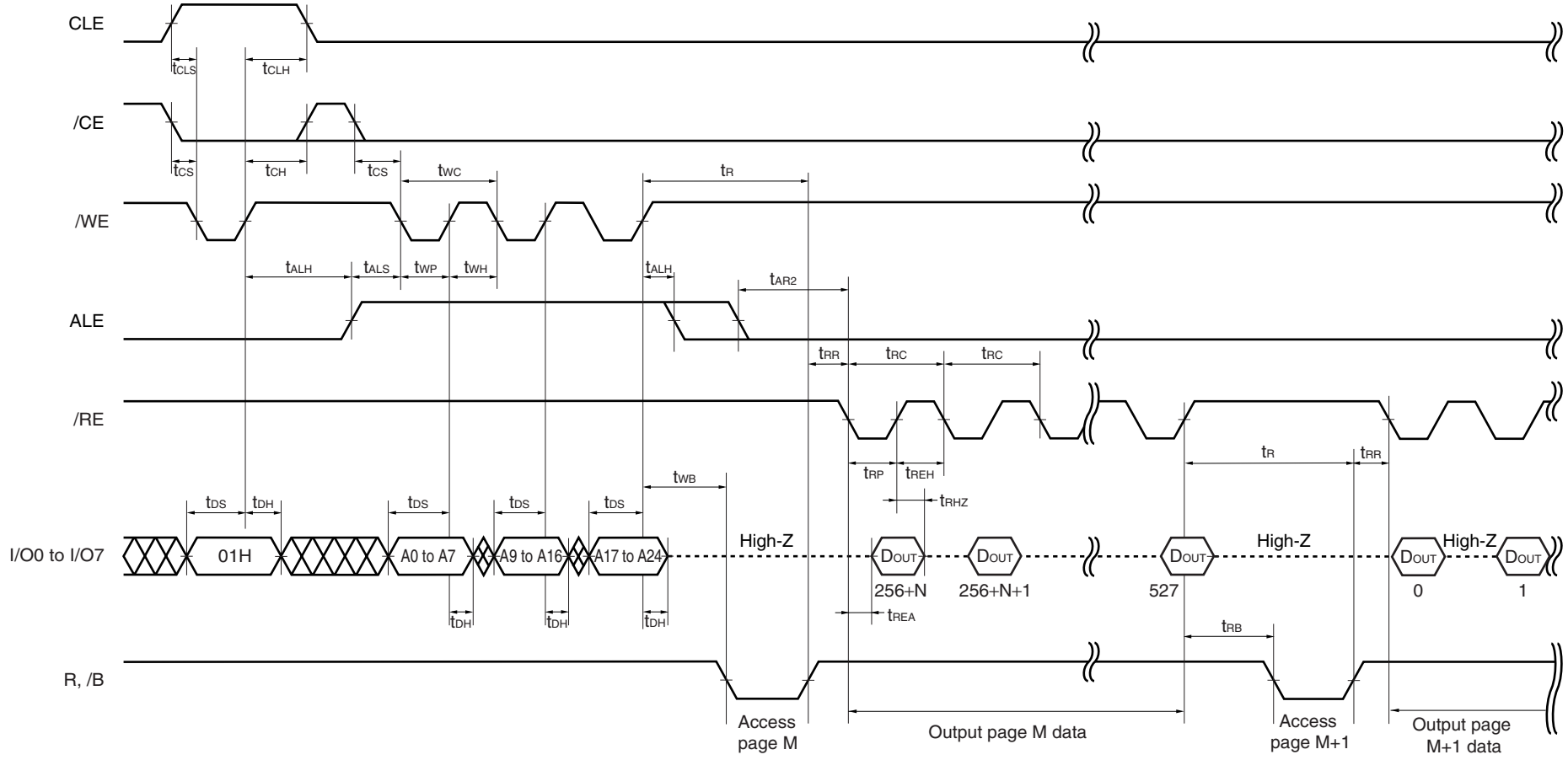
- When the “00H” command is set, the start address (SA) is set to area (A).
- When the “01H” command is set, the start address (SA) is set to area (B).
- When the “50H” command is set, the start address (SA) is set to area (C).

Sequential Read Cycle Timing Chart (1)
(In case of read mode (1))



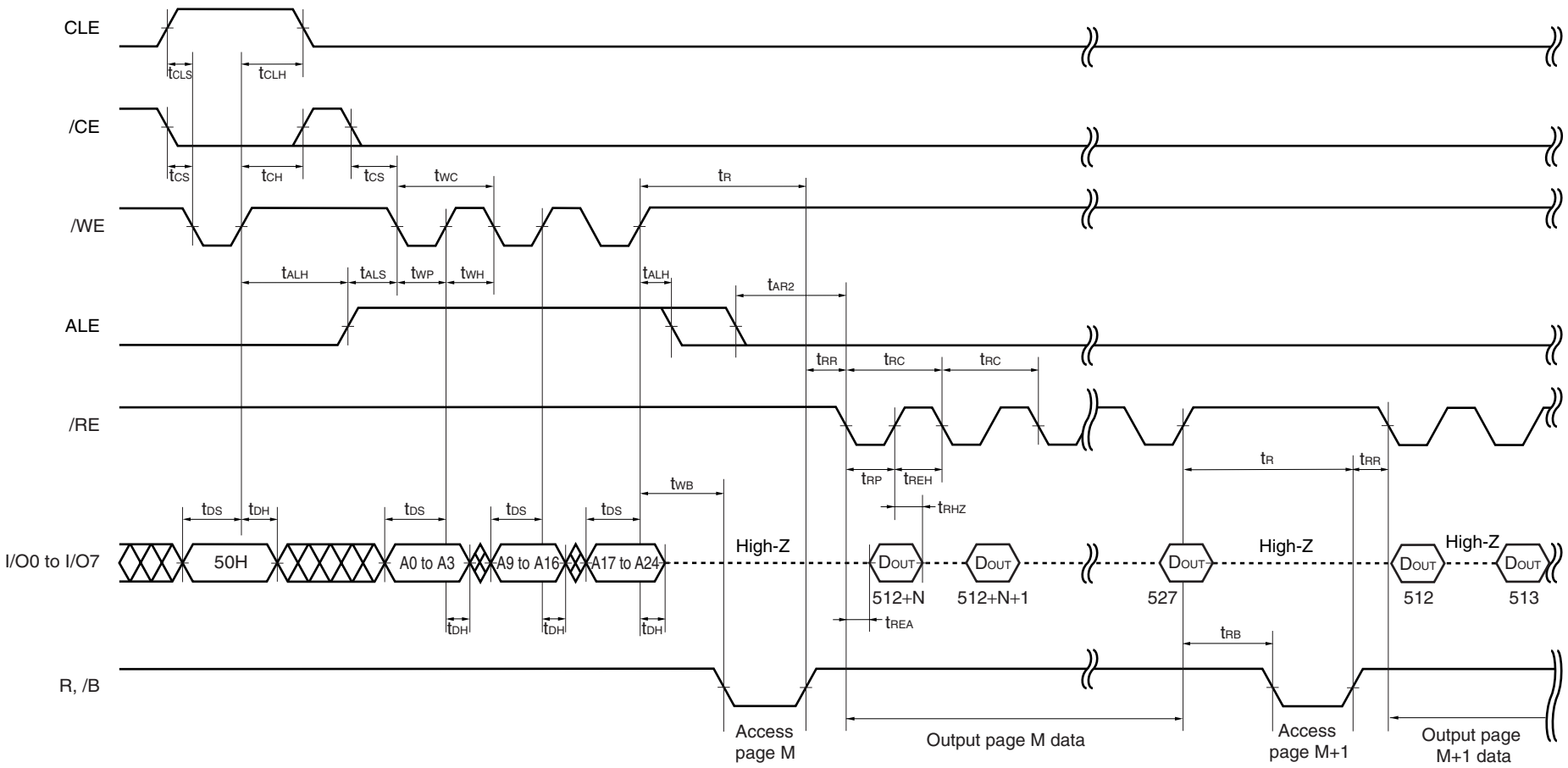
Remark Start address (SA) specification when read is performed with command 00H. N: 0 to 255

Sequential Read Cycle Timing Chart (2)
(In case of read mode (2))



Remark Start address (SA) specification when read is performed with command 01H. N: 0 to 255

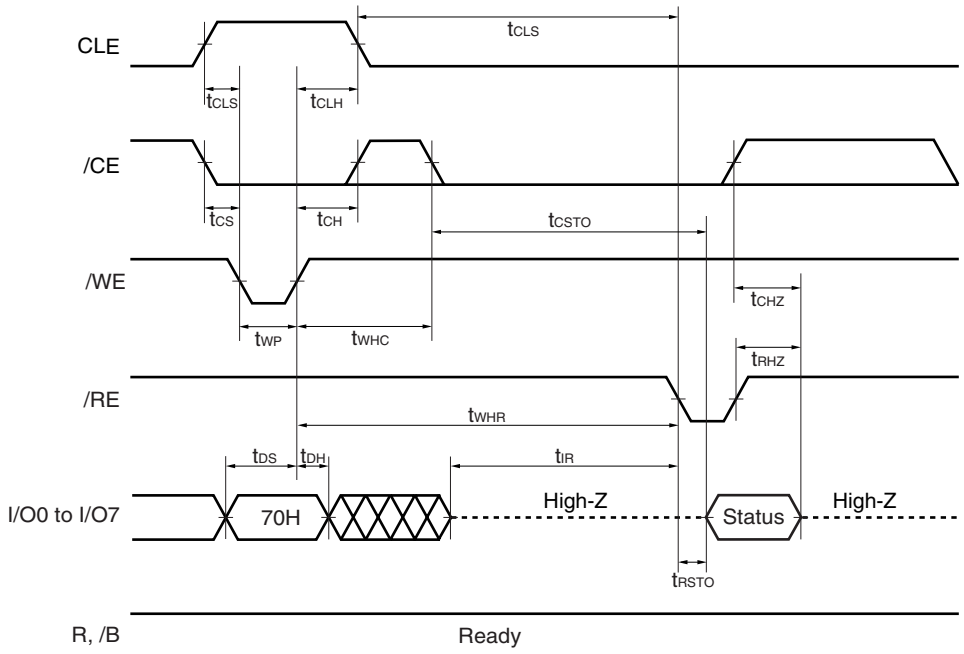
Sequential Read Cycle Timing Chart (3)
(In case of read mode (3))



Remark Start address (SA) specification when read is performed with command 50H. N: 0 to 15

Status Read

Status information can be output from the I/O pins with the /RE clock following input of the 70H command. Status read is a function to recognize the status of the device from external.

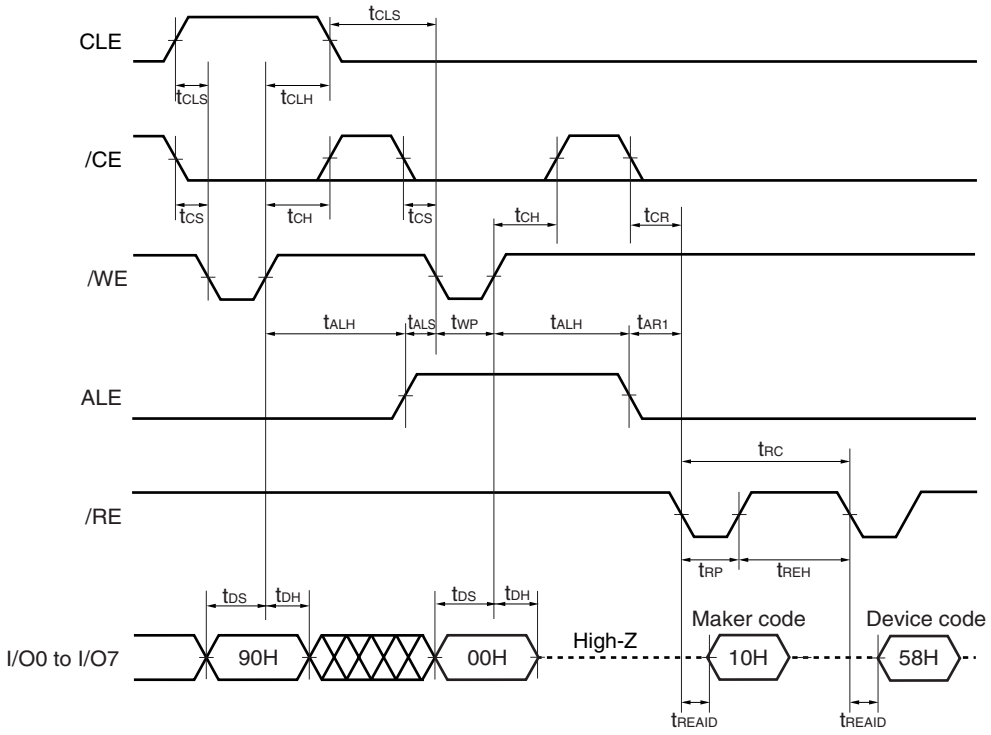


	Status	Status output data [Note]
I/O0	Ready / Busy	0 / 1
I/O1	Not used	0
I/O2	Not used	0
I/O3	Not used	0
I/O4	Not used	0
I/O5	Not used	0
I/O6	Ready / Busy	1 / 0
I/O7	Write protect	0

Note Use the status read command only during Ready.

ID Read

To recognize the ID code (maker code / device code) of this device in a system, execute the ID read command. The ID code can be read with the following timing.

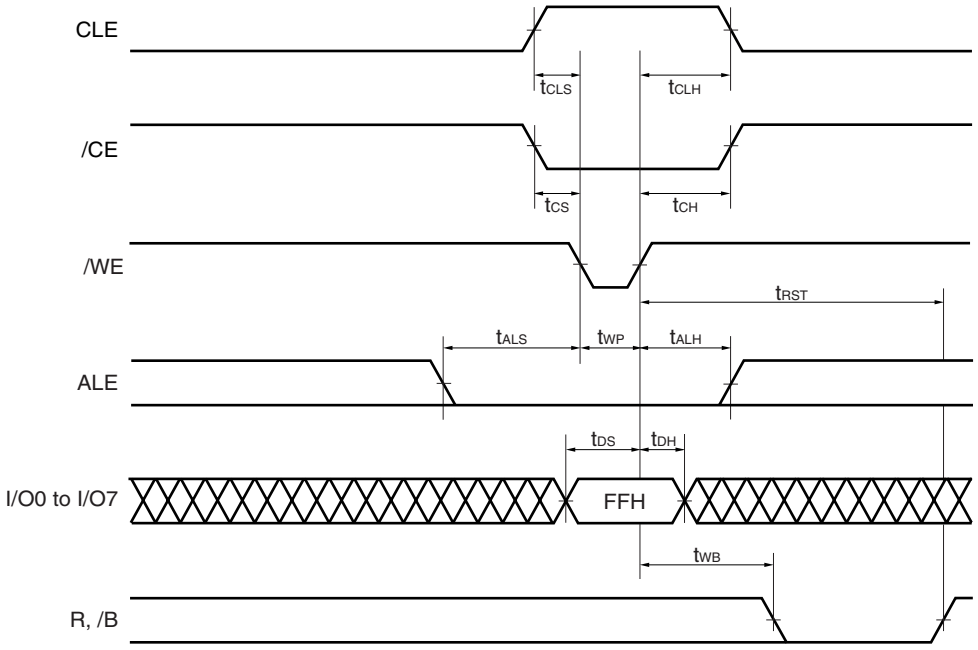


	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	HEX
Maker code	L	L	L	H	L	L	L	L	10H
Device code	L	H	L	H	H	L	L	L	58H

Cautions 1. If the /RE clock is input after the maker code and device code are output, the output data is not guaranteed. Therefore, do not input the /RE clock following device code output.

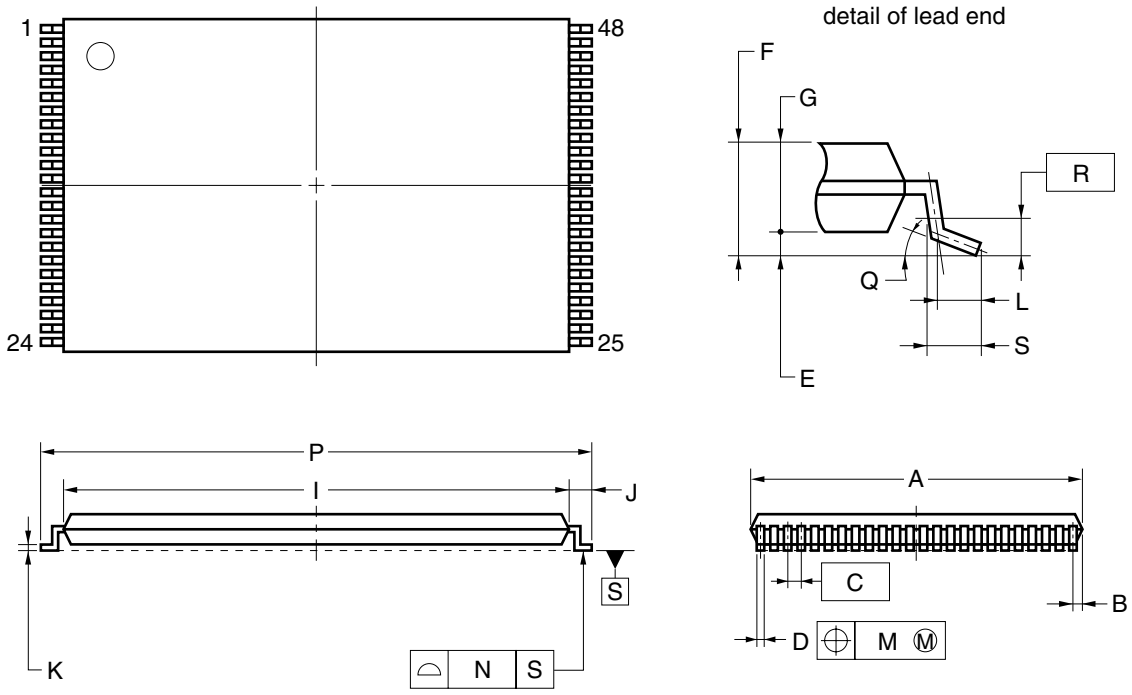
2. Do not input an address other than 00H after setting the ID read command (90H). If an address other than 00H is input, the data following /RE clock input is not guaranteed.

Reset Cycle Timing Chart



Package Drawings

48-PIN PLASTIC TSOP(I) (12x18)



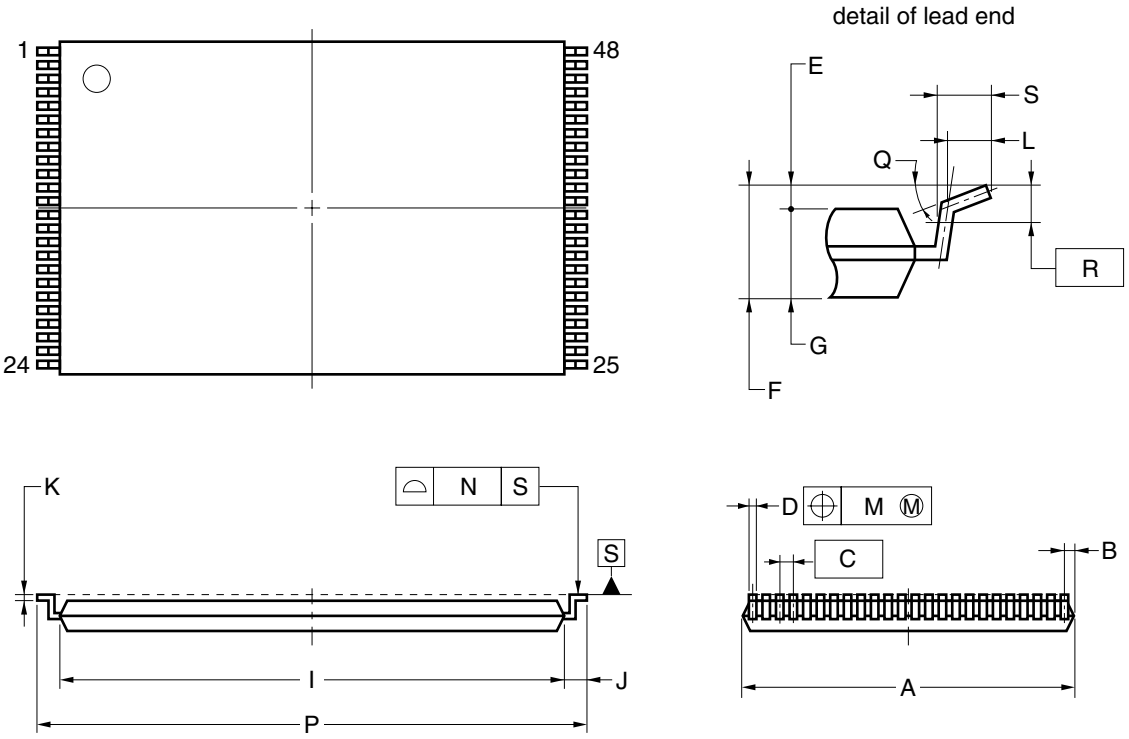
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

48-PIN PLASTIC TSOP(I) (12x18)



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S48GY-50-MKH1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C256112A.

Types of Surface Mount Device

μPD23C256112AGY-MJH : 48-pin PLASTIC TSOP(I) (12x18) (Normal bent)

μPD23C256112AGY-MKH : 48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

<R> μPD23C256112AGY-MJH-A : 48-pin PLASTIC TSOP(I) (12x18) (Normal bent)

<R> μPD23C256112AGY-MKH-A : 48-pin PLASTIC TSOP(I) (12x18) (Reverse bent)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Feb. 2006	p.2	p.1	Addition	Ordering Information	Lead-free products have been added
	pp.3,4	pp.2,3	Addition	Pin Configuration	Lead-free products have been added
	p.27	p.26	Addition	Recommended Soldering Conditions	Lead-free products have been added

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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