PRELIMINARY

Switching Driver with Regulator for Class-D Headphone Amplifier

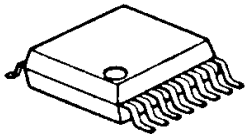
■ GENERAL DESCRIPTION

The **NJU8716A/B** is switching driver with regulator for class-D headphone amplifier. It incorporates optimum regulator for the driver of headphone amplifier.

The **NJU8716A/B** converts 1bit audio signals such as PWM/PDM to analog audio signals with simple external LC low-pass filter.

The **NJU8716A/B** provides completed digital system and high power-efficiency with class-D operation. Therefore it is suitable for portable audio applications.

■ PACKAGE OUTLINE

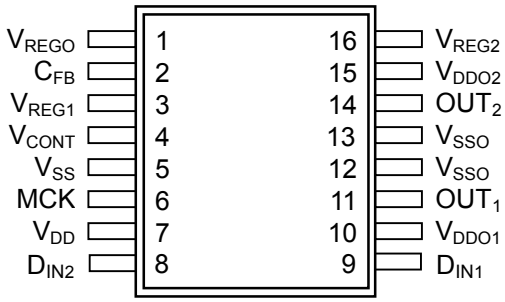


NJU8716AV, NJU8716BV

■ FEATURES

- 2-channel 1bit Audio Signal Input
- Headphone Output
- Built-in Regulator for Driver
- Logic Operating Voltage 1.7~3.0V(V_{DD})
- Driver Operating Voltage 1.6~3.5V(V_{DDO1}, V_{DDO2})
- Regulator Operating Voltage 4.0~5.75V(V_{REG1})
  1.9~4.0V(V_{REG2})
- C-MOS Technology
- Package Outline SSOP16

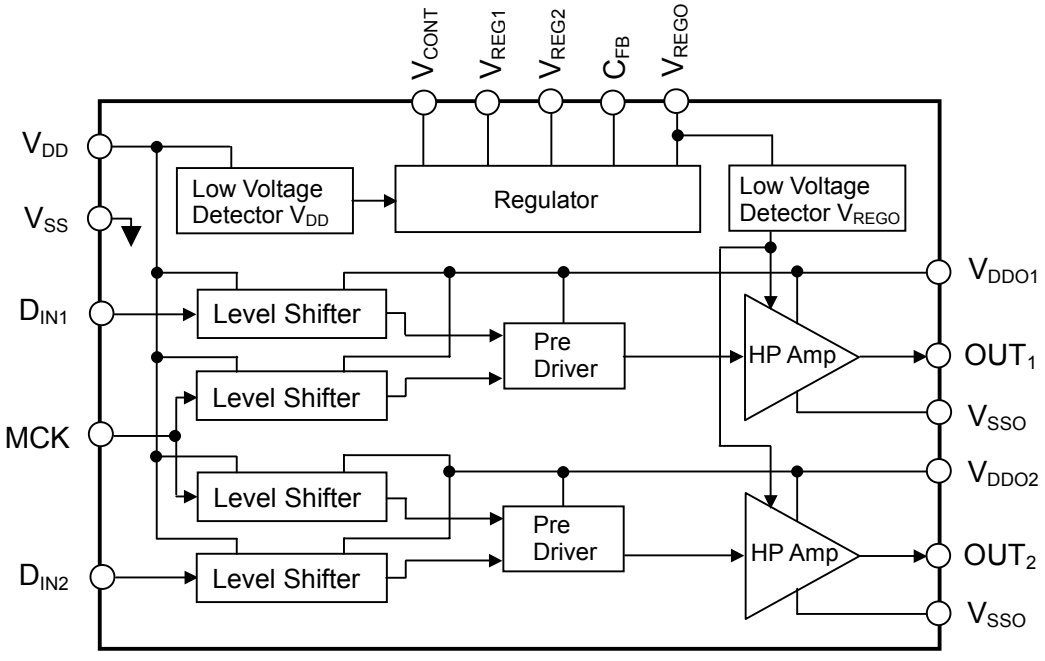
■ PIN CONFIGURATION



■ Version Lineup

Version	Data Latch
NJU8716A	The rising edge of MCK
NJU8716B	The falling edge of MCK

■ BLOCK DIAGRAM

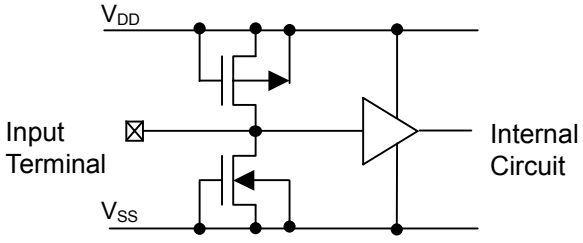


■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
1	V_{REGO}	O	Regulator Output Terminal
2	C_{FB}	I	Regulator Output Voltage Sense Terminal
3 16	V_{REG1} V_{REG2}	-	Regulator Power Supply
4	V_{CONT}	I	Regulator Output Voltage Control Terminal
5	V_{SS}	-	Power GND:V_{SS}=0V
6	MCK	I	Master Clock Input Terminal Audio signals are latched on the edge of MCK. A Version: latched on the rising edge B version: latched on the falling edge
7	V_{DD}	-	Power Supply: V_{DD}=2.0V
9 8	D_{IN1} D_{IN2}	I	Audio Signal Input Terminal 1,2
10 15	V_{DDO1} V_{DDO2}	-	Driver Power Supply 1,2
11 14	OUT_1 OUT_2	O	Output Terminal 1,2
12 13	V_{SSO}	-	Driver GND: V_{SSO}=0V

■ INPUT TERMINAL STRUCTURE

MCK, D_{IN1}, D_{IN2}



■ FUNCTIONAL DESCRIPTION

(1) Power Supply

V_{DD} : Power supply for input circuit and control logic. Keep the input logic level less than V_{DD}.
If V_{DD} reaches less than sleep detection voltage, power consumption can be saved with halts of built-in regulator.

V_{REG1} : Power supply for built-in regulator. Even after power-on, V_{REG1} line is shut off with transistor switch until V_{DD} has been started up.

V_{REG2} : Power supply for built-in regulator. Apply the required voltage with additional dropout voltage of regulator. By connecting V_{REGO} (regulator output) to V_{DDO1}, V_{DDO2} (Driver power supply), the power is provided at the drivers. And furthermore, the regulator output should be supplied to V_{DDO1} and V_{DDO2} by connecting de-coupling capacitor to get highly smoothed power supply.

(2) Regulator Output Voltage Control Terminal (V_{CONT})

V_{CONT} is the control terminal for regulator output voltage. V_{REGO} terminal generates double the voltage of supplied voltage to V_{CONT}. (Shorted between V_{REGO}-C_{FB})

(3) Master Clock (MCK)

Master clock (MCK) synchronizes the audio signal inputs (DIN_1 and DIN_2). The setup time and the hold time should be kept in the AC characteristics because DIN_1 and DIN_2 are fetched with the rising edge of MCK in A version, and the falling edge of MCK in B version. During the standby condition, MCK requires “L” level to avoid unnecessary power consumption. In addition, MCK requires jitter-free or jitter as small as possible because the jitter could lead to poor S/N ratio.

(4) Signal Output (OUT_1 / OUT_2)

OUT_1 and OUT_2 terminals keep the Hi-z condition if output voltage of V_{REGO} is lower than detection voltage. Output signals are appeared as PWM signals through the use of V_{DDO1} and V_{DDO2} in the OUT_1 and OUT_2 terminals If the output voltage is over than detection voltage. Output signals will be converted to analog signals via 2nd-order or higher LC filter.

■ POWER ON/DOWN SEQUENCE

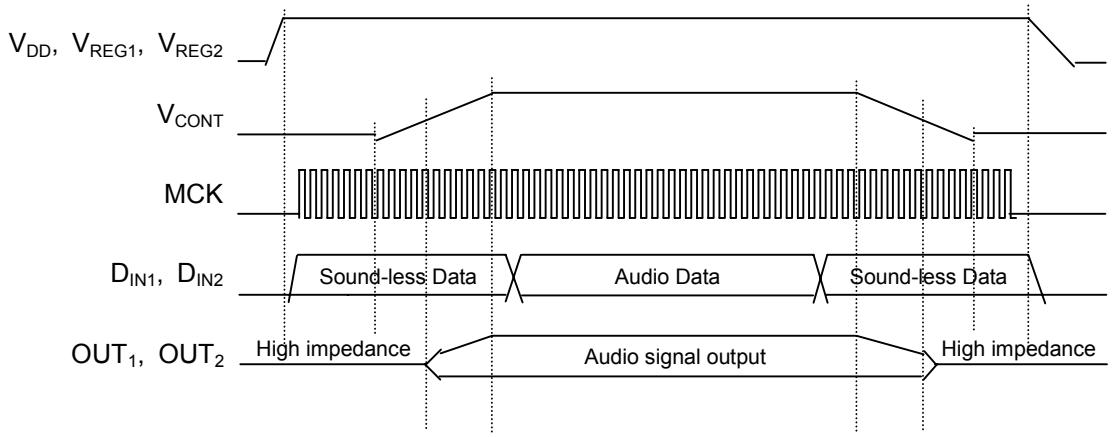
The pop-noise can be effectively suppressed with the following sequence when power ON and OFF.

(1) Power ON Sequence

1) Start up V_{DD}, V_{REG1} and V_{REG2}.
2) Input the master clock (MCK) and audio signals (D_{IN1}, D_{IN2}) after the start-up of V_{DD}, V_{REG1} and V_{REG2}. At this time, audio signals must be input as “Sound-less data”.
3) Increase V_{CONT}.
4) Input the audio data after V_{CONT} reaches a steady state.

(2) Power Down Sequence

The sequence must be executed in inverse order of the power ON sequence.



■ ABSOLUTE MAXMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +4.0	V
	$V_{DDO1, 2}$	-0.3 ~ +4.0	V
	V_{REG1}	V_{REG2} ~ +6.0	V
	V_{REG2}	-0.3 ~ +5.5	V
Input Voltage	Vin	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	Ta	-20 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C
Power Dissipation	P_D	300 (SSOP16)	mW

Note.1) The relations of "V_{DDO1},V_{DDO2}<V_{REG1}", "V_{REG2}<V_{REG1}", and "V_{DD}<V_{REG1}" must be maintained during operations.
Note.2) All voltage are relative to "V_{SS}= V_{SSO}=0V" reference.
Note.3) The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.
Note.4) De-coupling capacitors for "V_{DD}-V_{SS}", "V_{DDO1}-V_{SSO}" and "V_{DDO2}-V_{SSO}" should be connected for stable operation.

■ ELECTRICAL CHARACTERISTIC

(1) DC CHARACTERISTIC

(Ta=25°C, V_{DD}=2.0V, V_{DDO1}=V_{DDO2}=1.8V, V_{REG2}=2.15V, V_{REG1}=5.0V, V_{SS}=V_{SSO}=0.0V, Load Impedance=16Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		1.7	2.0	3.0	V
	V_{DDO}		1.6	1.8	3.5	V
Output Driver High side Resistance	R_H	$OUT_{1, 2}$=V_{DDO}-0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R_L	$OUT_{1, 2}$=0.1V	-	1.5	2	Ω
Power Supply Current At Operating (Mute signal input)	I_{DD}	No-load operating D_{IN1}, D_{IN2}=16f_S MCK=256f_S	-	0.05	0.10	MA
	I_{DDO}		-	0.25	0.5	
Digital Input Voltage	V_{IH}	MCK, D_{IN1}, D_{IN2}	0.7V_{DD}	-	V_{DD}	V
	V_{IL}	MCK, D_{IN1}, D_{IN2}	0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}	MCK, D_{IN1}, D_{IN2}	-	-	±1	μA

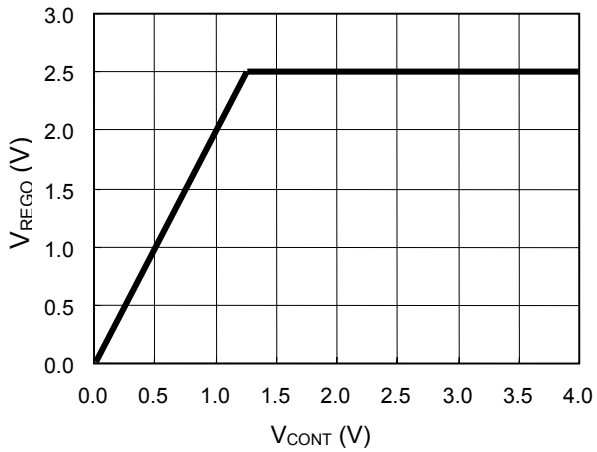
(2) REGULATOR CHARACTERRITICS

(Ta=25°C, V_{DD}=2.0V, V_{DDO1}=V_{DDO2}=1.8V, V_{REG2}=2.15V, V_{REG1}=5.0V, V_{SS}=V_{SSO}=0.0V, Load Impedance=16Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply	V_{REG1}			4.0	-	5.75	V
	V_{REG2}			1.9	-	4.0	V
Power Supply Current At Operating	I_{REG2}	No-load	D_{IN1}=L, D_{IN2}=L, MCK=L	-	0.4	0.8	mA
	I_{REG1}			-	0.1	0.2	
Off-Leakage Current	$I_{REG1OFF}$	V_{DD}=0.5V or lower		-	-	1	μA
Input Voltage	V_{CONT}			0	-	V_{REG2}	V
Input Leakage Current	I_{LK}	V_{CONT}		-	-	±1	μA
Output Voltage	V_{REGO1}	V_{REG2}=2.5V, V_{CONT}=1.0V		1.9	2.0	2.1	V
	V_{REGO2}	V_{REG2}=2.5V, V_{CONT}=0V		-	-	0.1	V
Output Current	I_{OUT}			70	-	-	mA
Output Sink Current	I_{SINK}			60	-	-	mA
V_{REG2}-V_{REGO} Dropout Voltage	ΔV_{IO}			-	-	0.2	V
Ripple Rejection	RR	Vr=0.1Vrms,Iout=70mA fr=1kHz		36	44	-	dB
Load Regulation Voltage	V_{LR}	V_{OUT1}=V_{OUT2}=-6dBm f_{OUT1}=f_{OUT2}=1kHz		-	690	1228	μVrms
V_{REGO} Low Voltage Detection	V_{DET1}			1.1	1.25	1.4	V
	V_{DET2}	Ta=-20 ~+70°C		1.0	1.25	1.5	V
Sleep Detection Voltage	V_{DET3}			0.5	0.75	1.0	V

Note.5) V_{LR} (Load Regulation Voltage) is effective with our measurement PCB only.

The following figure shows a representative example of V_{REGO} versus V_{CONT} at V_{REG2}=2.5V.

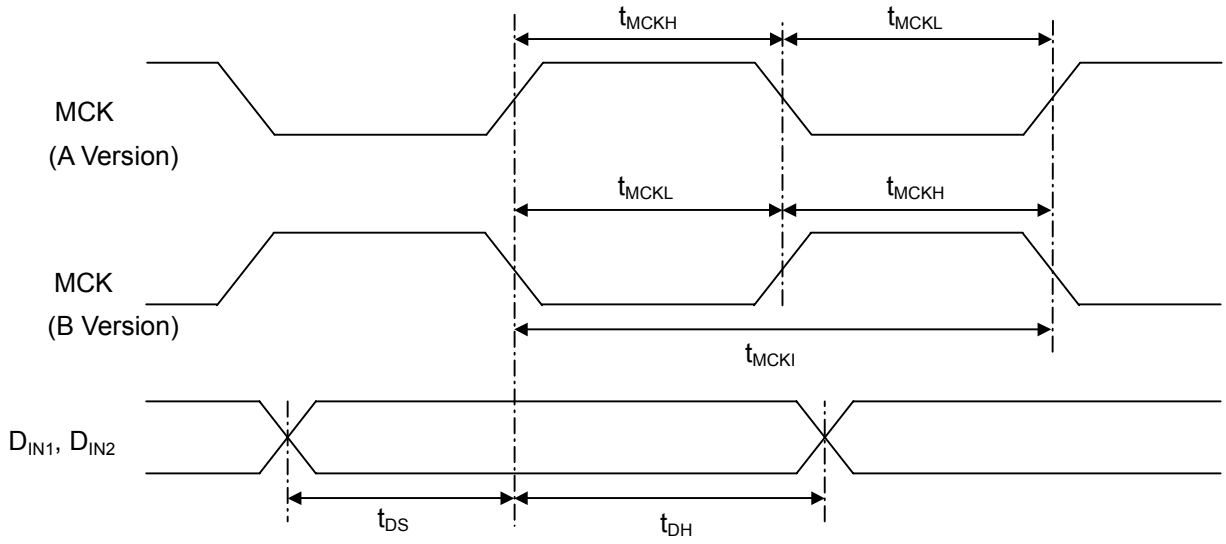


Note.6) Output voltage of V_{REGO} is maximum V_{REG2}.
In V_{DDO1} and V_{DDO2} terminals supplied from V_{REGO}, please set V_{REG2} and V_{CONT} not to exceed their operating voltage.

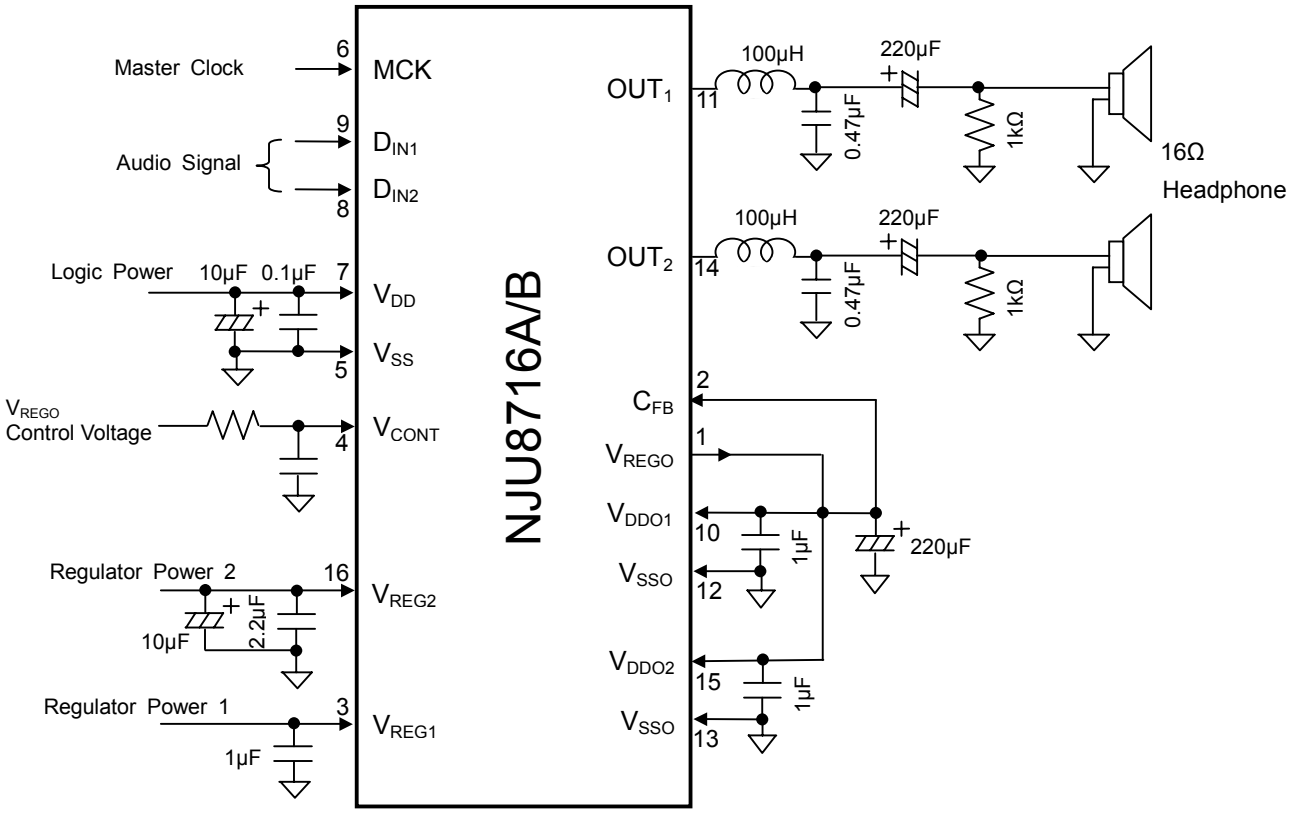
(3) AC CHARACTERISTICS

(Ta=25°C, V_{DD}=2.0V, V_{DDO1}=V_{DDO2}=1.8V, V_{REG2}=2.15V, V_{REG1}=5.0V, V_{SS}=V_{SSO}=0.0V, Load Impedance=16Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
MCK Frequency	f_{MCKI}		8	-	25	MHz
MCK Pulse Width (H)	t_{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		12	-	-	ns
D_{IN1}, D_{IN2} Setup Time	t_{DS}		20	-	-	ns
D_{IN1}, D_{IN2} Hold Time	t_{DH}		20	-	-	ns



■ APPLICATION CIRCUIT



Note.7) De-coupling capacitors must be connected between each power supply pin and GND.
The capacitor value should be adjusted on the application circuit and the temperature. It may malfunction if capacity value is small.

Note.8) A large-capacitance for the de-coupling capacitors for headphone speaker is recommended to improve a low-frequency characteristics. In addition, a low-ESR(Equivalent series resistance) capacitor is recommened for high power efficiency.

Note.9) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carafully to fit your application.