3.3 VOLT CMOS SyncFIFO™ WITH BUS-MATCHING 2,048 x 36, 4,096 x 36, 8,192 x 36, 16,384 x 36, 32,768 x 36, 65,536 x 36

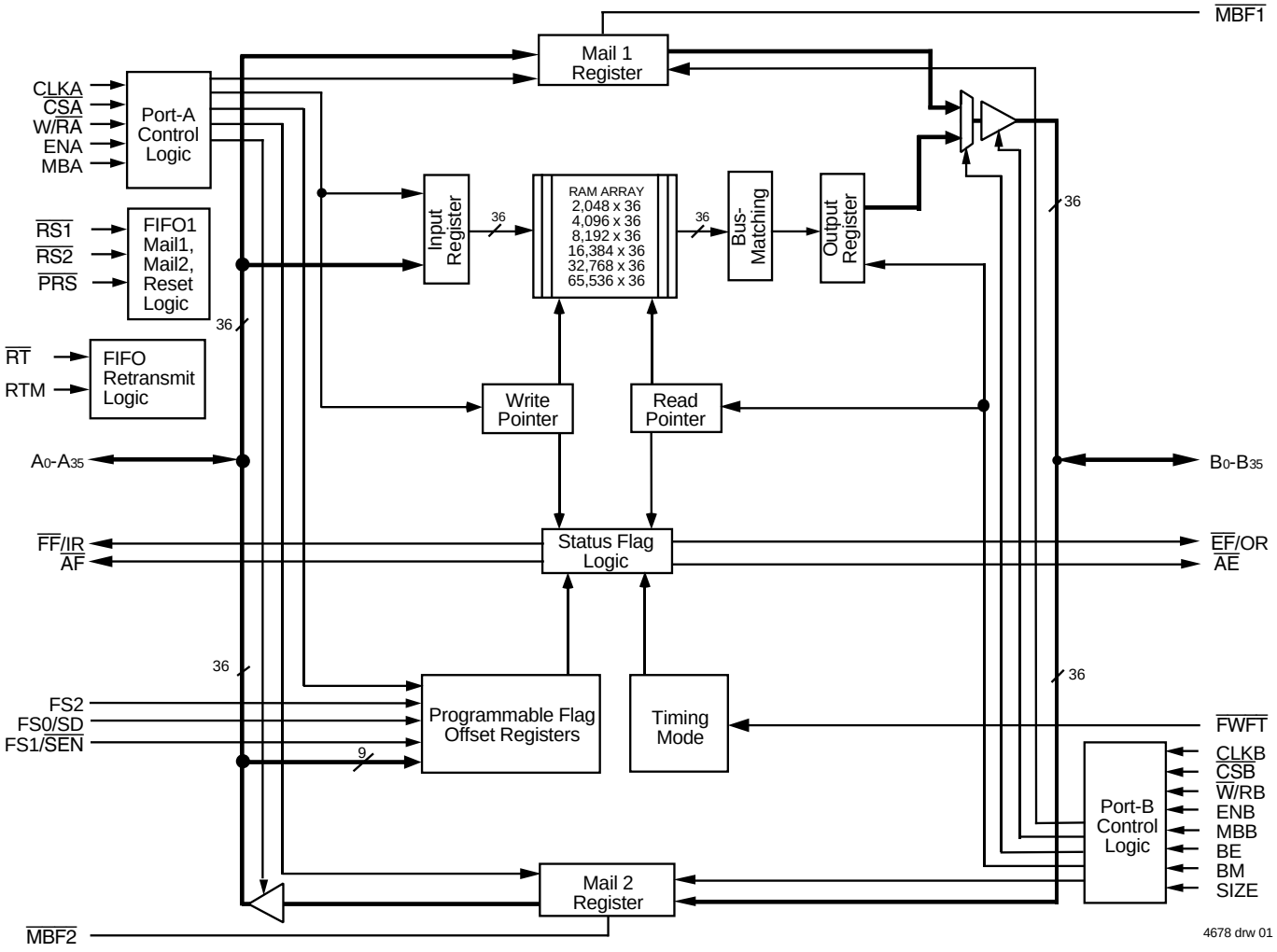
ADVANCE INFORMATION

IDT72V3653
IDT72V3663
IDT72V3673
IDT72V3683
IDT72V3693
IDT72V36103

FEATURES:

- Memory storage capacity:
  - IDT72V3653–2,048 x 36
  - IDT72V3663–4,096 x 36
  - IDT72V3673–8,192 x 36
  - IDT72V3683–16,384 x 36
  - IDT72V3693–32,768 x 36
  - IDT72V36103–65,536 x 36
- Clock frequencies up to 100 MHz (6.5 ns access time)
- Clocked FIFO buffering data from Port A to Port B
- IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$) or First Word Fall Through Timing (using OR and IR flag functions)
- Programmable Almost-Empty and Almost-Full flags; each has five default offsets (8, 16, 64, 256 and 1,024)
- Serial or parallel programming of partial flags
- Port B bus sizing of 36 bits (long word), 18 bits (word) and 9 bits (byte)
- Big- or Little-Endian format for word and byte bus sizes
- Retransmit Capability
- Reset clears data and configures FIFO, Partial Reset clears data but retains configuration settings
- Mailbox bypass registers for each FIFO
- Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Easily expandable in width and depth
- Auto power down minimizes power dissipation
- Available in a space-saving 128-pin Thin Quad Flatpack (TQFP)
- Pin and functionally compatible versions of the 5V operating IDT723653/723663/723673
- Pin compatible with the lower density parts, IDT72V3623/72V3633/72V3643
- Industrial temperature range (–40°C to +85°C) is available

FUNCTIONAL BLOCK DIAGRAM



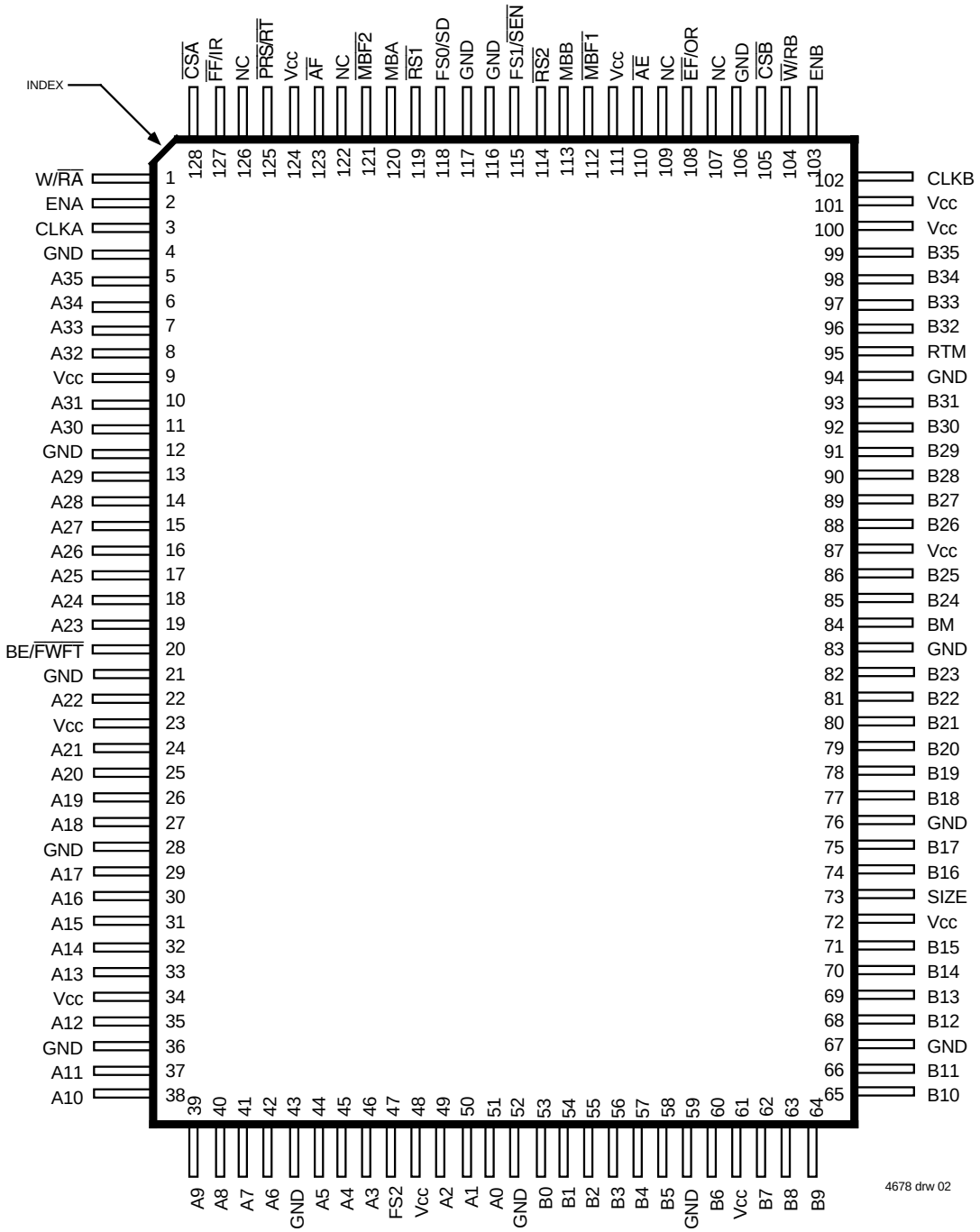
July 1999

DESCRIPTION:

The IDT72V3653/72V3663/72V3673/72V3683/72V3693/72V36103 are pin and functionally compatible versions of the IDT723653/723663/723673, designed to run off a 3.3V supply for exceptionally low power consumption. These devices are monolithic, high-speed, low-power, CMOS unidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 100 MHz and has read access times as fast as 6.5 ns. The 2,048/4,096/8,192/16,384/32,768/65,536 x 36 dual-port SRAM FIFO buffers data from Port A to Port B. FIFO data on Port B can output in 36-bit, 18-bit, or 9-bit formats with a choice of Big- or Little-Endian configurations.

These devices are synchronous (clocked) FIFOs, meaning each port employs a synchronous interface. All data transfers through a port are gated

PIN CONFIGURATION



TQFP (PK128-1, order code: PF)
TOP VIEW

to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFO via two mailbox registers. The mailbox registers' width matches the selected Port B bus width. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on these FIFOs: Reset and Partial Reset. Reset initializes the read and write pointers to the first location of the memory array and selects serial flag programming, parallel flag programming, or one of five possible default flag offset settings, 8, 16, 64, 256 or 1,024.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings.

The FIFO has Retransmit capability, a Retransmit is performed after four clock cycles of CLKA and CLKB, by takingthe Retransmit pin, $\overline{RT}$ LOW while the Retransmit Mode pin, $\overline{RTM}$ is HIGH. When a Retransmit is performed the read pointer is reset to the first memory location.

These devices have two modes of operation: In the *IDT Standard mode*, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the *First Word Fall Through mode* (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required (Nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/$\overline{FWFT}$ pin during Reset determines the mode in use.

The FIFO has a combined Empty/Output Ready Flag ($\overline{EF}$/OR) and a combined Full/Input Ready Flag ($\overline{FF}$/IR). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether the memory is full or not. The IR and OR functions are selected in the First Word Fall Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

The FIFO has a programmable Almost-Empty flag ($\overline{AE}$) and a programmable Almost-Full flag ($\overline{AF}$). $\overline{AE}$ indicates when a selected number of words remain in the FIFO memory. $\overline{AF}$ indicates when the FIFO contains more than a selected number of words.

$\overline{FF}$/IR and $\overline{AF}$ are two-stage synchronized to the port clock that writes data into its array. $\overline{EF}$/OR and $\overline{AE}$ are two-stage synchronized to the port clock that reads data from its array. Programmable offsets for $\overline{AE}$ and $\overline{AF}$ are loaded in parallel using Port A or in serial via the SD input. Five default offset settings are also provided. The $\overline{AE}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the empty boundary and the $\overline{AF}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the full boundary. All these choices are made using the FS0, FS1 and FS2 inputs during Reset.

Interspersed Parity is available and can be selected during a Master Reset of the FIFO. If Interspersed Parity is selected then during parallel programming of the flag offset values, the device will ignore data lines A8, A17, A26 and A35. If Non-Interspersed Parity is selected then data lines A32, A33, A34 and A35 will be ignored, (A8, A17 and A26 will become valid bits).

Two or more devices may be used in parallel to create wider data paths. In First Word Fall Through mode, more than one device may be connected in series to create greater word depths. The addition of external components is unnecessary.

If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72V3653/72V3663/72V3673/72V3683/72V3693/72V36103 are characterized for operation from 0°C to 70°C. Industrial temperature range (-40°C to +85°C) is available by special order. They are fabricated using IDT's high speed, submicron CMOS technology.

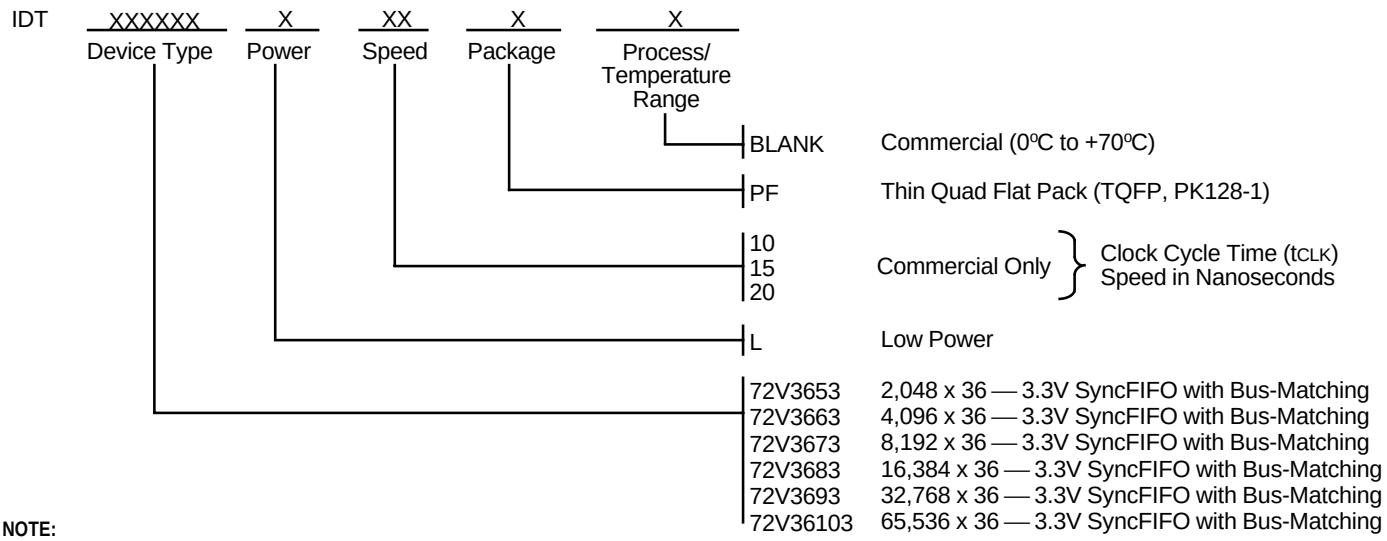
PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag (Port B)	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the Almost-Empty B offset register, X.
$\overline{AF}$	Almost-Full Flag (Port A)	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Almost-Full A offset register, Y.
B0-B35	Port B Data	I/O	36-bit bidirectional data port for side B.
BE/$\overline{FWFT}$	Big-Endian/ First Word Fall Through	I	This is a dual purpose pin. During Master Reset, a HIGH on BE will select Big-Endian operation. In this case, depending on the bus size, the most significant byte or word written to Port A is read from Port B first. A LOW on BE will select Little-Endian operation. In this case, the least significant byte or word written to Port A is read from Port B first. After Master Reset, this pin selects the timing mode. A HIGH on $\overline{FWFT}$ selects IDT Standard mode, a LOW selects First Word Fall Through mode. Once the timing mode has been selected, the level on $\overline{FWFT}$ must be static throughout device operation.
BM	Bus-Match Select (Port B)	I	A HIGH on this pin enables either byte or word bus width on Port B, depending on the state of SIZE. A LOW selects long word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. $\overline{FF}$/IR and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. $\overline{EF}$/OR and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on Port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$/OR	Empty/Output Ready Flag (Port B)	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In the FWFT mode, the OR function is selected. OR indicates the presence of valid data on the B0-B35 outputs, available for reading. $\overline{EF}$/OR is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B.
$\overline{FF}$/IR	Full/Input Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the IR function is selected. IR (Port A) indicates whether or not there is space available for writing to the FIFO memory. $\overline{FF}$/IR is synchronized to the LOW-to-HIGH transition of CLKA.
FS0/SD FS1/$\overline{SEN}$ FS2	Flag Offset Select 0/ Serial Data, Flag Offset Select 1/ Serial Enable Flag Offset Select 2	I I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During Reset, FS1/$\overline{SEN}$ and FS0/SD, together with FS2, select the flag offset programming method. Three offset register programming methods are available: automatically load one of five preset values (8, 16, 64, 256 or 1,024), parallel load from Port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on 2 CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 22 for the 72V3653, 24 for the 72V3663, 26 for the 72V3673, 28 for the 72V3683, 30 for the 72V3693 and, 32 for the 72V36103. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.

PIN DESCRIPTIONS (Continued)

Symbol	Name	I/O	Description
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a Port A read or write operation.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a Port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Reset ($\overline{RS1}$) or Partial Reset ($\overline{PRS}$).
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Reset ($\overline{RS2}$) or Partial Reset ($\overline{PRS}$).
$\overline{RS1}$, $\overline{RS2}$	Resets	I	A LOW on both pins initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW-to-HIGH transition on $\overline{RS1}$ selects the programming method (serial or parallel) and one of five programmable flag default offsets. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RS1}$ is LOW.
$\overline{PRS}$/ $\overline{RT}$	Partial Reset/ Retransmit	I	This pin muxed for both Partial Reset and Retransmit operations, it is used in conjunction with the RTM pin. If RTM is LOW, then a LOW on this pin initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained. If RTM is HIGH, then a LOW on this pin performs a Retransmit and initializes the read pointer only, to the first memory location.
RTM	Retransmit Mode	I	This pin is used in conjunction with the $\overline{RT}$ pin. When RTM is HIGH a Retransmit is performed when $\overline{RT}$ is taken HIGH.
SIZE	Bus Size Select (Port B)	I	A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation.
$\overline{W}$/RA	Port A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on Port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the HIGH impedance state when $\overline{W}$/RB is LOW.

ORDERING INFORMATION



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NOTE:

1. Industrial temperature range is available by special order.

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