# CY27C256A

# 32K x 8 CMOS EPROM

## Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— $t_{AA}$ = 70 ns max.**
- **Low power**
  - **— 220 mW max.**
  - **— Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in the windowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **— 32-pin PLCC**
  - **— 28-pin TSOP-I**
  - **— 28-pin, 600-mil plastic or hermetic DIP**
  - **— 32-pin hermetic LCC**

## Functional Description

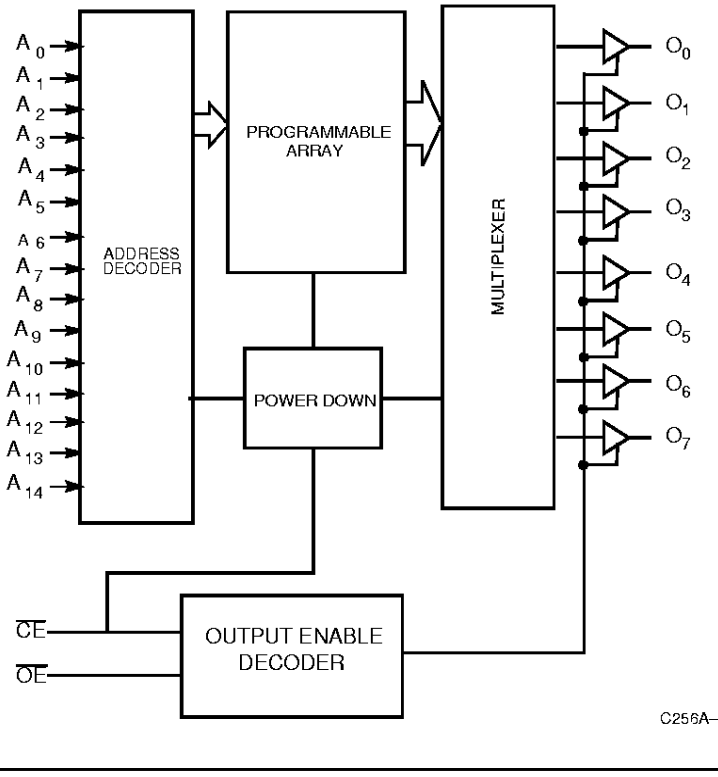
The CY27C256A is a high–performance, 256K CMOS EPROM organized in 32 Kbytes. It is available in industry–standard 28–pin, 600–mil DIP, 32–pin LCC and PLCC, and 28–pin TSOP–I packages. The CY27C256A is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C256A is equipped with a power–down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low–power stand–by mode. The $\overline{OE}$ pin three–states the outputs without putting the device into stand–by mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three–stated outputs.

The memory cells utilize proven EPROM floating–gate technology and byte–wide intelligent programming algorithms. The EPROM cell requires only 12.75V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

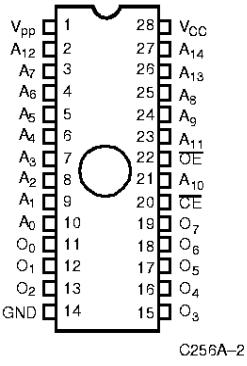
The CY27C256A is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{14}$–$A_0$ will appear at the outputs

### Logic Block Diagram

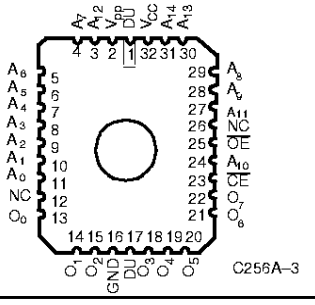



### Pin Configurations

DIP
Top View




LCC/PLCC [1]
Top View

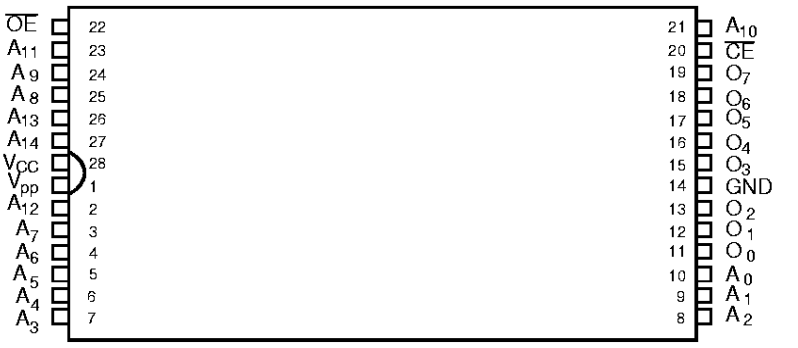



**Notes:**

1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

## Pin Configurations (continued)

TSOP
Top View
Type 1




C256A–4

## Selection Guide

| | | 27C256A–70 | 27C256A–90 | 27C256A–120 | 27C256A–150 | 27C256A–200 |
|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 70 | 90 | 120 | 150 | 200 |
| $\overline{CE}$ Access Time (ns) | | 70 | 90 | 120 | 150 | 200 |
| $\overline{OE}$ Access Time (ns) | | 25 | 30 | 40 | 50 | 60 |
| $I_{CC}$[2] (mA) Power Supply Current | Com'l | 50 | 50 | 50 | 50 | 50 |
| | Mil | 60 | 60 | 60 | 60 | 60 |
| $I_{SB}$[3] (mA) Stand–by Current | Com'l | 15 | 15 | 15 | 15 | 15 |
| | Mil | 25 | 25 | 25 | 25 | 25 |

**Notes:**
2. $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f=5 MHz.
3. $V_{CC}$ = Max., $\overline{CE}$ = $V_{IH}$.

## Maximum Ratings

(Above which the useful life may be impaired. For user guide–lines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +5.5V

DC Input Voltage ..... –3.0V to +7.0V

Transient Input Voltage ..... –3.0V for <20 ns

DC Program Voltage ..... 13.0V

UV Erasure ..... 7258 Wsec/cm$^2$

Static Discharge Voltage ..... >2001V (per MIL–STD–883, Method 3015)

Latch–Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial[4] | –40°C to +85°C | 5V ± 10% |
| Military[5] | –55°C to +125°C | 5V ± 10% |

**Notes:**
4. Contact a Cypress representative for industrial temperature range spec–ification.
5. $T_A$ is the "instant on" case temperature.

## Electrical Characteristics Over the Operating Range[6, 7]

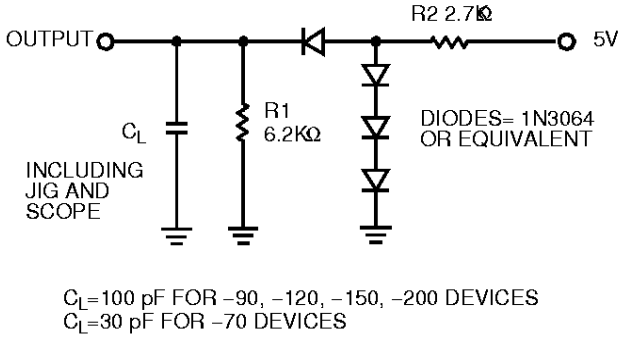
| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −400 µA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 2.1 mA | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs | | 2.0 | $V_{CC}$+0.5 | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs | | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | −10 | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output Disable | | −10 | +10 | µA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$=Max., $I_{OUT}$=0 mA, f=5 MHz | Com'l | | 50 | mA |
| | | | Mil | | 60 | mA |
| $I_{SB}$ | Stand−By Current | $V_{CC}$=Max., $\overline{CE}$ = $V_{IH}$ | Com'l | | 15 | mA |
| | | | Mil | | 25 | mA |

## Capacitance[7]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

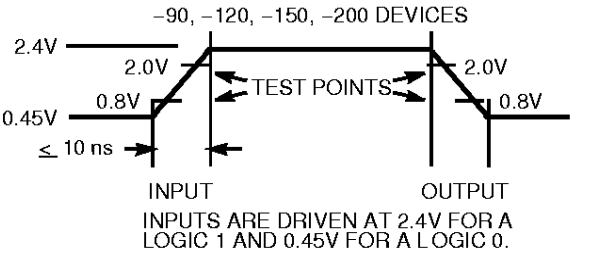
**Notes:**
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

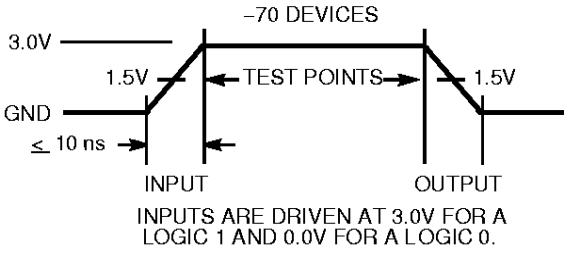
## AC Test Loads and Waveforms




$C_L$=100 pF FOR −90, −120, −150, −200 DEVICES
$C_L$=30 pF FOR −70 DEVICES

C256A−5



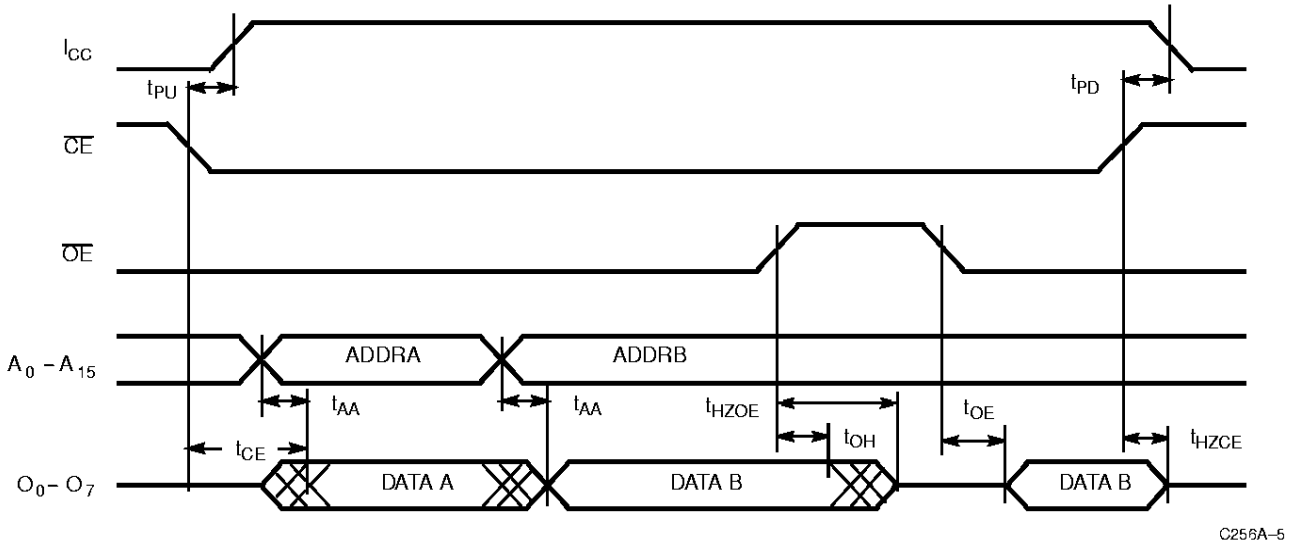




C256A−6

**Switching Characteristics** Over the Operating Range

| Parameter | Description | 27C256A-70 | | 27C256A-90 | | 27C256A-120 | | 27C256A-150 | | 27C256A-200 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{AA}$ | Address to Output Valid | | 70 | | 90 | | 120 | | 150 | | 200 | ns |
| $t_{OE}$ | $\overline{OE}$ Active to Output Valid | | 25 | | 30 | | 35 | | 40 | | 60 | ns |
| $t_{HZOE}$ | $\overline{OE}$ Inactive to High Z | | 25 | | 30 | | 35 | | 40 | | 60 | ns |
| $t_{CE}$ | $\overline{CE}$ Active to Output Valid | | 70 | | 90 | | 120 | | 150 | | 200 | ns |
| $t_{HZCE}$ | $\overline{CE}$ Inactive to High Z | | 25 | | 30 | | 30 | | 30 | | 30 | ns |
| $t_{PU}$ | $\overline{CE}$ Active to Power–Up | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ Inactive to Power–Down | | 60 | | 65 | | 65 | | 65 | | 65 | ns |
| $t_{OH}$ | Output Data Hold | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

**Switching Waveform**




## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C256A in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm$^2$ power rating, the exposure time would be approximately 35 minutes. The CY27C256A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high–intensity UV light for an extended period of time. 7258 Wsec/cm$^2$ is the recommended maximum dosage.

## Programming Modes

Programming support is available from Cypress as well as from a number of third–party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

**Table 1. Programming Electrical Characteristics.**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{PP}$ | Programming Power Supply | 12.5 | 13 | V |
| $I_{PP}$ | Programming Supply Current | | 50 | mA |
| $V_{IHP}$ | Programming Input Voltage HIGH | 3.0 | $V_{CC}$ | V |
| $V_{ILP}$ | Programming Input Voltage LOW | –0.5 | 0.4 | V |
| $V_{CCP}$ | Programming $V_{CC}$ | 6.0 | 6.5 | V |

**Table 2. Mode Selection Table.**

| Mode | Pin Function[8] | | | | | |
|---|---|---|---|---|---|---|
| | CE | OE | $V_{PP}$ | $A_0$ | $A_9$ | Data |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $A_0$ | $A_9$ | $O_7 - O_0$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $A_0$ | $A_9$ | High Z |
| Stand–by | $V_{IH}$ | X | $V_{IH}$ | X | X | High Z |
| Program | $V_{ILP}$ | $V_{IHP}$ | $V_{PP}$ | $A_0$ | $A_9$ | $D_7 - D_0$ |
| Program Verify | $V_{IHP}$ | $V_{ILP}$ | $V_{PP}$ | $A_0$ | $A_9$ | $O_7 - O_0$ |
| Program Inhibit | $V_{IHP}$ | $V_{IHP}$ | $V_{PP}$ | $A_0$ | $A_9$ | High Z |
| Signature Read (MFG) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{HV}$[9] | 34H |
| Signature Read (DEV) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{HV}$[9] | 21H |

**Notes:**
8. X can be $V_{IL}$ or $V_{IH}$.
9. $V_{HV}$=12±0.5V

## Ordering Information[10]

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 70 | CY27C256A–70JC | J65 | 32–Lead Plastic Leaded Chip Carrier | Commercial |
| | CY27C256A–70PC | P15 | 28–Lead (600–Mil) Molded DIP | |
| | CY27C256A–70WC | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| | CY27C256A–70ZC | Z28 | 28–Lead Thin Small Outline Package | |
| | CY27C256A–70QMB | Q55 | 32–Pin Windowed Rectangular Leadless Chip Carrier | Military |
| | CY27C256A–70WMB | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| 90 | CY27C256A–90JC | J65 | 32–Lead Plastic Leaded Chip Carrier | Commercial |
| | CY27C256A–90PC | P15 | 28–Lead (600–Mil) Molded DIP | |
| | CY27C256A–90WC | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| | CY27C256A–90ZC | Z28 | 28–Lead Thin Small Outline Package | |
| | CY27C256A–90QMB | Q55 | 32–Pin Windowed Rectangular Leadless Chip Carrier | Military |
| | CY27C256A–90WMB | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| 120 | CY27C256A–120JC | J65 | 32–Lead Plastic Leaded Chip Carrier | Commercial |
| | CY27C256A–120PC | P15 | 28–Lead (600–Mil) Molded DIP | |
| | CY27C256A–120WC | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| | CY27C256A–120ZC | Z28 | 28–Lead Thin Small Outline Package | |
| | CY27C256A–120QMB | Q55 | 32–Pin Windowed Rectangular Leadless Chip Carrier | Military |
| | CY27C256A–120WMB | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| 150 | CY27C256A–150JC | J65 | 32–Lead Plastic Leaded Chip Carrier | Commercial |
| | CY27C256A–150PC | P15 | 28–Lead (600–Mil) Molded DIP | |
| | CY27C256A–150WC | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| | CY27C256A–150ZC | Z28 | 28–Lead Thin Small Outline Package | |
| | CY27C256A–150QMB | Q55 | 32–Pin Windowed Rectangular Leadless Chip Carrier | Military |
| | CY27C256A–150WMB | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| 200 | CY27C256A–200JC | J65 | 32–Lead Plastic Leaded Chip Carrier | Commercial |
| | CY27C256A–200PC | P15 | 28–Lead (600–Mil) Molded DIP | |
| | CY27C256A–200WC | W16 | 28–Lead (600–Mil) Windowed CerDIP | |
| | CY27C256A–200ZC | Z28 | 28–Lead Thin Small Outline Package | |
| | CY27C256A–200QMB | Q55 | 32–Pin Windowed Rectangular Leadless Chip Carrier | Military |
| | CY27C256A–200WMB | W16 | 28–Lead (600–Mil) Windowed CerDIP | |

**Notes:**

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

## MILITARY SPECIFICATIONS
### Group A Subgroup Testing

#### DC Characteristics

| Parameter | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |
| $I_{SB}$ | 1, 2, 3 |

#### Switching Characteristics

| Parameter | Subgroups |
|---|---|
| $t_{AA}$ | 7, 8, 9, 10, 11 |
| $t_{OE}$ | 7, 8, 9, 10, 11 |
| $t_{CE}$ | 7, 8, 9, 10, 11 |

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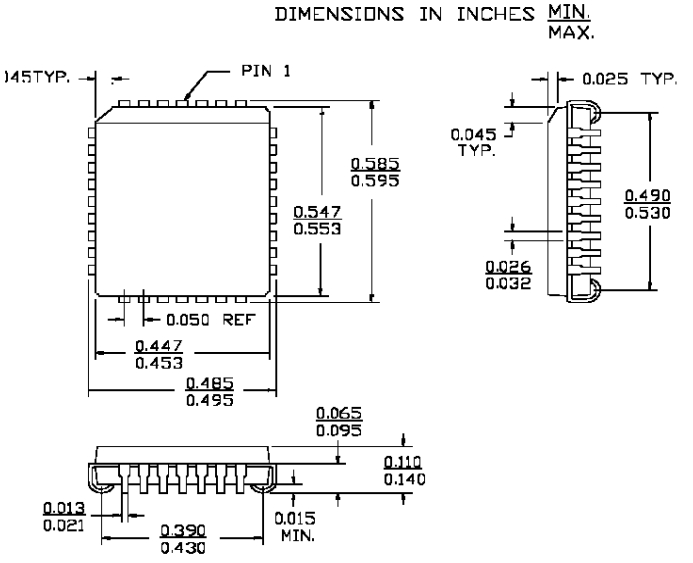
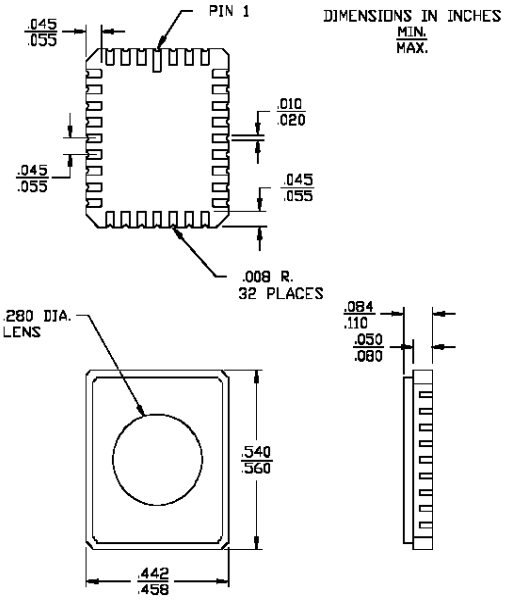
## Package Diagrams

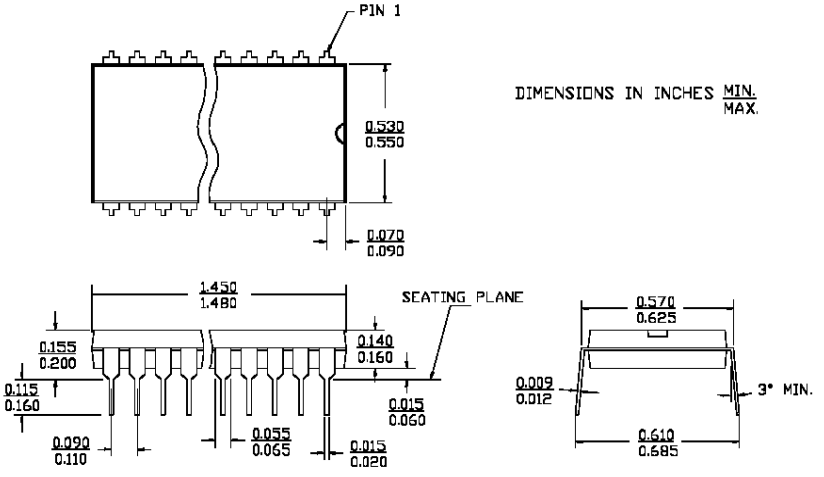
**32-Lead Plastic Leaded Chip Carrier J65**




**32-Rn Windowed Rectangular Leadless Chip Carrier Q55**
MIL-STD-1835 C-12

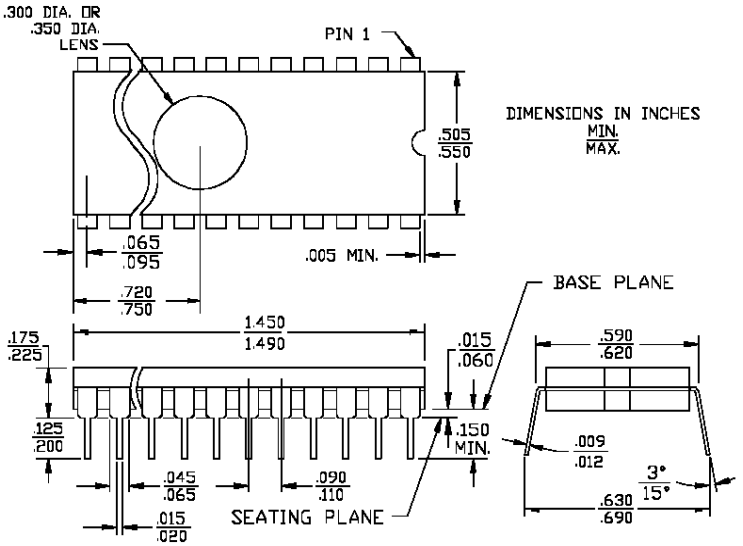



**28-Lead (600-Mil)Molded DIP P15**



## Package Diagrams (Continued)

**28-Lead (600-Mil)Windowed CerDIP W16**
MIL-STD-1835 D-10 Config.A




**28-Lead Thin Small Outline Package Z28**