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MOS FIELD EFFECT TRANSISTOR 2SK3377

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3377 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Low On-state Resistance

 $R_{DS(on)1} = 44 \text{ m}\Omega \text{ MAX}. \text{ (V}_{GS} = 10 \text{ V}, I_D = 10 \text{ A})$ $R_{DS(on)2} = 78 \text{ m}\Omega \text{ MAX.} (V_{GS} = 4.0 \text{ V}, I_D = 10 \text{ A})$

- Low Ciss: Ciss = 760 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3377	TO-251 (MP-3)		
2SK3377-Z	TO-252 (MP-3Z)		

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	Voss	60	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	ID(DC)	±20	Α
Drain Current (Pulse) Note1	ID(pulse)	±50	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	30	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note2	las	15	Α
Single Avalanche Energy Note2	Eas	23	mJ

(TO-251)





Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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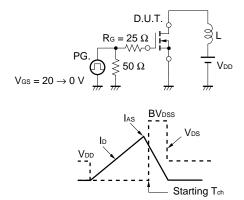
The mark <R> shows major revised points.

ELECTRICAL CHARACTERISTICS (TA = 25°C)

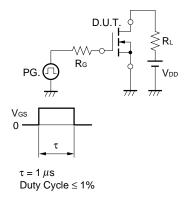
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	٧
Forward Transfer Admittance Note	y fs	V _{DS} = 10 V, I _D = 10 A	5	10		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 10 A		35	44	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 10 A		54	78	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		760		pF
Output Capacitance	Coss	V _{GS} = 0 V		150		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		71		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 10 A		13		ns
Rise Time	tr	V _{GS} = 10 V		170		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		43		ns
Fall Time	tf			34		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		17		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		3.0		nC
Gate to Drain Charge	Q _{GD}	I _D = 20 A		4.7		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 20 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	I _F = 20 A, V _{GS} = 0 V		39		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		62		nC

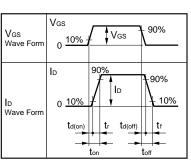
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



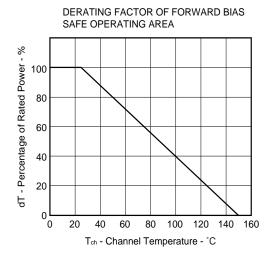
TEST CIRCUIT 2 SWITCHING TIME

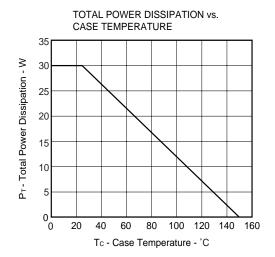




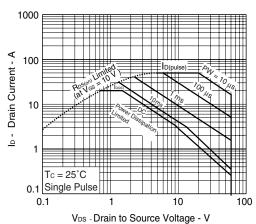
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

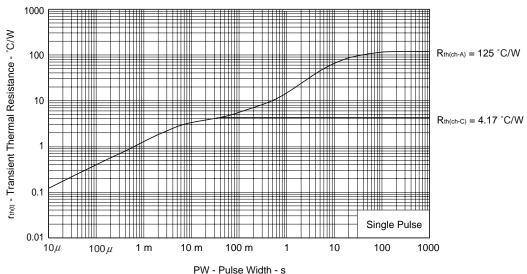




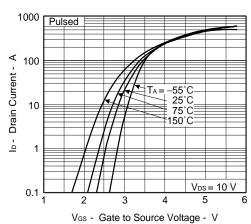
FORWARD BIAS SAFE OPERATING AREA



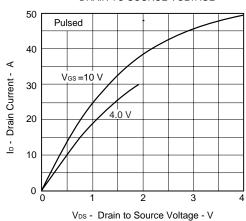
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



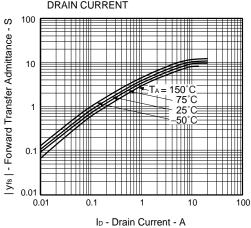
FORWARD TRANSFER CHARACTERISTICS



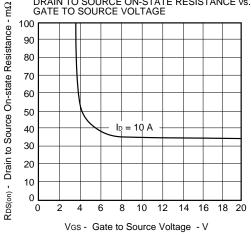
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



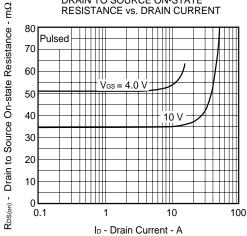
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



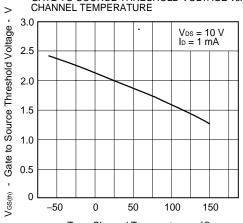
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



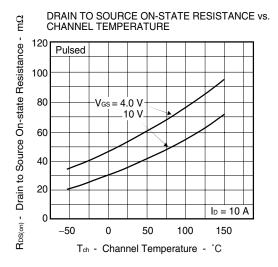
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

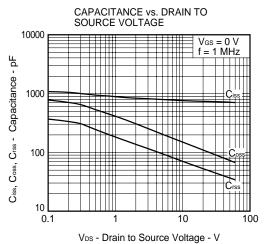


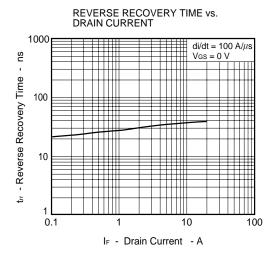
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

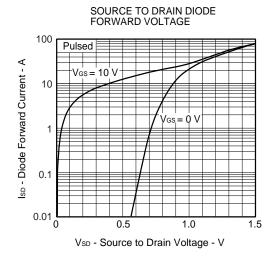


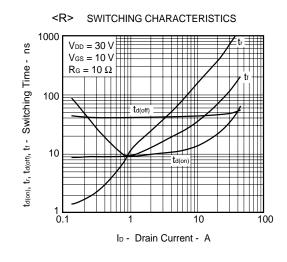
 T_{ch} - Channel Temperature - $^{\circ}\text{C}$

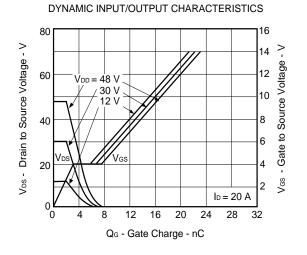


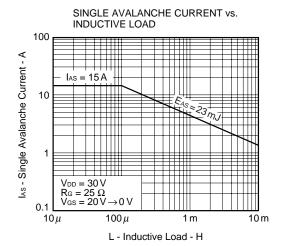


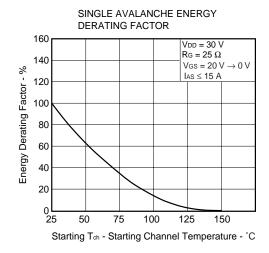






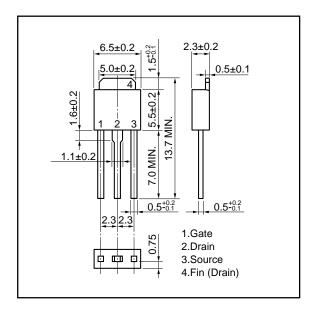




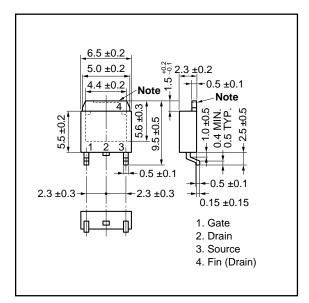


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

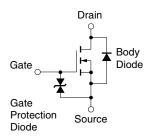


2) TO-252 (MP-3Z)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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