HI-8383

ARINC 429 DIFFERENTIAL LINE DRIVER

General Description

The HI-8383 bus interface device is a silicon gate CMOS device designed as a line driver in accordance with the ARINC 429 bus specifications.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-8383 to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

The differential outputs of the HI-8383 are independently programmable to the ARINC 429 output rise and fall time specifications, for both high speed and low speed applications, through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the V_{REF} input. No on-chip overvoltage and short-circuit protection of the differential outputs is provided on this device. If required the HI-8382 is recommended.

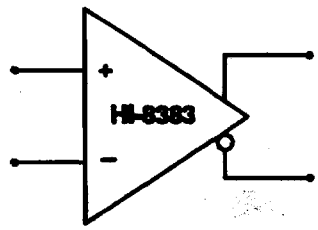
The HI-8383 is intended for use with either of two companion CMOS devices, the HI-8282 ARINC 429 Serial Transmitter/Dual Receiver, or the HI-8482 ARINC 429 Dual Line Receiver. These devices provide the necessary data formatting between the system processor bus and the ARINC 429 protocol. All three products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information, including HI-8282 and HI-8482 data sheets.

Features

- Low Power CMOS
- TTL and CMOS Compatible Inputs
- Programmable Output Voltage Swing
- Adjustable ARINC Rise and Fall Times
- Operates at Data Rates Up to 100 Kbits
- Allows External Output Protection
- Full Military Temperature Range

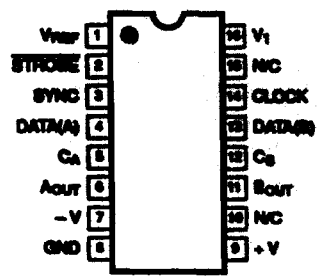
Chip Topography

Function

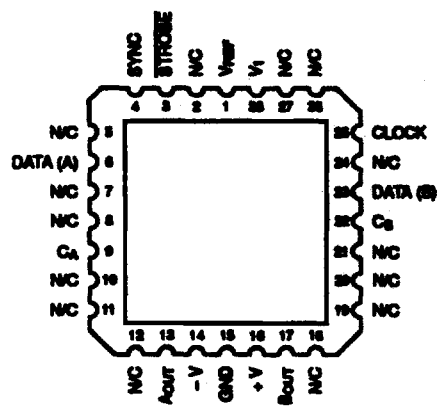


ARINC 429 DIFFERENTIAL LINE DRIVER

Pin Configurations



16 PIN DIP
(TOP VIEW)



28 PIN CHIP CARRIERS (LCC & PLCC)
(TOP VIEW)

HOLT INC.
INTEGRATED CIRCUITS

Functional Description

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input. This built in feature allows the HI-8383 to be used in applications not requiring the HI-8282 companion circuit. Each logic input, including the power enable ($\overline{\text{STROBE}}$) input, are TTL/CMOS compatible.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-8383: + 15V, – 15V and + 5V. The + 5V supply powers the internal bus current regulator and also provides a reference voltage that determines the output voltage swing. The differential output voltage swing will equal $2V_{REF}$. If a value of V_{REF} other than + 5V is needed, a separate + 5V power supply is required for pin V_1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, A_{OUT} will switch to the $+V_{REF}$ rail and B_{OUT} will switch to the $-V_{REF}$ rail (a logic high state). Reversing the data input states will cause A_{OUT} to switch to the $-V_{REF}$ rail and B_{OUT} to switch to the $+V_{REF}$ rail (a logic low state). With both data input signals at a logic low state, the outputs will both switch to 0V (null state).

The driver output impedance is nominally 36 Ohms (See Figure 2). The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the C_A and C_B input pins. For high-speed operation (100KBPS), the values are typically $C_A = C_B = 75$ pF, while $C_A = C_B = 500$ pF is typical for low-speed operation (12.5 to 14KBPS).

The HI-8383 outputs have no Zener diodes for overvoltage protection nor fuses for short circuit protection and therefore should be used only when external protection requirements can not be easily implemented with the HI-8382 device.

The driver can be externally powered down by applying a logic high to the $\overline{\text{STROBE}}$ input pin. If this feature is not being used, the pin should be tied to ground.

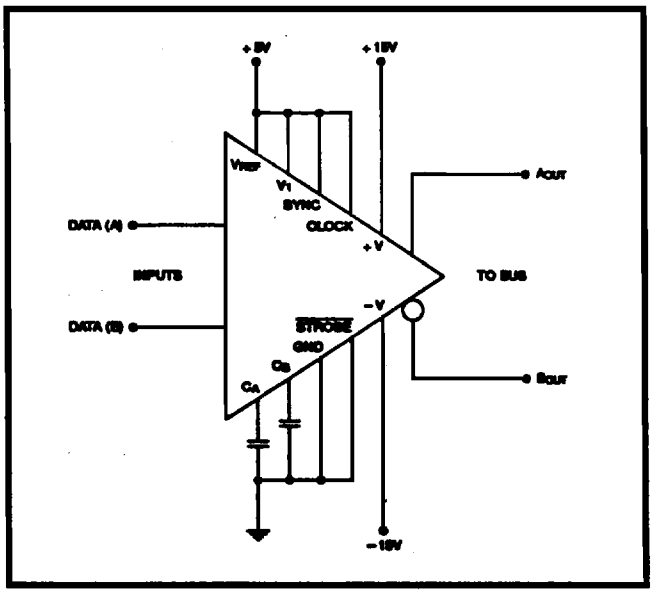


FIGURE 1. ARINC 429 BUS APPLICATION

Truth Table

SYNC	CLOCK	DATA(A)	DATA(B)	A_{OUT}	B_{OUT}	COMMENTS
X	L	X	X	0V	0V	NULL
L	X	X	X	0V	0V	NULL
H	H	L	L	0V	0V	NULL
H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOW
H	H	H	L	$+V_{REF}$	$-V_{REF}$	HIGH
H	H	H	H	0V	0V	NULL

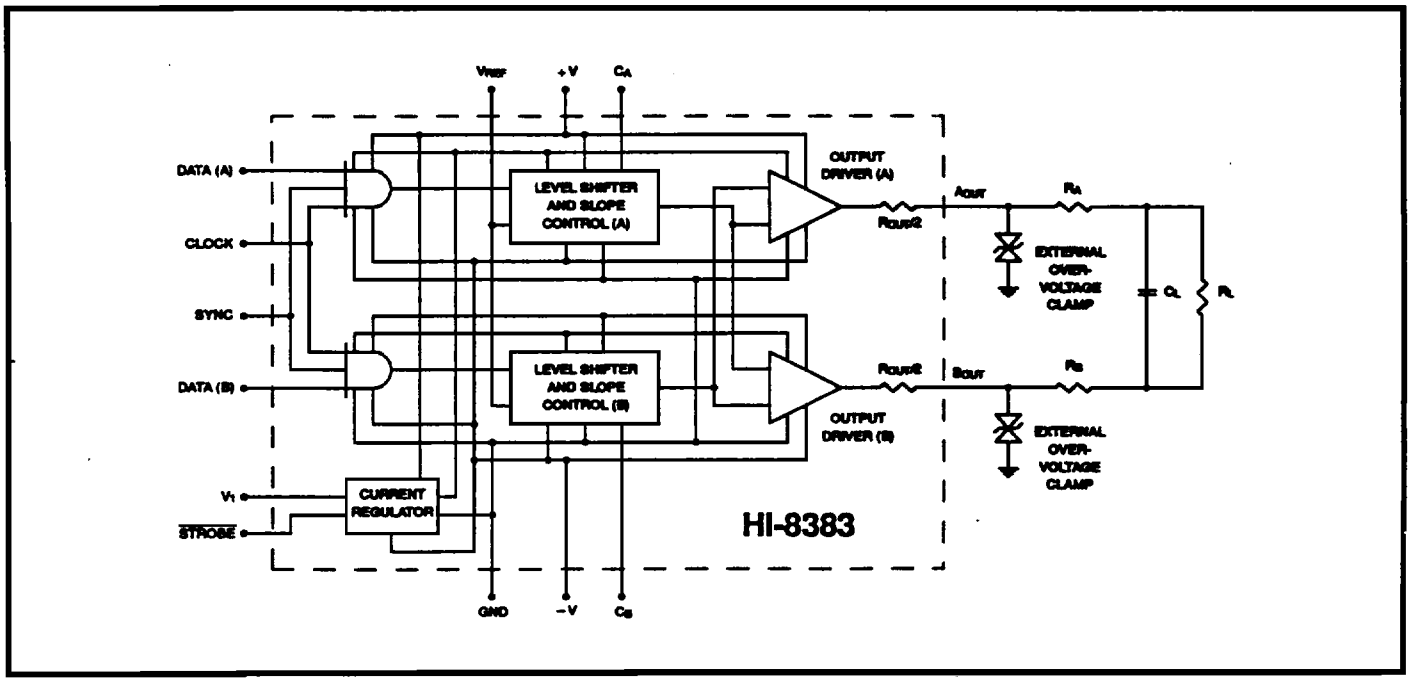


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Pin Descriptions

SYMBOL	FUNCTION	DESCRIPTION
V_{REF}	POWER	THE REFERENCE VOLTAGE USED TO DETERMINE THE OUTPUT VOLTAGE SWING.
STROBE	INPUT	A LOGIC HIGH ON THIS INPUT PLACES THE DRIVER IN POWER DOWN MODE.
SYNC	INPUT	SYNCHRONIZES DATA INPUTS.
DATA (A)	INPUT	DATA INPUT TERMINAL A.
C_A	INPUT	CONNECTION FOR DATA (A) SLEW-RATE
A_{OUT}	OUTPUT	ARINC OUTPUT TERMINAL A.

SYMBOL	FUNCTION	DESCRIPTION
-V	POWER	-15v ± 10%
GND	POWER	0.0V
+V	POWER	+15V ± 10%
B_{OUT}	OUTPUT	ARINC OUTPUT TERMINAL B.
C_B	INPUT	CONNECTION FOR DATA (B) SLEW-RATE CAPACITOR.
DATA (B)	INPUT	DATA INPUT TERMINAL B.
CLOCK	INPUT	SYNCHRONIZES DATA INPUTS
V_L	POWER	5V ± 5%

Absolute Maximum Ratings

V_{DD} = +15V dc ±10%, All Voltages Referenced to GND

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	V_{DIF}	Voltage Between +V and -V terminals		40	V
Supply Voltages	+V		+10.8 to +16.5		V
	-V		-10.8 to -16.5		V
	V_L		+5 ±10%	+7	V
Voltage Reference	V_{REF}	For ARINC 429 For Applications Other Than ARINC	+5 ±5% 0 to 6	6 6	V V
Input Voltage Range	V_{IN}			≥ GND -0.3 ≤ V_L +0.3	V V
Output Short-Circuit Duration		See NOTE: 1			
Output Overvoltage Protection		See NOTE: 2			
Operating Temperature Range	T_A	16 PIN DIP & 28 PIN LCC 28 PIN PLCC	-55 to +125 -40 to +85		°C °C
Storage Temperature Range	T_{STG}	Soldering, 10 seconds	-65 to +150	+275	°C
Lead Temperature					°C
Junction Temperature	T_J			+175	°C
Power Dissipation @ +25°C	P_D	16 PIN DIP See NOTE: 3 28 PIN LCC See NOTE: 3 28 PIN PLCC See NOTE: 3		1.725 1.120 2.143	W W W
Thermal Resistance, Junction - to - Ambient	$\varnothing_{JA}$	16 PIN DIP 28 PIN LCC 28 PIN PLCC		86.5 133.7 70.0	°C/W °C/W °C/W

NOTE 1 – Heatsinking may be required for Output Short Circuit at +125°C and for 100KBPS at +125°C.

NOTE 2 – Use the HI-8382 if Output Overvoltage Protection and/or Short Circuit Pass Protection is required.

NOTE 3 – Derate above +25°C, 11.5 mW/°C for 16 PIN DIP, 7.5mW/°C for 28 PIN LCC and 14.2mW/°C for 28 PIN LCC.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Current +V (Operating)	I_{CCOP} (+V)	No Load (0 – 100KBPS)			+11	mA
Supply Current –V (Operating)	I_{CCOP} (–V)	No Load (0 – 100KBPS)			–11	mA
Supply Current V_1 (Operating)	I_{CCOP} (V_1)	No Load (0 – 100KBPS)			500	µA
Supply Current V_{REF} (Operating)	I_{CCOP} (V_{REF})	No Load (0 – 100KBPS)			500	µA
Supply Current +V (Power Down)	I_{CCPD} (+V)	$\overline{STROBE}$ = HIGH	–475		475	µA
Supply Current –V (Power Down)	I_{CCPD} (–V)	$\overline{STROBE}$ = HIGH	–475		475	µA
Supply Current –V (During Short Circuit Test)	I_{SC} (–V)	Short to Ground See NOTE: 1			TBD	mA
Supply Current +V (During Short Circuit Test)	I_{SC} (+V)	Short to Ground See NOTE: 1			TBD	mA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to Ground V_{RIN} = 0 See NOTE: 2	–80			mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to Ground V_{RIN} = 0 See NOTE: 2	+80			mA
Input Current (Input High)	I_{IH}				1.0	µA
Input Current (Input Low)	I_{IL}				1.0	µA
Output Voltage High (Output to Ground)	V_{OH}	No Load (0 – 100KBPS)	$+V_{REF}$ –.25		$+V_{REF}$ +.25	V
Output Voltage Low (Output to Ground)	V_{OL}	No Load (0 – 100KBPS)	$-V_{REF}$ –.25		$-V_{REF}$ +.25	V
Output Voltage Null	V_{NULL}	No Load (0 – 100KBPS)	–250		+250	mV
Input Capacitance	C_{IN}				15	pF
NOTE: 1 Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.						
NOTE: 2 Interchangeability of force and sense is acceptable.						

AC Electrical Characteristics

+V = 15V, –V = –15V, V_1 = V_{REF} = 5.0V, T_A = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Rise Time (A_{OUT}, B_{OUT})	t_R	C_A = C_B = 75pF	1.0		2.0	µs
Fall Time (A_{OUT}, B_{OUT})	t_F	C_A = C_B = 75pF	1.0		2.0	µs
Propagation Delay Input to Output	t_{PLH}	C_A = C_B = 75pF			3.0	µs
Propagation Delay Input to Output	t_{PHL}	C_A = C_B = 75pF			3.0	µs

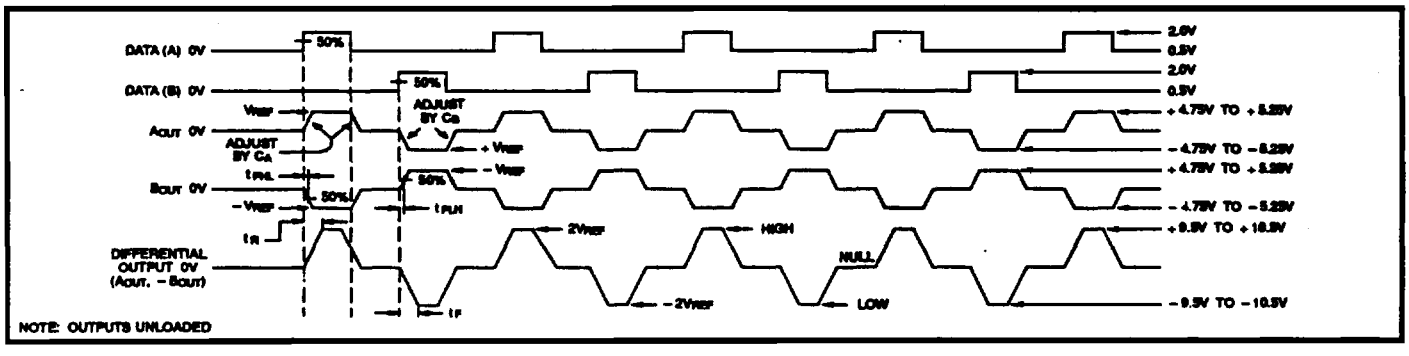


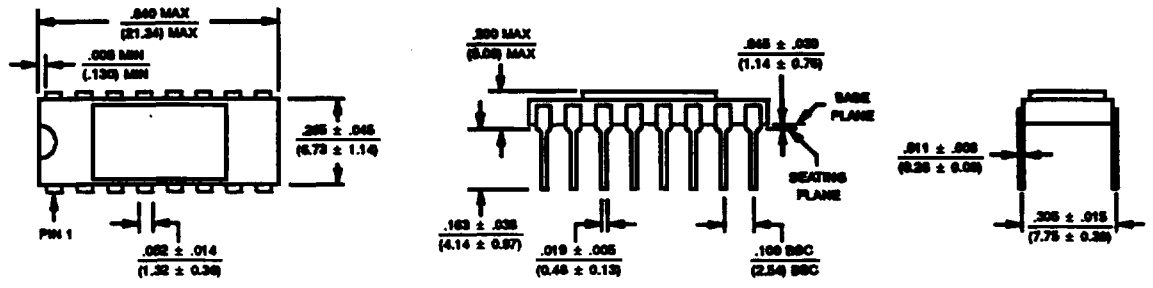
FIGURE 3. SWITCHING WAVEFORMS

HI-8383 Standard Packaging

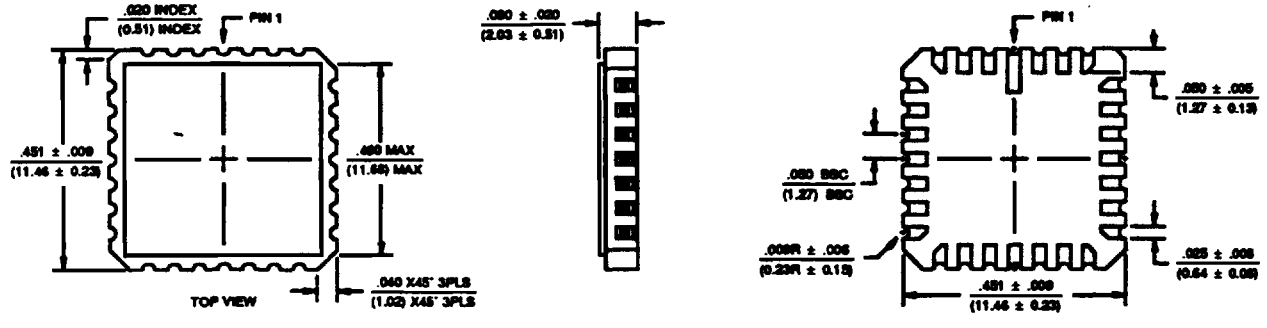
TERMINAL CONNECTIONS

16 PIN DIP				28 PIN LEADLESS CHIP CARRIER (LCC) 28 PIN J-LEADED PLASTIC CHIP CARRIER (PLCC)							
PIN		PIN		PIN		PIN		PIN		PIN	
1	V_{REF}	9	+V	1	V_{REF}	8	N/C	15	GND	22	C_B
2	$\overline{STROBE}$	10	N/C	2	N/C	9	C_A	16	+V	23	DATA (B)
3	SYNC	11	B_{OUT}	3	$\overline{STROBE}$	10	N/C	17	B_{OUT}	24	N/C
4	DATA (A)	12	C_B	4	SYNC	11	N/C	18	N/C	25	CLOCK
5	C_A	13	DATA (B)	5	N/C	12	N/C	19	N/C	26	N/C
6	A_{OUT}	14	CLOCK	6	DATA (A)	13	A_{OUT}	20	N/C	27	N/C
7	-V	15	N/C	7	N/C	14	-V	21	N/C	28	V_I
8	GND	16	V_I								

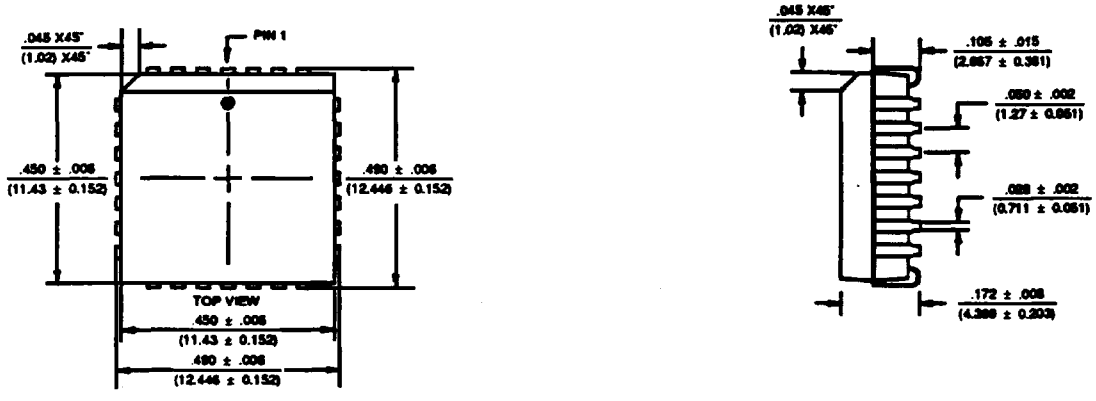
16 PIN DIP



28 PIN LEADLESS CHIP CARRIER (LCC)



28 PIN PLASTIC J-LEADED CHIP CARRIER (PLCC)



Ordering Information

INDUSTRIAL TEMPERATURE RANGE (-40°C to +85°C)

HI-8383C	-16 pin Ceramic DIP, Industrial Screen	HI-8383J	- 28 pin Plastic J-leaded PLCC, Industrial Screen
HI-8383S	- 28 pin Ceramic LCC, Industrial Screen		

MILITARY TEMPERATURE RANGE (-55°C to +125°C)

HI-8383CT	- 16 pin Ceramic DIP, Industrial Screen	HI-8383JT	- 28 pin Plastic J-leaded PLCC, Industrial Screen
HI-8383CM	- 16 pin Ceramic DIP, w/o burn-in	HI-8383ST	- 28 pin Ceramic LCC, Industrial Screen
HI-8383CM-01	- 16 pin Ceramic DIP, with burn-in	HI-8383SM	- 28 pin Ceramic LCC, w/o burn-in
		HI-8383SM-01	- 28 pin Ceramic LCC, with burn-in

Additional packaging and screening options are available upon request. **Vendor CAGE Number: 44270**

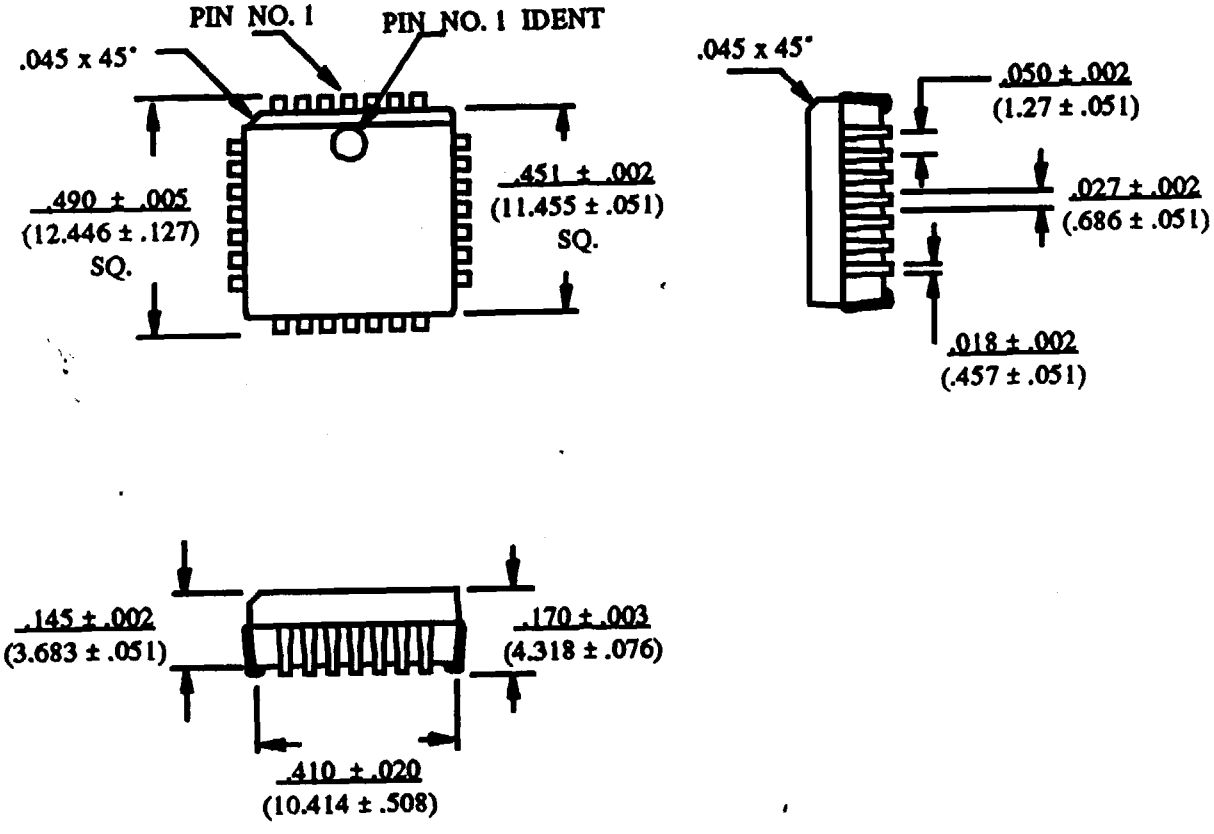
NOTES:

HOLT INC.
INTEGRATED CIRCUITS

Holt Integrated Circuits, Inc. / 45 PARKER, **Irvine, CA 92718 / (714) 859-8800 or (800) 222-HOLT** 07/92

28-PIN PLASTIC PLCC HI-8382J / HI-8383J

Package Type Designator: J



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INTEGRATED CIRCUITS

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HI-8382J PIN ASSIGNMENTS

(28-Pin J-Lead Plastic PLCC Package)

PIN NO.	PIN FUNCTION	PIN NO.	PIN FUNCTION
1	V_{REF}	15	GND
2	N/C	16	+V
3	$\overline{\text{STROBE}}$	17	B_{OUT}
4	SYNC	18	N/C
5	N/C	19	N/C
6	DATA (A)	20	N/C
7	N/C	21	N/C
8	N/C	22	C_B
9	C_A	23	DATA(B)
10	N/C	24	N/C
11	N/C	25	CLOCK
12	N/C	26	N/C
13	A_{OUT}	27	N/C
14	-V	28	V_l

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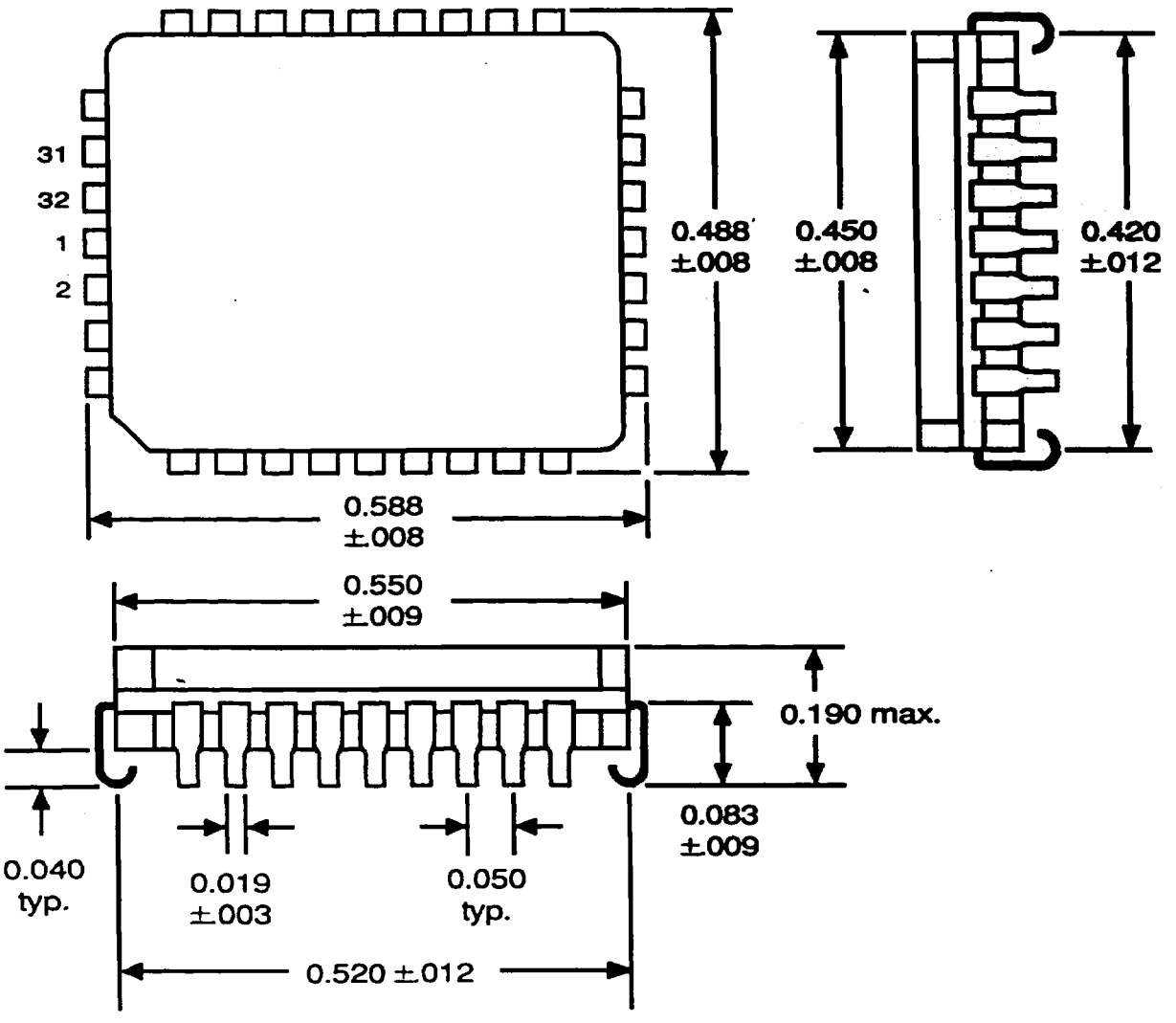
32-PIN J-LEAD CERQUAD

HI-8382U / HI-8383U SERIES



SIZE	FSCM / CAGE NO.	DOC. NO.	REV. New
A	44270	SCALE: None	SHEET 2 OF 2

PIN ASSIGNMENTS

HI-8383U *Series Packages*

PIN #	FUNCTION
1	VREF
2	STROBE
3	SYNC
4	N/C
5	N/C
6	N/C
7	N/C
8	DATA (A)
9	C_A
10	N/C
11	N/C
12	N/C
13	AOUT
14	N/C
15	-V
16	N/C
17	GND
18	+V
19	N/C
20	N/C
21	BOUT
22	N/C
23	N/C
24	C_B
25	DATA (B)
26	N/C
27	N/C
28	N/C
29	N/C
30	CLOCK
31	V1
32	N/C