# QUAD S-R LATCH — 54/74279

## SPEED/PACKAGE AVAILABILITY

54 F,W 74 B

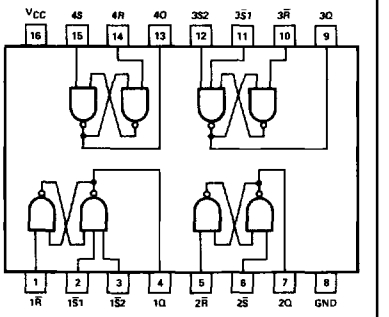
## TRUTH TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{S}$* | $\overline{R}$ | Q |
| H | H | $Q_0$ |
| L | H | H |
| H | L | L |
| L | L | H[1] |

H = high level
L = low level
$Q_0$ = the level of Q before these input conditions were established
*For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low
[1]This output is pseudo-stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (H) level.

## PIN CONFIGURATION

B,F,W PACKAGE




## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| TEST CONDITIONS | | | | 54/74 $C_L$ = 15pF $R_L$ = 400Ω | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | FROM INPUT | TO OUTPUT | MIN | TYP | MAX | UNIT |
| Propagation delay time | | | | | | | |
| $t_{PLH}$ | Low-to-high | $\overline{S}$ | | | 12 | 22 | ns |
| $t_{PHL}$ | High-to-low | | | | 9 | 15 | |
| $t_{PHL}$ | High-to-low | $\overline{R}$ | | | 15 | 27 | |

Load circuit and typical waveforms are shown at the front of section.

LOGIC

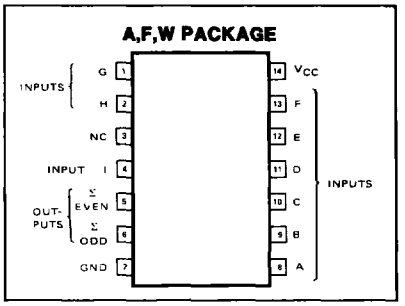
# 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER — 54/74280

## SPEED/PACKAGE AVAILABILITY

54S F,W 74S A

## PIN CONFIGURATION

A,F,W PACKAGE




## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| TEST CONDITIONS | | | | 54/74S $C_L$ = 15pF $R_L$ = 180Ω | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | FROM INPUT | TO OUTPUT | MIN | TYP | MAX | UNIT |
| Propagation delay time | | | | | | | |
| $t_{PLH}$ | Low-to-high | Data | Σ Even | | 14 | 21 | ns |
| $t_{PHL}$ | High-to-low | | | | 11.5 | 18 | |
| $t_{PLH}$ | Low-to-high | Data | Σ Odd | | 14 | 21 | |
| $t_{PHL}$ | High-to-low | | | | 11.5 | 18 | |

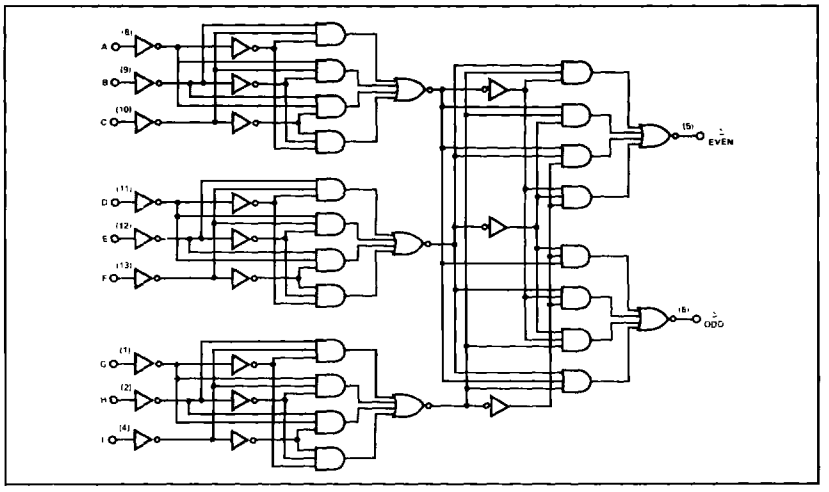
Load circuit and typical waveforms are shown at the front of section.

## TRUTH TABLE

| NUMBER OF INPUTS A THRU I THAT ARE HIGH | OUTPUTS | |
|---|---|---|
| | Σ EVEN | Σ ODD |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

H = high level L = low level

## BLOCK DIAGRAM






## SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

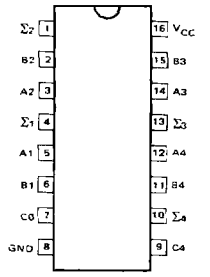
## DESCRIPTION

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

## PIN CONFIGURATION

B,F,W PACKAGE

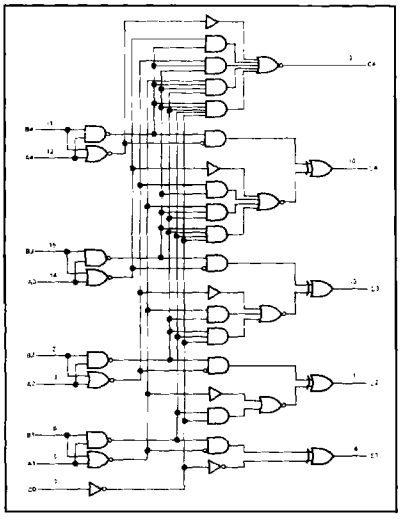



## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER★ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | LIMITS MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | C0 | Any Σ | $C_L$ = 15pF, $R_L$ = 2kΩ | | 16 | 24 | ns |
| $t_{PHL}$ | | | | | 15 | 24 | |
| $t_{PLH}$ | $A_i$ or $B_i$ | $\Sigma_i$ | | | 15 | 24 | ns |
| $t_{PHL}$ | | | | | 15 | 24 | |
| $t_{PLH}$ | C0 | C4 | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | | 11 | 17 | |
| $t_{PLH}$ | $A_i$ or $B_i$ | C4 | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | | 12 | 17 | |

★$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

## BLOCK DIAGRAM



## TRUTH TABLE

| INPUT | | | | OUTPUT | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN CO=L | | | WHEN CO=H | | |
| | | | | | | WHEN C2=L | | | WHEN C2=H |
| A1 | B1 | A2 | B2 | Σ1 | Σ2 | C2 | Σ1 | Σ2 | C2 |
| A3 | B3 | A4 | B4 | Σ3 | Σ4 | C4 | Σ3 | Σ4 | C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4

LOGIC

# DECADE COUNTER 54/74290

## SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

## DESCRIPTION

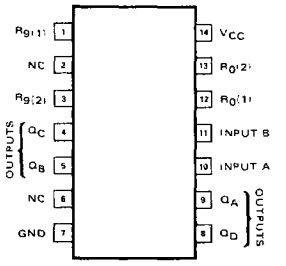
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS290 has a gated zero reset and has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

## PIN CONFIGURATION

A,F,W PACKAGE



**BCD COUNT SEQUENCE**
**(See Note A)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**BI-QUINARY (5-2)**
**(See Note B)**

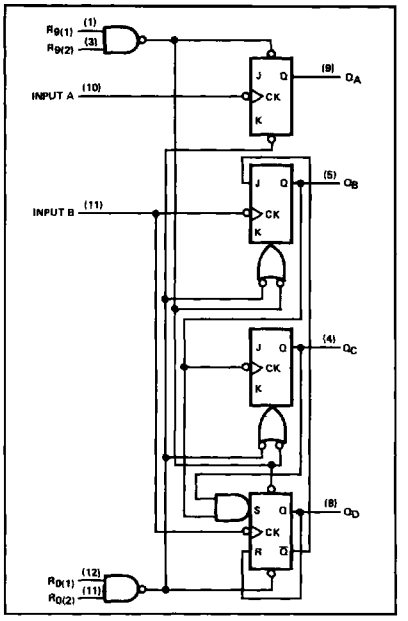
| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{g(1)}$ | $R_{g(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

NOTES:
A. Output $Q_A$ is connected to input B for BCD count.
B. Output $Q_D$ is connected to input A for bi-quinary count.
C. Output $Q_A$ is connected to input B.
D. H = high level, L = low level, X = irrelevant

**BLOCK DIAGRAM**



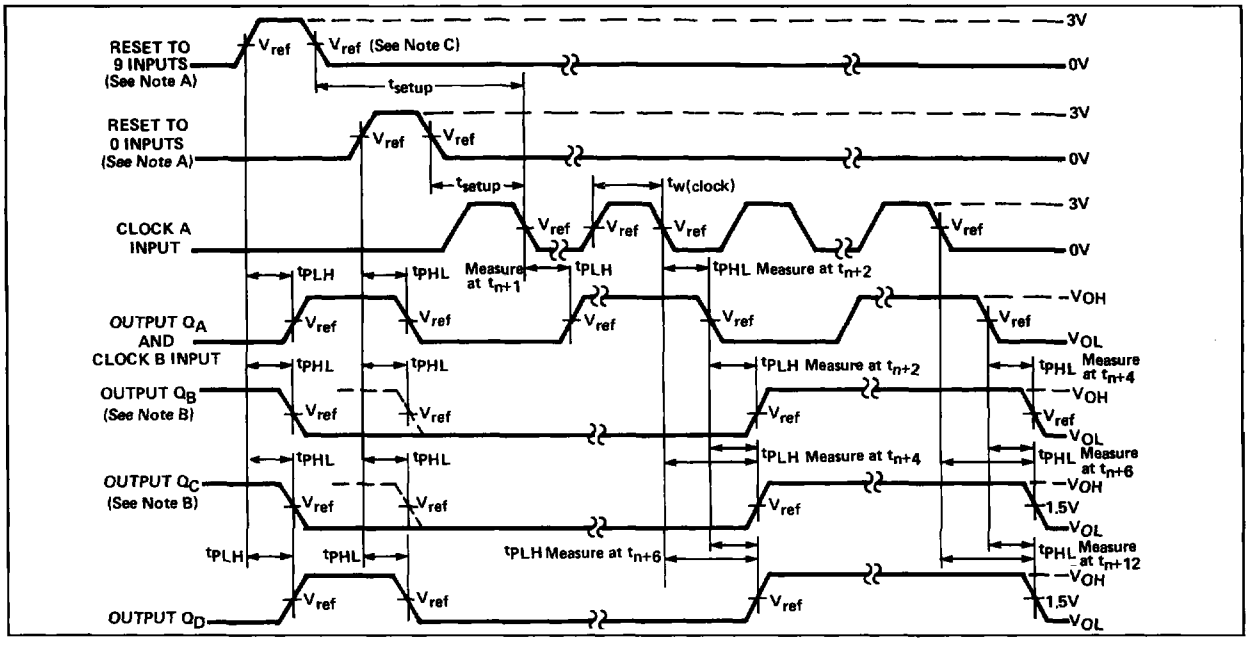

The J and K inputs shown without connection are for reference only and are functionally at a high level.

## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER* | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | LIMITS | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | UNIT |
| $f_{Count}$ | | A | $Q_A$ | | 32 | 42 | | MHz |
| | | B | $Q_B$ | | 16 | | | |
| $t_w$ | Input pulse width | | | | | | | |
| | | A | Q | | 15 | | | ns |
| | | B | Q | | 30 | | | ns |
| | | Reset | Q | | 15 | | | ns |
| $t_{Setup}$ | Input setup time | | | | 25↓ | | | ns |
| Propagation delay time | | | | | | | | |
| $t_{PLH}$ | Low-to-high level | A | $Q_A$ | $C_L$ = 15pF, $R_L$ = 2kΩ | | 10 | 16 | ns |
| $t_{PHL}$ | High-to-low level | | | | | 12 | 18 | |
| $t_{PLH}$ | Low-to-high level | A | $Q_D$ | | | 32 | 48 | ns |
| $t_{PHL}$ | High-to-low level | | | | | 34 | 50 | |
| $t_{PLH}$ | Low-to-high level | B | $Q_B$ | | | 10 | 16 | ns |
| $t_{PHL}$ | High-to-low level | | | | | 14 | 21 | |
| $t_{PLH}$ | Low-to-high level | B | $Q_C$ | | | 21 | 32 | ns |
| $t_{PHL}$ | High-to-low level | | | | | 23 | 35 | |
| $t_{PLH}$ | Low-to-high level | B | $Q_D$ | | | 21 | 32 | ns |
| $t_{PHL}$ | High-to-low level | | | | | 23 | 35 | |
| $t_{PHL}$ | High-to-low level | Set-to-0 | Any | | | 26 | 40 | ns |
| $t_{PLH}$ | Low-to-high level | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | ns |
| $t_{PHL}$ | High-to-low level | | $Q_B$, $Q_C$ | | | 26 | 40 | |

$t_{PLH}$ = low-to-high-level output
$t_{PHL}$ = high-to-low-level output

## PARAMETER MEASUREMENT INFORMATION




**VOLTAGE WAVEFORMS**

NOTES:

A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15ns$, $t_f \leq 5ns$, PRR = 1 MHz, duty cycle ≈ 50%, $Z_{out} \approx 50$ ohms.

B. $C_L$ includes probe and jig capacitance.

C. All diodes are 1N916 or 1N3064.

D. Each reset input is tested separately with the other reset at 4.5V.

E. Reference waveforms are shown with dashed lines.

F. $V_{ref}$ = 1.3V.

LOGIC



## SPEED/PACKAGE AVAILABILITY

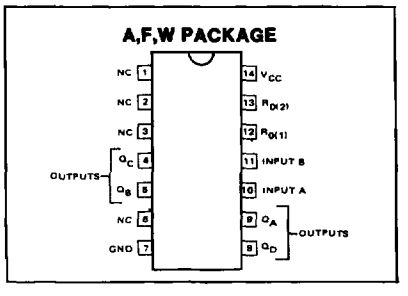
54LS F,W 74LS A

## DESCRIPTION

This monolithic counter contains four master-slave flip-flops and a gated zero reset to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

To use the maximum count length (decade or four-bit binary) of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the function table.

## PIN CONFIGURATION

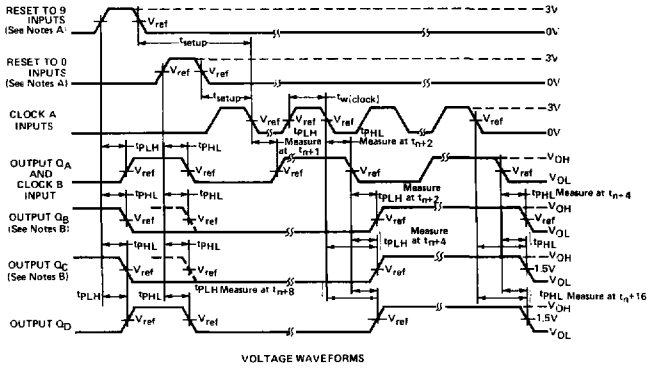


## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER★ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | LIMITS MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{Count}$ | A | $Q_A$ | | 32 | 42 | | MHz |
| | B | $Q_B$ | | 16 | | | |
| $t_w$ Input pulse width | A | Q | | 15 | | | ns |
| | B | Q | | 30 | | | ns |
| | Reset | Q | | 15 | | | ns |
| $t_{Setup}$ Input setup time | | | | 25↓ | | | ns |
| $t_{PLH}$ | A | $Q_A$ | $C_L$ = 15pF, | | 10 | 16 | ns |
| $t_{PHL}$ | | | $R_L$ = 400Ω | | 12 | 18 | |
| $t_{PLH}$ | A | $Q_D$ | | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 46 | 70 | |
| $t_{PLH}$ | B | $Q_B$ | | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | |
| $t_{PLH}$ | B | $Q_C$ | | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | |
| $t_{PLH}$ | B | $Q_D$ | | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | ns |

★$f_{max}$ = maximum count frequency
$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output

## PARAMETER MEASUREMENT INFORMATION




### VOLTAGE WAVEFORMS

NOTES:
A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. $C_L$ includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. $V_{ref}$ = 1.3 V.

## COUNT SEQUENCE

(See Note C)

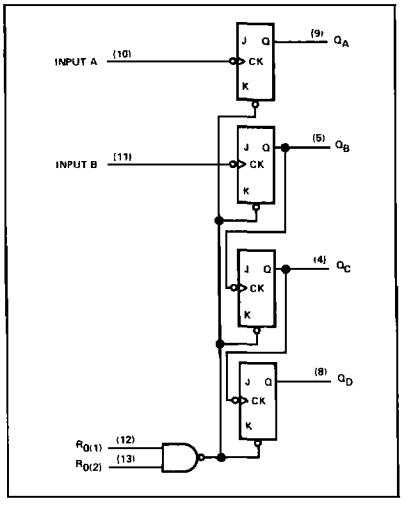
| COUNT | OUTPUT $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|---|---|---|---|---|
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

## RESET/COUNT FUNCTION TABLE

| RESET INPUTS $R_{0(1)}$ | $R_{0(2)}$ | OUTPUT $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|---|---|---|---|---|---|
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

NOTES:
A. Output $Q_A$ is connected to input B for BCD count.
B. Output $Q_D$ is connected to input A for bi-quinary count.
C. Output $Q_A$ is connected to input B.
D. H = high level, L = low level, X = irrelevant

## BLOCK DIAGRAM




The J and K inputs shown without connection are for reference only and are functionally at a high level.