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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR

2SK3511

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3511 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance: $R_{DS(on)} = 12.5 \, m\Omega$ MAX. (Vgs = 10 V, Ib = 42 A)
- Low Ciss: Ciss = 5900 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3511	TO-220AB
2SK3511-S	TO-262
2SK3511-ZJ	TO-263
2SK3511-Z	TO-220SMD Note

Note TO-220SMD package is produced only in Japan.

(TO-220AB)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	75	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±83	Α
Drain Current (pulse) Note1	I _{D(pulse)}	±260	Α
Total Power Dissipation (Tc = 25°C)	Рт	100	W
Total Power Dissipation (T _A = 25°C)	Рт	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note2	IAS	52	Α
Single Avalanche Energy Note2	Eas	250	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting Tch = 25°C, VDD = 35 V, RG = 25 Ω , VGS = 20 \rightarrow 0 V



(TO-262)



(TO-263, TO-220SMD)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.25	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W



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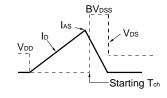


ELECTRICAL CHARACTERISTICS (TA = 25°C)

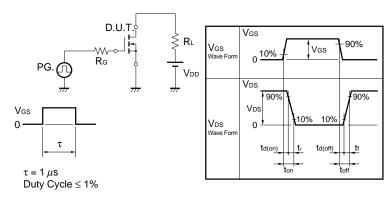
		1		1	1	
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ioss	Vps = 75 V, Vgs = 0 V			10	μΑ
Gate Leakage Current	Igss	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.0	3.0	4.0	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 42 A	21	45		S
Drain to Source On-state Resistance	R _{DS(on)}	Vgs = 10 V, ID = 42 A		9.5	12.5	mΩ
Input Capacitance	Ciss	Vps = 10 V		5900		pF
Output Capacitance	Coss	Vgs = 0 V		810		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		400		pF
Turn-on Delay Time	t _{d(on)}	VDD = 38 V, ID = 42 A		30		ns
Rise Time	t r	Vgs = 10 V		21		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 0 \Omega$		72		ns
Fall Time	t f			12		ns
Total Gate Charge	Q _G	VDD = 60 V		100		nC
Gate to Source Charge	Qgs	Vgs = 10 V		24		nC
Gate to Drain Charge	Q _{GD}	ID = 83 A		35		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 83 A, VGS = 0 V		1.1		V
Reverse Recovery Time	trr	IF = 83 A, VGS = 0 V		70		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		200		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \, \Omega \\ \text{VGS} = 20 \rightarrow 0 \, \text{V} \end{array} \begin{array}{c} \text{PG.} \\ \text{PS.} \\ \text{W.s.} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{V.DD.} \\ \text{V.DD.} \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = 2 \text{ mA} \\ \hline \\ VOD \end{array}$$



0

lo - Drain Current - A

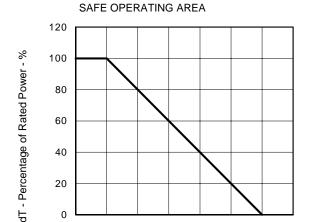
0

25

50

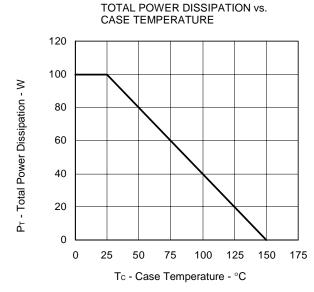
TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS



Tc - Case Temperature - °C

75

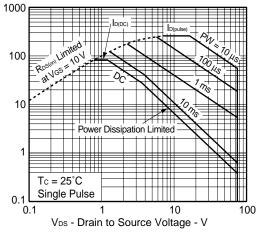




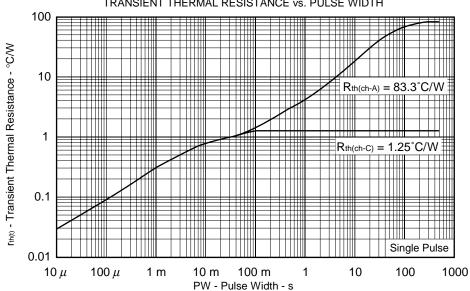
100

125

150 175

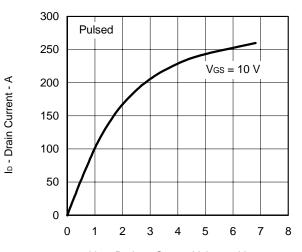


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



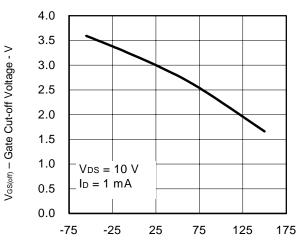


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



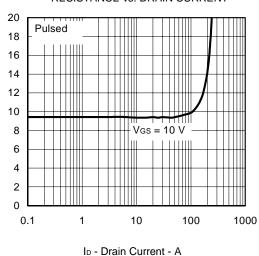
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

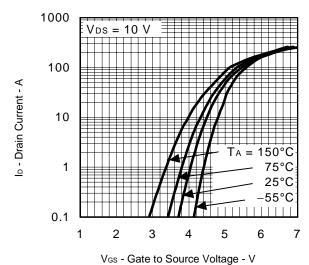


 T_{ch} - Channel Temperature - $^{\circ}C$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

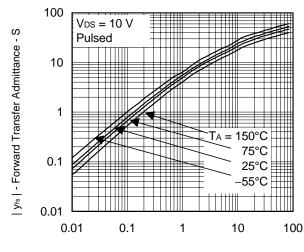


FORWARD TRANSFER CHARACTERISTICS



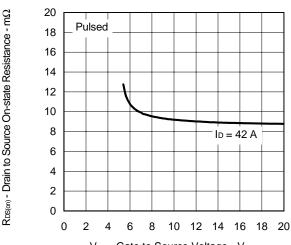
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FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



ID - Drain Current - A

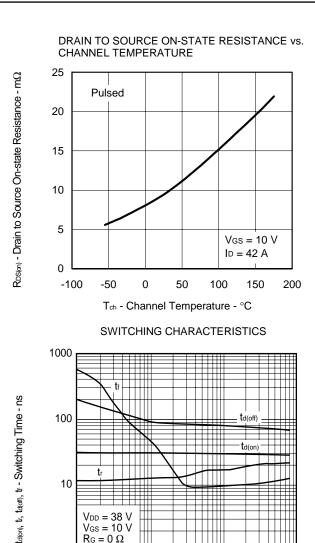
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

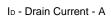


Vgs - Gate to Source Voltage - V

 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$





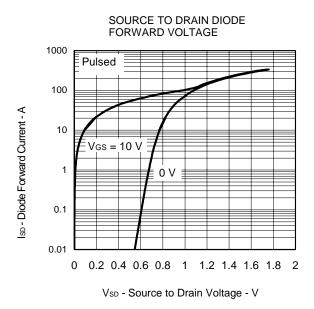


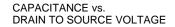
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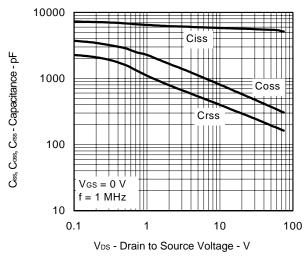
100

 $V_{GS} = 10 \text{ V}$ $R_{G} = 0 \Omega$

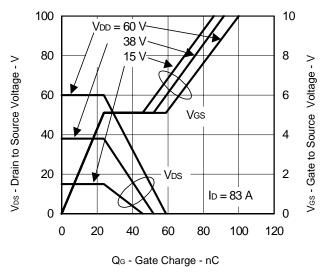
0.1



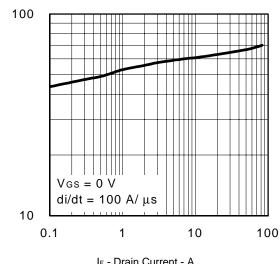




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



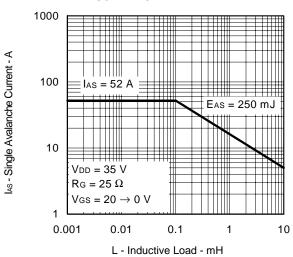
REVERSE RECOVERY TIME vs. DRAIN CURRENT



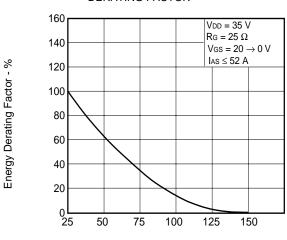
IF - Drain Current - A

tr - Reverse Recovery Time - ns

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



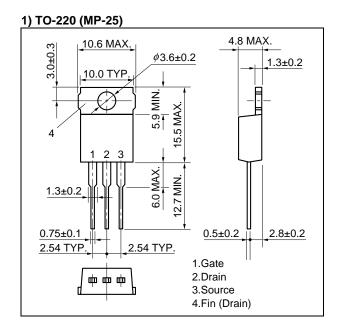
SINGLE AVALANCHE ENERGY DERATING FACTOR

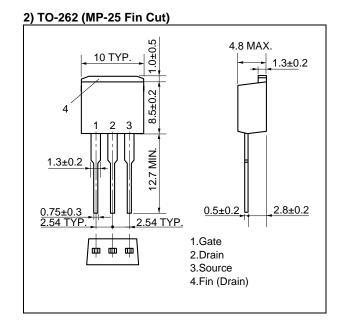


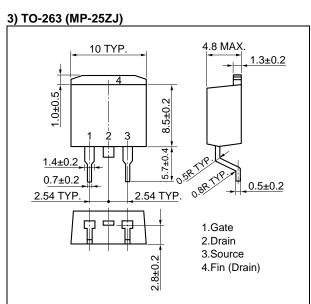
Starting T_{ch} - Starting Channel Temperature - $^{\circ}$ C

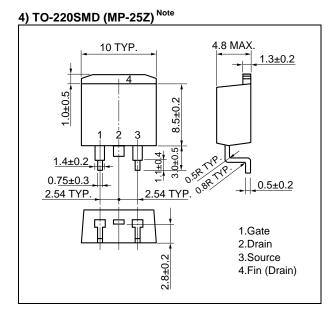


PACKAGE DRAWINGS (Unit: mm)



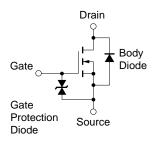






Note This Package is only produced in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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