4-Port HDMI™ Signal Switch with I²C Control

Features

- 4:1 HDMI Switch Mux/DeMux
- Non-Blocking EQ path for ideal EQ control in main Receiver chipset
- -3dB bandwidth up to 4.6Gbps to support HDMI 1.3a (16-bit color depth per channel)
- HDMI 1.4 data rate ready
- DDC active signal buffer or passive switch selectable
- I²C Register control for switch configuration
- Automatic HDCP reset circuitry for quick communication when switching from one port to another
- Connector Plug-in detection and Interrupt Flag setting
- Selectable HPD signal outputs with 5V open drain output stage or 3.3V output buffer
- 3.3V power supply and standby power supply
- TMDS output enable control
- Ultra-low power consumption to support Energy Star™ Compliance
- ESD protection on all I/O pins
  - 8kV contact per IEC61000-4-2, level 4
- Packaging (Pb-free & Green available):
  - 80-contact LQFP

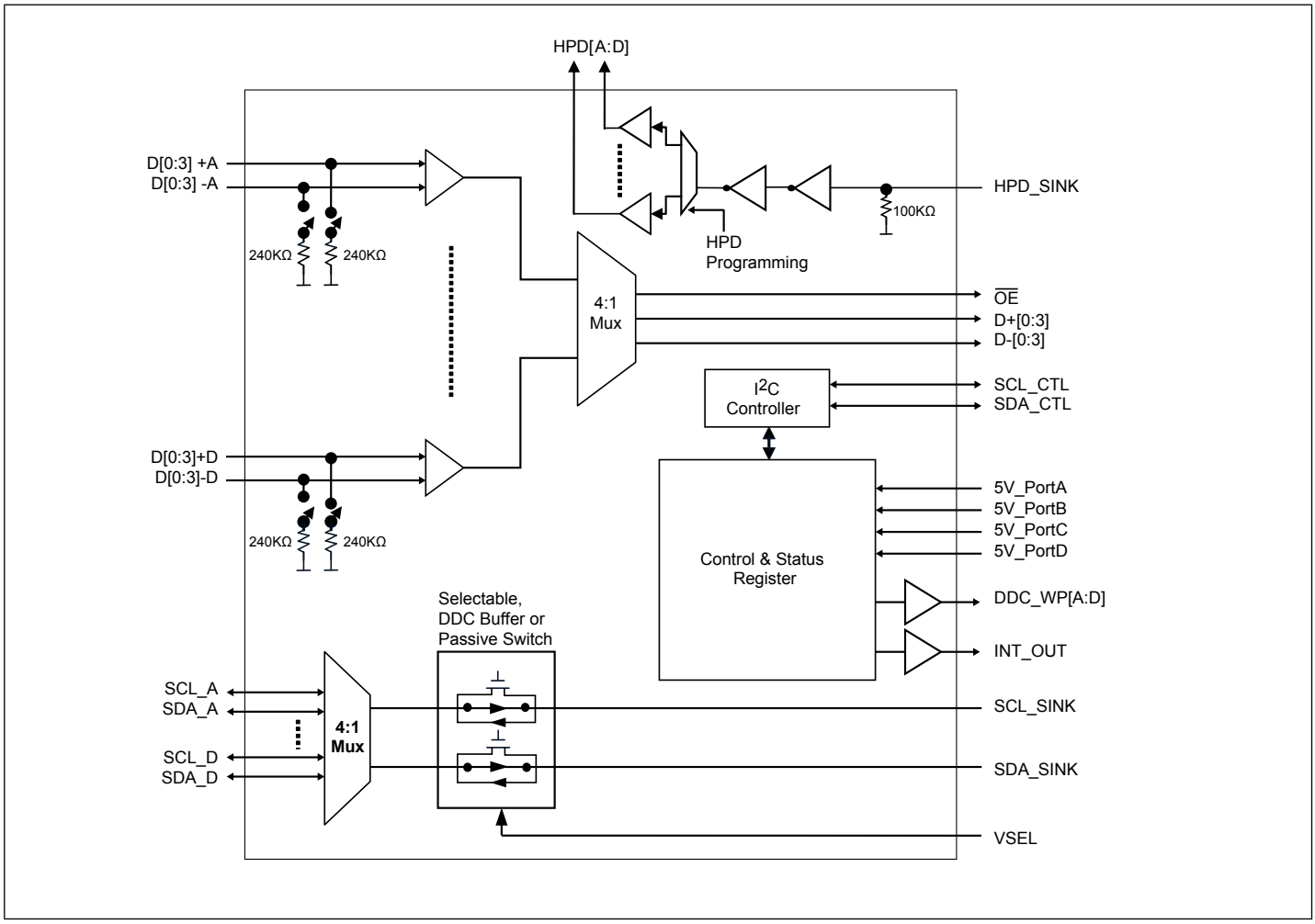
Description

Pericom Semiconductor's PI3HDMI series of switch circuits are targeted for high-resolution video networks that are based on DVI/HDMI™ standards. The PI3HDMI2410-A is a 4-to-1 HDMI Mux/DeMux signal switch. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation. The maximum data rate support is up to 4.6Gbps which can meet HDMI 1.3a standard and support the resolution requirement of next generation HDTV and PC graphics of HDMI 1.4.

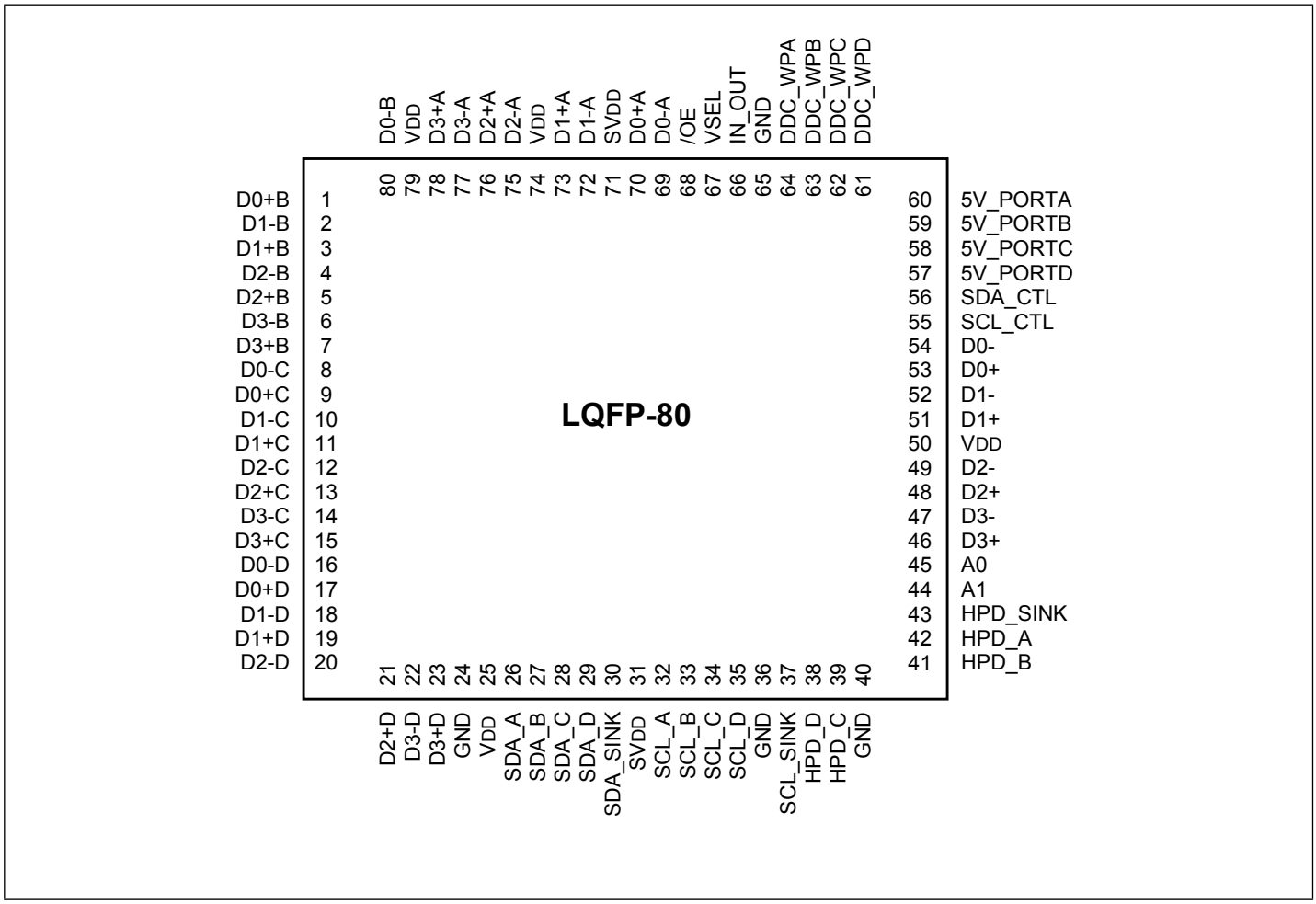
PI3HDMI2410-A is designed specifically for ATC-Sink requirements. All switch control settings are through I²C bus to provide flexible design and reduce peripheral components. Selectable active signal buffer for DDC bus can optimize the bi-directional data transmission for long trace or cable applications.

All input pins are protected with Pericom's ESD protection circuits supporting ESD damage as high as 8kV contact per IEC61000-4-2 Level 4 specification. The ultra-low power operation of PI3HDMI2410-A meets the demand of low power consumption Energy Star™ designs.

Block Diagram



Pin Assignment – 80-Contact LQFP



Pinout Table

Pin Name	I/O Type	Description
V_{DD}	Power	3.3V power supply. When V_{DD} is off, the TMDS and DDC channels will be powered down.
SV_{DD}	Power	3.3V or 5V standby power supply. SV_{DD} is for all side band signals (except DCC) and the I²C control register unit.
GND	Ground	Ground connection
HPD_SINK	I	Sink side hot plug detector input with 100kΩ pull-down resistor to ground.
HPD_A	O	Port A HPD output
HPD_B	O	Port B HPD output
HPD_C	O	Port C HPD output
HPD_D	O	Port D HPD output
D0+A D0-A D1+A D1-A D2+A D2-A D3+A D3-A	I/O	Port A TMDS input / output
D0+B D0-B D1+B D1-B D2+B D2-B D3+B D3-B	I/O	Port B TMDS input / output
D0+C D0-C D1+C D1-C D2+C D2-C D3+C D3-C	I/O	Port C TMDS input / output

Continued >

Pin Name	I/O Type	Description
D0+D D0-D D1+D D1-D D2+D D2-D D3+D D3-D	I/O	Port D TMDS input / output
D0+ D0- D1+ D1- D2+ D2- D3+ D3-	I/O	Sink Side TMDS input / output
SCL_A	I/O	Port A DDC Clock
SCL_B	I/O	Port B DDC Clock
SCL_C	I/O	Port C DDC Clock
SCL_D	I/O	Port D DDC Clock
SDA_A	I/O	Port A DDC Data
SDA_B	I/O	Port B DDC Data
SDA_C	I/O	Port C DDC Data
SDA_D	I/O	Port D DDC Data
SCL_SINK	I/O	Sink side DDC Clock
SDA_SINK	I/O	Sink side DDC Data
SCL_CTL	I/O	I²C Clock
SDA_CTL	I/O	I²C Data
INT_OUT	O	Interrupt pin. Logic status output pin of INT flag.
DDC_WPA, DDC_WPB, DDC_WPC, DDC_WPD,	O	Open drain output. General purpose logic configured by B0b[5].
$\overline{OE}$	I	Output Enable control. Active low. $\overline{OE}$ only disables the high-speed TMDS channel but not the side band signals and I²C circuitry supplied by SV_{DD}.

Continued >

Pin Name	I/O Type	Description
A1	I	I²C Address 1
A0	I	I²C Address 0
5V_PortA, 5V_PortB, 5V_PortC, 5V_PortD	I	Connector 5V port.
VSEL	I	DDC buffer V_{IL} selection. VSEL = 0V, V_{IL} = 0.5V (Default value with 70kΩ pull-down resistor) VSEL = 0.5 V_{DD}, V_{IL}=0.45V VSEL = V_{DD}, V_{IL}=0.6V

I²C Control Register

	b7 (MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address Byte	1	0	1	0	1	A1 (W)	A0 (W)	1/0 *

* 0:Write; 1:Read

Truth Table

If HPD Sink is used, B0b[4] = 0

Port Selection	HPD Input Select	HPD Output Select	HPDA	HPDB	HPDC	HPDD
Port A	HPD Sink	Open Drain	HPD Sink	L	L	L
Port B	HPD Sink	Open Drain	L	HPD Sink	L	L
Port C	HPD Sink	Open Drain	L	L	HPD Sink	L
Port D	HPD Sink	Open Drain	L	L	L	HPD Sink

Port Selection	HPD Input Select	HPD Output Select	HPDA	HPDB	HPDC	HPDD
Port A	HPD Sink	Buffer	$\overline{\text{HPD Sink}}$	H	H	H
Port B	HPD Sink	Buffer	H	$\overline{\text{HPD Sink}}$	H	H
Port C	HPD Sink	Buffer	H	H	$\overline{\text{HPD Sink}}$	H
Port D	HPD Sink	Buffer	H	H	H	$\overline{\text{HPD Sink}}$

Data Byte 0: Control Register

For register access, Byte 0 and Byte 1 are sequentially Read or Write together

Bit	Description	Type	Power Up Condition	Logic Settings
7	HDMI input port selection	W	0	00 = Port A 01 = Port B 10 = Port C 11 = Port D
6	HDMI input port selection	W	0	
5	DDC_WP Write Protection Setting	W	0	0 = Not active. DDC_WPA, DDC_WPB, DDC_WPC, and DDC_WPD pins are all set to Hi-Z 1 = Write Protection Active DDC_WPA, DDC_WPB, DDC_WPC, and DDC_WPD pins are all set to logic Low.
4	HPD Input Selection	W	0	0 = HPD_SINK When B1b[7] = 0 (open drain mode) HPD[A:D] logic = HPD_SINK logic When B1b[7] = 1 (output buffer mode) HPD[A:D] logic = Inverted HPD_SINK logic 1 = I²C Register Setting from B0b[0:3] Under I²C register control mode, HPD[A:D] can be individually controlled by B0b[0:3] for HPD output.
3	HPD Port D Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B1b[7] = 0 (open drain mode) B0b[3]=0, set HPD [D] to Low B0b[3]=1, set HPD [D] to Hi-Z When B1b[7] = 1 (output buffer mode) B0b[3]=0, set HPD [D] to High B0b[3]=1, set HPD [D] to Low II. Byte0 b[4] = 0 Test Mode

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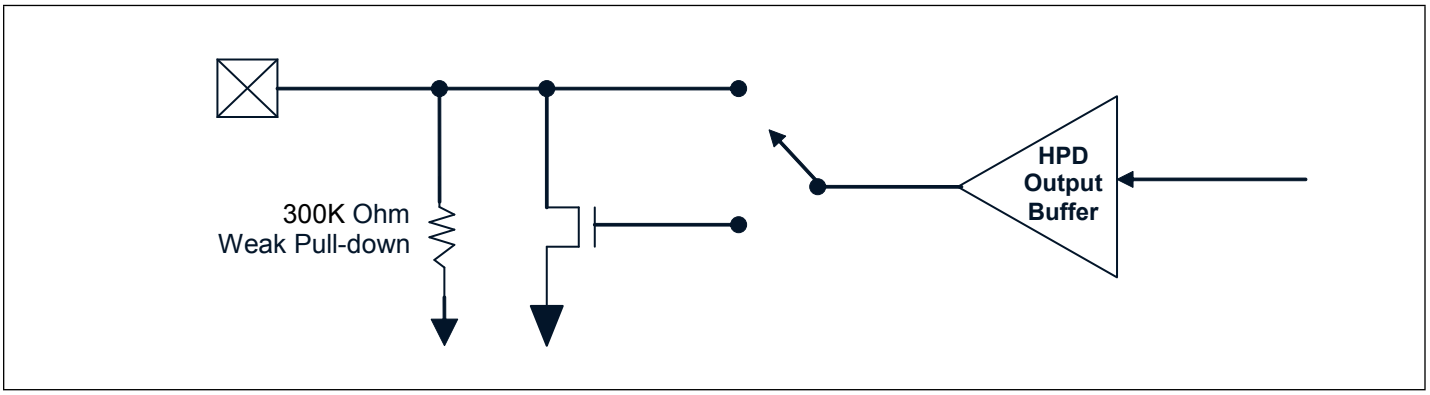
Bit	Description	Type	Power Up Condition	Logic Settings
2	HPD Port C Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B1b[7] = 0 (open drain mode) B0b[2]=0, set HPD [C] to Low B0b[2]=1, set HPD [C] to Hi-Z When B1b[7] = 1 (output buffer mode) B0b[2]=0, set HPD [C] to High B0b[2]=1, set HPD [C] to Low II. Byte0 b[4] = 0 Test Mode
1	HPD Port B Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B1b[7] = 0 (open drain mode) B0b[1]=0, set HPD [B] to Low B0b[1]=1, set HPD [B] to Hi-Z When B1b[7] = 1 (output buffer mode) B0b[1]=0, set HPD [B] to High B0b[1]=1, set HPD [B] to Low II. Byte0 b[4] = 0 Test Mode
0	HPD Port A Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B1b[7] = 0 (open drain mode) b[0]=0, set HPD [A] to Low b[0]=1, set HPD [A] to Hi-Z When B1b[7] = 1 (output buffer mode) b[0]=0, set HPD [A] to High b[0]=1, set HPD [A] to Low. II. Byte0 b[4] = 0 Test Mode

Data Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Logic Settings
7	HPD Output Stage selection	W	0	0 = Open Drain 1 = Output Buffer
6	TMDS Output Enable	W	1	0 = Output Disable Disabled TMDS channel and enter standby mode. Side band signals and I²C circuitry are still alive. 1 = Output Enable
5	5V_PortD connect	R	0	0 = Disconnected 1 = Connected; INT Flag B1b[1] is set by 5V_PortD edge signal when logic state changes from High to Low or from Low to High.
4	5V_PortC connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortC edge signal when logic state changes from High to Low or from Low to High
3	5V_PortB connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortB edge signal when logic state changes from High to Low or from Low to High.
2	5V_PortA connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortA edge signal when logic state changes from High to Low or from Low to High.
1	INT Flag	RW	0	0 = INT Flag Clear 1 = INT Flag Set INT Flag will be set from logic Low to High, when any 5V_Port has detected plug or unplug transition action. INT Flag is cleared to low after I²C bus reads the register byte 1.
0	DDC channel selection	W	0	0 = Passive switch 1 = Active switch buffer For power saving operation, passive switch can be selected to further reduce the active power consumption.

HPD Output Buffer



Note:

1. During normal or standby mode, the HPD block is active. HPD signal output is programmed by the control register, B0b[0:4].
2. Open drain buffer is recommended with a 1K-Ohm pull-up resistor to 5V. If HPD output buffer is selected, external buffer transistor is required to avoid 5V to 3.3V leakage.

HPD Output Logic Control

Byte 0 bit 4 selects the HPD signal input from HPD_Sink pin or from internal control register B0b[0:3]. SV_{DD} provides power supply to HPD block.

	HPD	
SVDD, 5V Standby Power	**B0b[4]=1, HPD = I²C Register Setting B0b[3:0]**	**B0b[4]=0, HPD = HPD_SINK**
Off	LOW (internal weak pull-down resistor to ground)	LOW (internal weak pull-down resistor to ground)
On	Control Register Setting	HPD_Sink (Default=Low)

TMDS Channel Pull-down Resistor Control

Pull-down resistor active conditions:

1. The Data Channel is unselected
2. Output enable control $\overline{OE}$ is disable($\overline{OE}$=High) or B1b[6]=Low, pull down on all channels
3. Without normal operation supply VDD input (but standby voltage SVDD is still On), pull down on all channels

Output Enable Control

Output Enable or Disable can be asserted through external $\overline{OE}$ pin or through I²C.

$\overline{OE}$	OE_I2C B1b[6]	Operation
Low	High	Enable
Low	Low	Disable
High	X	Disable

*** Default value: $\overline{OE}$ = Low ; Byte 1 b[6] = High**

Absolute Maximum Ratings (Over operating free-air temperature range)

Item	Rating
Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-20 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Specifications V_{DD} = 3.3V ±10%, Ambient Temperature -40 to +85°C

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	Supply Current of V_{DD} and SV_{DD}	Output Enable, SV_{DD} = 3.3V		4	5.0	mA
I_{DDQ}	Quiescent Supply Current of V_{DD} and SV_{DD}	Output Disable, SV_{DD} = 3.3V		1.0	2.0	
I_{DDsb}	Standby Supply Current	SV_{DD} = 3.3V, V_{DD} = 0V		0.1	0.5	
V_{OH_DDC}	DDC passive switch Output High Voltage	V_{IN} = 3.3V External pull-up to VDD from 1.5kΩ to 2kΩ.	V_{DD}-1.0			V
V_{OL_DDC}	DDC Buffer Output Low Voltage	Source side, External pull-up to V_{DD} from 1.5kΩ to 4.7kΩ			0.4	
		Sink side, I_{OL} = 3mA	0.65	0.75	0.97	

Symbol	Parameter	Conditions	Min	Nom	Max	Units
$V_{IH\_5V\_A}$' $V_{IH\_5V\_B}$' $V_{IH\_5V\_C}$' $V_{IH\_5V\_D}$'	Input High Voltage of 5V ports		2.4			
$V_{IL\_5V\_A}$' $V_{IL\_5V\_B}$' $V_{IL\_5V\_C}$' $V_{IL\_5V\_D}$'	Input Low Voltage of 5V ports				0.8	
V_{OL_HPD}	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	
	Open Drain Output Low Voltage	I_{OL} = 4 mA	0		0.4	
V_{OH_HPD}	Buffer Output High Voltage	I_{OH} = 3 mA	2.4			
$I_{OFF\ (HPD)}$	Off Leakage Current	V_{DD} = 0V, V_{IN} = 3.6V		12		µA
		V_{DD} = 0V, V_{IN} = 5.5V		20		
I_{OZ_HPD}	Open Drain Output Leakage Current	V_{DD} = 3.6V, V_{IN} = 3.6V		12		
		V_{DD} = 3.6V, V_{IN} = 5.5V		21		
$V_{OL\_DDC\_WP}$	Open Drain Output Low Voltage				0.4	V
C_{IO}[1]	Input/output capacitance (Passive Switch)	V_{DD} = 0V or 3.0V, Frequency = 100kHz		6	9	pF

Note:

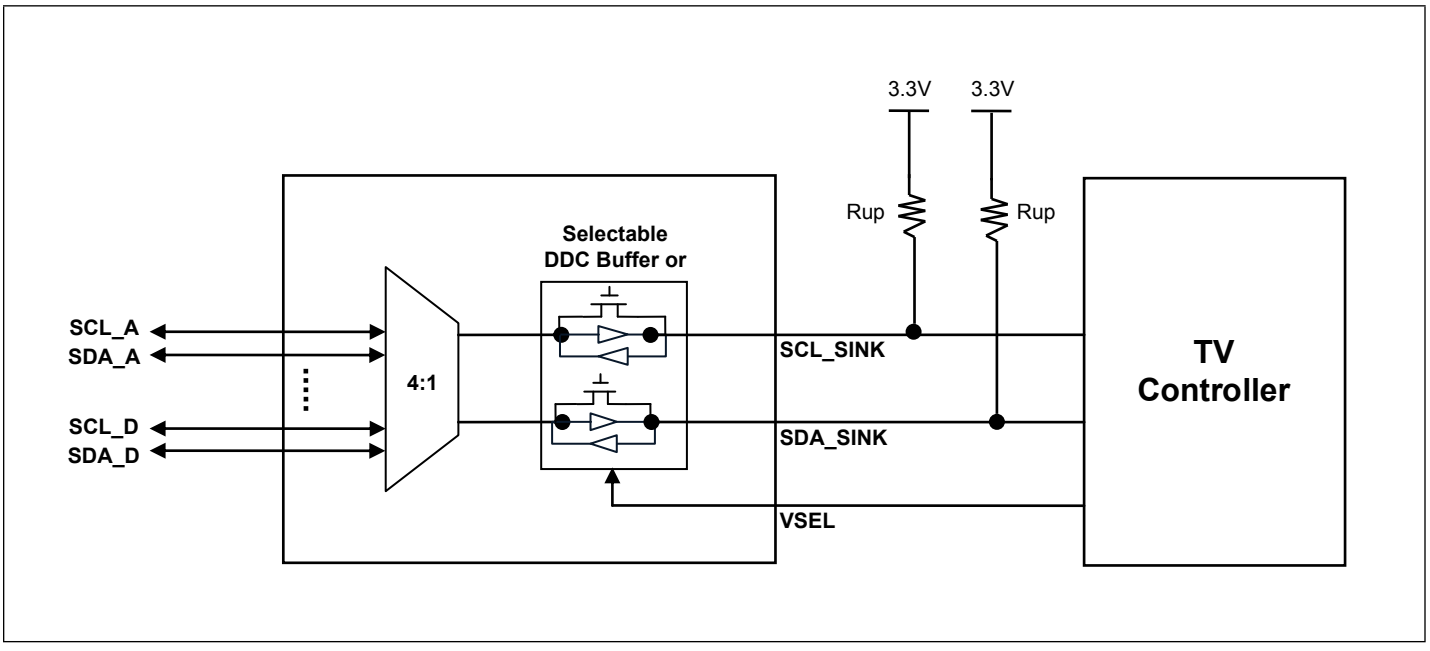
1. Measured at Vbias = 0V or 5V, Vrms = 0.2V; Vbias = 1.65V, Vrms = 0.2V; Vbias = 2.5V, Vrms = 1.2V

DDC Channel Block

V_{DD} = 3.3V ±10%, Ambient Temperature -40 to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{OH\ Passive\ (Sink)}$	Sink Side DDC Passive Switch Output High Voltage	V_{IN}=3.3V. External pull-up Rup to V_{DD} from 1.5kΩ to 2kΩ	V_{DD} - 0.5			V
V_{IH_DDC}	Source Side DDC Buffer Input High Voltage		2			V
V_{IL_DDC}	Source Side DDC Buffer Input Low Voltage				0.4	V
V_{OL_DDC1}	Sink Side DDC Buffer Output Low Voltage, V_{SEL} = V_{DD}	External pull-up Rup to V_{DD} from 1.5kΩ to 2kΩ	0.7		0.9	V
V_{IL_DDC1}	Sink Side DDC Buffer Input Low Voltage, V_{SEL} = V_{DD}				0.62	V
V_{OL_DDC2}	Sink Side DDC Buffer Output Low Voltage, V_{SEL} = GND	External pull-up Rup to V_{DD} from 1.5kΩ to 2kΩ	0.7		0.9	V
V_{IL_DDC2}	Sink Side DDC Buffer Input Low Voltage, V_{SEL} = GND				0.5	V
V_{OL_DDC3}	Sink Side DDC Buffer Output Low Voltage, VSEL = 0.5 V_{DD}	External pull-up to V_{DD} from 1.5kΩ to 2kΩ	0.7		0.9	V
V_{IL_DDC3}	Sink Side DDC Buffer Input Low Voltage, V_{SEL} = 0.5 V_{DD}				0.46	V

DDC Channel Application Diagram



Dynamic Specifications

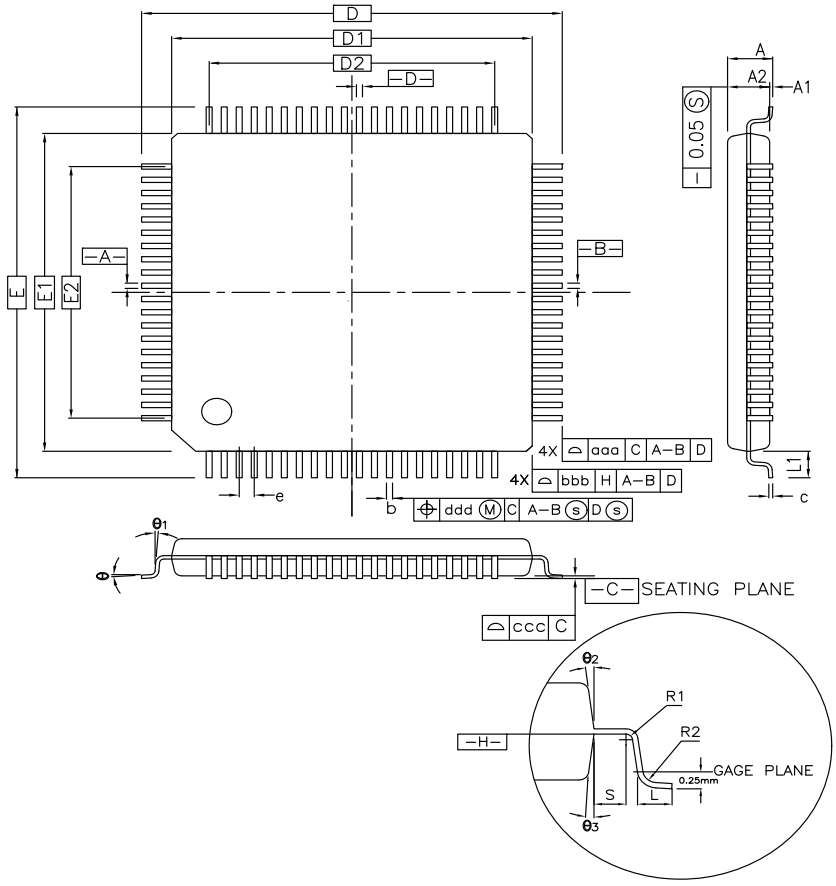
V_{DD} = 3.3V ±10%, T_A -40 to +85°C, GND = 0V

Parameter	Description	Conditions	Min	Typ	Max	Units
X_{TALK}	Crosstalk on High-speed Channels	f = 1.13 GHz		-34		dB
		f = 825 MHz		-36		
O_{IRR}	OFF Isolation on High-speed Channels	f = 1.13 GHz		-36		
		f = 825 MHz		-38		
I_{LOSS}	Defferential Insertion Loss on High-speed Channels	DR = 1.65Gbps DR = 2.0Gbps DR = 2.25Gbps DR = 3.0Gbps DR = 3.4Gbps		-1.5 -1.73 -1.82 -2.4 -2.7		dB
BW	-3dB BW for TMDS channels			2.3		GHz

Capacitance Measurement

Test Condition	Capacitance	Units
SDA_CTL	3.0	pF
SCL_CTL	2.3	
HPD_Sink	1.7	

Packaging Mechanical: 80-Contact LQFP (FF)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D_1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E_1	12.00 BSC.			0.472 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTE :
1. ALL DIMENSION IN MM
2. Refer JEDEC MS–026/BDD
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM® Enabling Serial Connectivity

DATE: 03/18/09

DESCRIPTION: 80-contact, Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FF (FF80)

DOCUMENT CONTROL #: PD-2064 REVISION: A

07-0100

Note:

- **For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php**

Ordering Information

Ordering Code	Package Code	Package Type
PI3HDMI2410-AFFE	FF80	Pb-free & Green, 80-Contact, LQFP

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. E = Pb-free and Green

3. Adding an X suffix = Tape/Reel