CMOS SRAM
256K-BIT(32K X 8) N341256

■ Features

- CMOS SRAM organized as 32,768 X 8bits
- Single +5.0V(±10%) Power Supply
- High Speed Access time : 12/15/20/25ns
- Low power operation

  N341256 (Standard type)

  Active : 180mA(max.)

  Standby : 60mA(max.)

  N341256-L (Low Power type)

  Active : 160mA(max.)

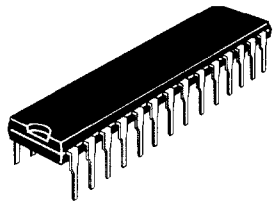
  Standby : 55mA(max.)

●Packages

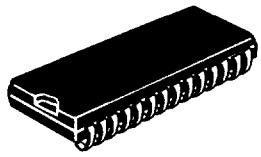
-28pin Plastic DIP(300mil)

-28pin Plastic SOJ(300mil)

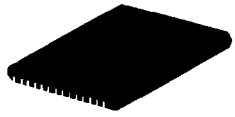
-28pin Plastic TSOP (Type I)



28pin Plastic DIP(300mil)



28pin Plastic SOJ(300mil)



28pin Plastic TSOP(Type I)

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■ Description

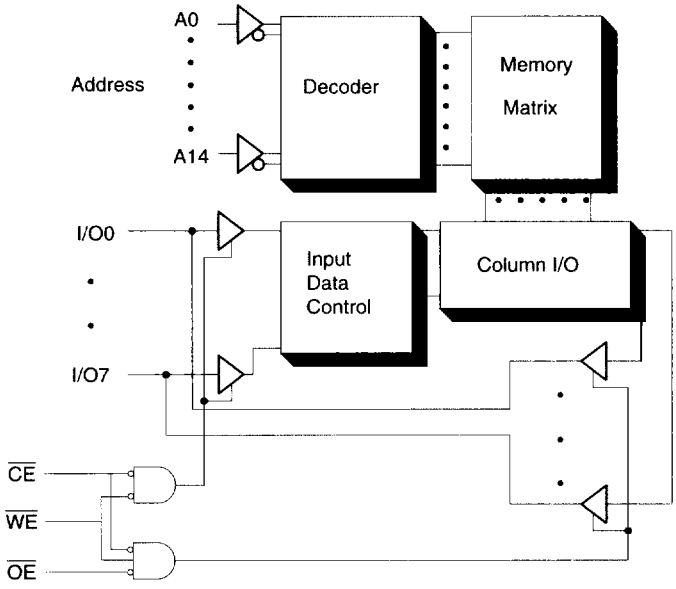
The N341256 is a high performance CMOS static RAM organized as 32,768 X 8bits.

Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip select ($\overline{CE}$) inputs are both Low.

Reading is accomplished when $\overline{WE}$ is High and $\overline{CE}$ and the output enable ($\overline{OE}$) are both Low.

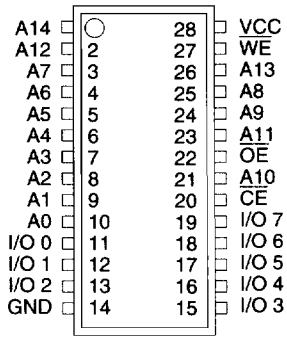
The N341256 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

■ Functional Block Diagram

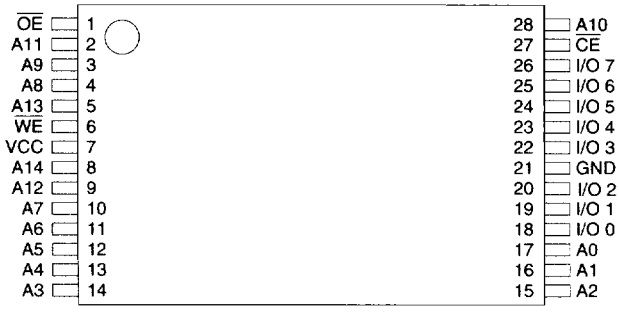


■ Pin Configuration

28 pin Plastic DIP/SOJ



28 pin Plastic TSOP (Type I)



■ Pin Description

SYMBOL	PIN NAME
A0-A14	Address input
I/O0-I/O7	Data input/output
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
VCC	PowerSupply Pin(+5V)
GND	Ground Pin

■ Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	High	High impedance	Standby
Low	High	Low	Data out	Read
X	Low	Low	Data in	Write
High	High	Low	High impedance	Output disable

Note : X = don't care.

■ Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-55 to 125	°C
TSTG	Storage Temperature	-55 to 125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTICE

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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■ Recommended Operating Conditions

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	VCC
0°C to 70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	VCC + 0.5V	V
VIL	Input Low Voltage	-0.5	-	0.8	V

Note : VIL(min) = -3.0V for pulse width less than 20ns.

■ Capacitance

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

■ DC Electrical Characteristics

(Vcc=5.0V ± 10%, TA = 0 to +70°C, VLC ≤ 0.2V, VHC ≥ VCC - 0.2V)

Symbol	Parameter	Power	N341256 -12	N341256 -15	N341256 -20	N341256 -25	Unit
ICC	Dynamic Operating Current	Standard type	180	170	160	150	mA
	$\overline{CE}$ ≤ VIL, VCC = max, f = fmax, IOUT = 0mA	Low Power type	160	150	140	130	mA
	VIN ≥ VIH or ≤ VIL						
ISB	Standby Power Supply Current (TTL level)	Standard type	60	50	40	35	mA
	$\overline{CE}$ ≥ VIH, VCC = max, f = fmax, VIN ≥ VIH or ≤ VIL	Low Power type	55	45	35	30	mA
ISB1	Full Standby Power Supply Current (CMOS level)	Standard type	10	10	10	10	mA
	$\overline{CE}$ ≥ VHC, VCC = max, f = 0, VIN ≥ VHC or ≤ VLC	Low Power type	5	5	5	5	mA

DC Electrical Characteristics(1)

(Vcc = 5.0V ± 10%)

Symbol	Parameter	Test condition	Standard type		Low Power type		Unit
			Min.	Max.	Min.	Max.	
I ILI I	Input Leakage current	VCC = max, VIN = GND to VCC	-	5	-	2	μA
I ILO I	Output Leakage Current	VCC = max, $\overline{CE}$ ≥ VIH, VOUT = GND to VCC	-	5	-	2	μA
VOL	Output low voltage	IOL =8mA, VCC = min	-	0.4	-	0.4	V
		IOL =10mA, VCC = min	-	0.5	-	0.5	V
VOH	Output high voltage	IOL =-4mA, VCC = min	2.4	-	2.4	-	V

■ AC Test Conditions

Input pulse levels	GND to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2

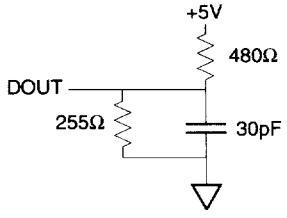


Figure 1. Output Load Equivalent

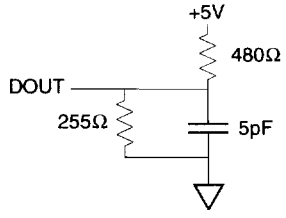


Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

(Vcc=5.0V ± 10%, TA = 0°C to 70°C)

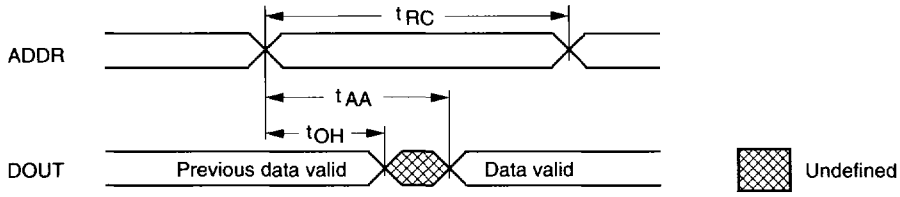
Description	Symbol	N341256-12		N341256-15		N341256-20		N341256-25		Unit
Read Cycle		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle time	t_{RC}	12		15		20		25		ns
Address access time	t_{AA}		12		15		20		25	ns
Chip enable access time	t_{ACE}		12		15		20		25	ns
Output hold from address change	t_{OH}	3		3		3		3		ns
Chip enable to output in low-Z	t_{LZCE}	5		5		5		5		ns
Chip disable to output in high-Z	t_{HZCE}		5		5		5		10	ns
Chip enable to power up time	t_{PU}	0		0		0		0		ns
Chip disable to power down time	t_{PD}		12		15		20		25	ns
Output enable access time	t_{AOE}		6		8		10		12	ns
Output enable to output in low-Z	t_{LZOE}	0		0		0		0		ns
Output disable to output in high-Z	t_{HZOE}		5		5		5		10	ns

(Vcc=5.0V ± 10%, TA = 0°C to 70°C)

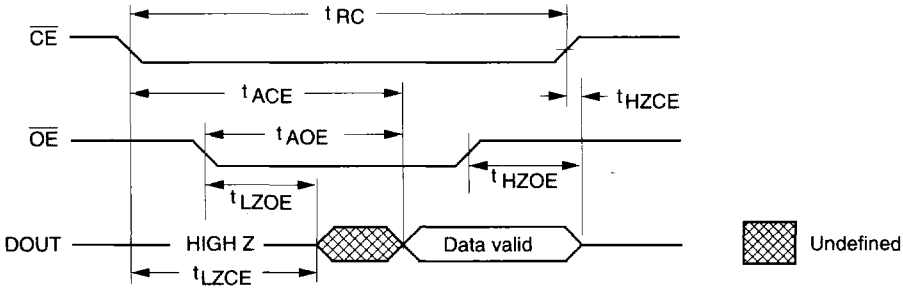
Description	Symbol	N341256-12		N341256-15		N341256-20		N341256-25		Unit
Write Cycle		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle time	t_{WC}	12		15		20		25		ns
Chip enable to end of write	t_{CW}	10		12		13		15		ns
Address valid to end of write	t_{AW}	10		12		13		15		ns
Address set-up time	t_{AS}	0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		ns
Write pulse width	t_{WP}	10		11		12		15		ns
Data set-up time	t_{DS}	7		8		9		10		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write disable to output in low-Z	t_{LZWE}	0		0		0		0		ns
Write enable to output in high-Z	t_{HZWE}		3		3		3		5	ns

■ AC Timing Waveforms

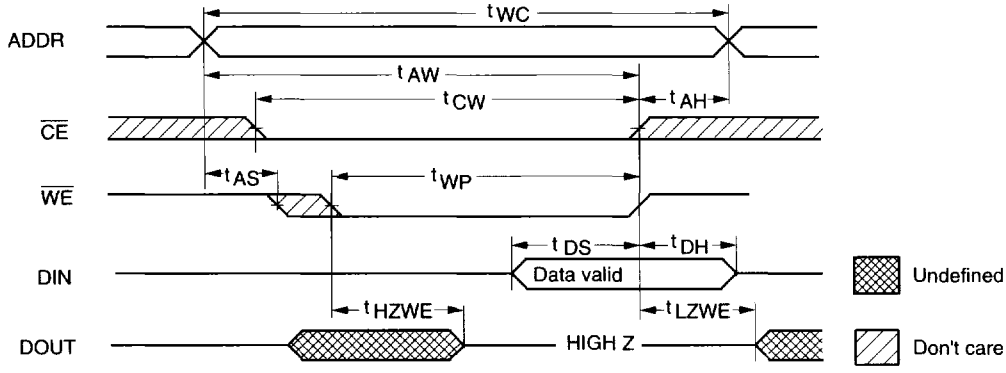
Read Cycle No.1



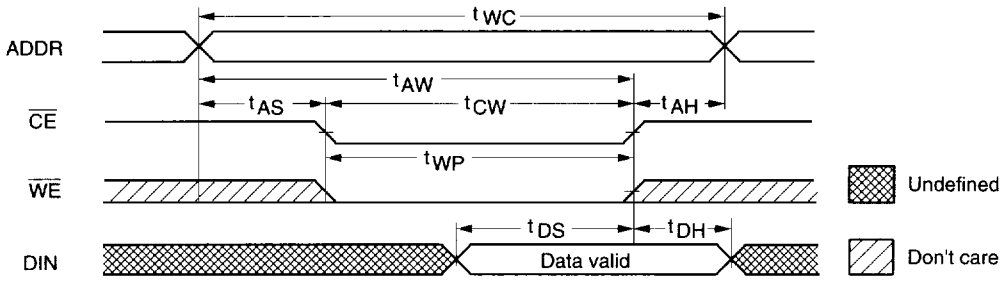
Read Cycle No.2



Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Chip Enable Controlled)



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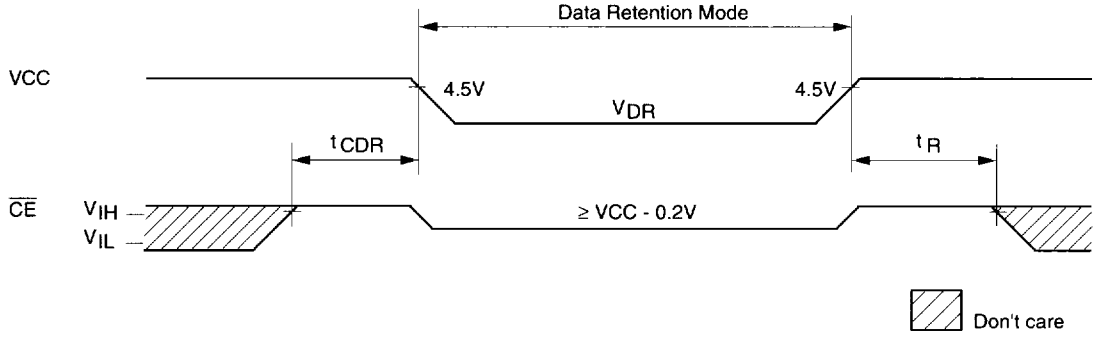
■ Data Retention Electrical Characteristics (Low Power type only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	VCC for Retention data			2	-	-	V
I_{CCDR}	Data retention current	$\overline{CE}$ ≥ VCC-0.2V	VCC = 2V	-	95	500	µA
		VIN ≥ VCC-0.2V or ≤ 0.2V	VCC = 3V	-	350	750	µA
t_{CDR}	Chip deselect to data retention time			0	-	-	ns
t_R	Operation recovery time			t_{RC}	-	-	ns

Low VCC Data Retention Waveform



■ Ordering Information

N3 41256 Δ Δ - X X □

	Device Type	Package	Speed	Power

Power	Blank	Standard Type
	L	Low Power Type
Speed	12 / 15 / 20 / 25	ns
Package	P	Plastic DIP 300mil
	SJ	Plastic SOJ 300mil
	TS	Plastic TSOP (Type I)
Device Type	41256	256Kbit SRAM 32K X 8

PART NO.	Access Time (ns)	Operating Current (mA)	Power down Standby Current (mA)	Package
N341256P-12	12	180	60	28Pin Plastic DIP
N341256SJ-12	12	180	60	28Pin Plastic SOJ
N341256TS-12	12	180	60	28Pin Plastic TSOP
N341256P-15	15	170	50	28Pin Plastic DIP
N341256SJ-15	15	170	50	28Pin Plastic SOJ
N341256TS-15	15	170	50	28Pin Plastic TSOP
N341256P-20	20	160	40	28Pin Plastic DIP
N341256SJ-20	20	160	40	28Pin Plastic SOJ
N341256TS-20	20	160	40	28Pin Plastic TSOP
N341256P-25	25	150	35	28Pin Plastic DIP
N341256SJ-25	25	150	35	28Pin Plastic SOJ
N341256TS-25	25	150	35	28Pin Plastic TSOP
N341256P-12L	12	160	55	28Pin Plastic DIP
N341256SJ-12L	12	160	55	28Pin Plastic SOJ
N341256TS-12L	12	160	55	28Pin Plastic TSOP
N341256P-15L	15	150	45	28Pin Plastic DIP
N341256SJ-15L	15	150	45	28Pin Plastic SOJ
N341256TS-15L	15	150	45	28Pin Plastic TSOP
N341256P-20L	20	140	35	28Pin Plastic DIP
N341256SJ-20L	20	140	35	28Pin Plastic SOJ
N341256TS-20L	20	140	35	28Pin Plastic TSOP
N341256P-25L	25	130	30	28Pin Plastic DIP
N341256SJ-25L	25	130	30	28Pin Plastic SOJ
N341256TS-25L	25	130	30	28Pin Plastic TSOP