

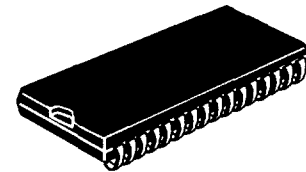


CMOS SRAM 1M-BIT(128K X 8)

PRELIMINARY
N341026

■ Features

- CMOS SRAM organized as 131,072 X 8bits
- Single +5.0V(±10%) Power Supply
- High Speed Access time : 15/17/20/25ns
- Low power operation
 - N341026 (Standard type)
 - Active : 185mA (max.)
 - Standby : 55mA (max.)
 - N341026-L (Low Power type)
 - Active : 165mA (max.)
 - Standby : 50mA (max.)



32pin Plastic SOJ(400mil)

● Packages

- 32pin Plastic SOJ(400mil)
- (Center Pin type)

■ Description

The N341026 is a high performance CMOS static RAM organized as 131,072 X 8bits.

Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip select ($\overline{CE}$) inputs are both Low .

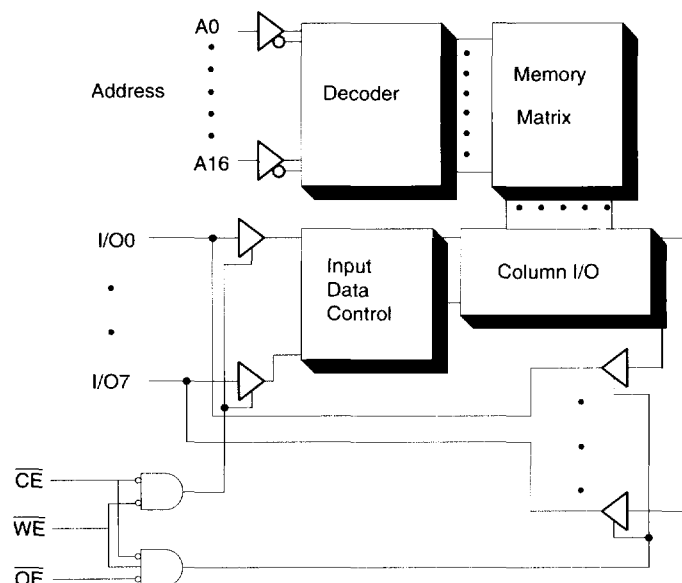
Reading is accomplished when $\overline{WE}$ is High and $\overline{CE}$ and the

output enable ($\overline{OE}$) are both Low .

The N341026 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

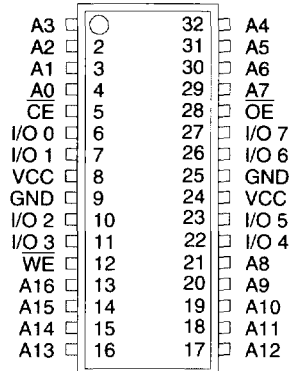
5

■ Functional Block Diagram



Pin Configuration

32 pin Plastic SOJ
Center Pin Type



Pin Description

SYMBOL	PIN NAME
A0-A16	Address input
I/O0-I/O7	Data input/output
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
VCC	Power Supply Pin(+5V)
GND	Ground Pin

Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	High	High impedance	Standby
Low	High	Low	Data out	Read
X	Low	Low	Data in	Write
High	High	Low	High impedance	Output disable

Note : X = don't care.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-55 to 125	°C
TSTG	Storage Temperature	-55 to 125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTICE

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	VCC
0°C to 70°C	0V	5.0V±10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	VCC + 0.5V	V
VIL	Input Low Voltage	-0.5	-	0.8	V

Note : VIL(min) = -3.0V for pulse width less than 20ns.

Capacitance

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN=0V	8	pF
COUT	Output Capacitance	VOUT=0V	8	pF

■ DC Electrical Characteristics

($V_{CC} = 5.0V \pm 10\%$, $T_A = 0$ to $+70^\circ C$, $V_{LC} \leq 0.2V$, $V_{HC} \geq V_{CC} - 0.2V$)

Symbol	Parameter	Power	N341026 -15	N341026 -17	N341026 -20	N341026 -25	Unit
ICC	Dynamic Operating Current $\overline{CE} \leq V_{IL}$, $V_{CC} = \max$, $f = f_{max}$, $I_{OUT} = 0mA$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$	Standard type	185	165	155	145	mA
		Low Power type	165	155	140	135	mA
ISB	Standby Power Supply Current (TTL level) $\overline{CE} \geq V_{IH}$, $V_{CC} = \max$, $f = f_{max}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$	Standard type	55	50	45	40	mA
		Low Power type	50	45	40	35	mA
ISB1	Full Standby Power Supply Current (CMOS level) $\overline{CE} \geq V_{HC}$, $V_{CC} = \max$, $f = 0$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	Standard type	10	10	10	10	mA
		Low Power type	5	5	5	5	mA

DC Electrical Characteristics(1)

($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test condition	Standard type		Low Power type		Unit
			Min.	Max.	Min.	Max.	
ILI	Input Leakage current	$V_{CC} = \max$, $V_{IN} = GND$ to V_{CC}	-5	5	-2	2	μA
ILO	Output Leakage Current	$V_{CC} = \max$, $\overline{CE} \geq V_{IH}$, $V_{OUT} = GND$ to V_{CC}	-5	5	-2	2	μA
VOL	Output low voltage	$I_{OL} = 8mA$, $V_{CC} = \min$	-	0.4	-	0.4	V
		$I_{OL} = 10mA$, $V_{CC} = \min$	-	0.5	-	0.5	V
VOH	Output high voltage	$I_{OH} = -4mA$, $V_{CC} = \min$	2.4	-	2.4	-	V

■ AC Test Conditions

Input pulse levels	GND to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2

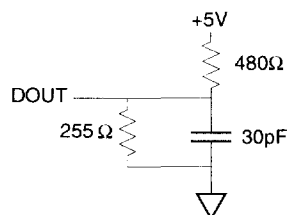


Figure 1. Output Load Equivalent

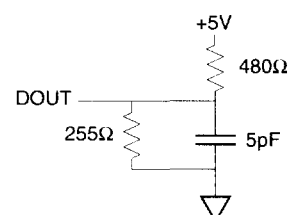


Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

(V_c = 5.0V ± 10%, T_A = 0°C to 70°C)

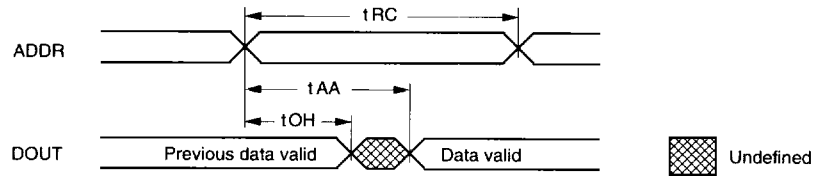
Description	Symbol	N341026-15		N341026-17		N341026-20		N341026-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
Read Cycle time	t _{RC}	15		17		20		25		ns
Address access time	t _{AA}		15		17		20		25	ns
Chip enable access time	t _{ACE}		15		17		20		25	ns
Output hold from address change	t _{OH}	3		3		3		3		ns
Chip enable to output in low-Z	t _{LZCE}	5		5		5		5		ns
Chip disable to output in high-Z	t _{HZCE}		7		7		8		10	ns
Chip enable to power up time	t _{PU}	0		0		0		0		ns
Chip disable to power down time	t _{PD}		15		17		20		25	ns
Output enable access time	t _{AOE}		6		6		6		8	ns
Output enable to output in low-Z	t _{LZOE}	0		0		0		0		ns
Output disable to output in high-Z	t _{HZOE}		6		6		6		8	ns

(V_{cc} = 5.0V ± 10%, T_A = 0°C to 70°C)

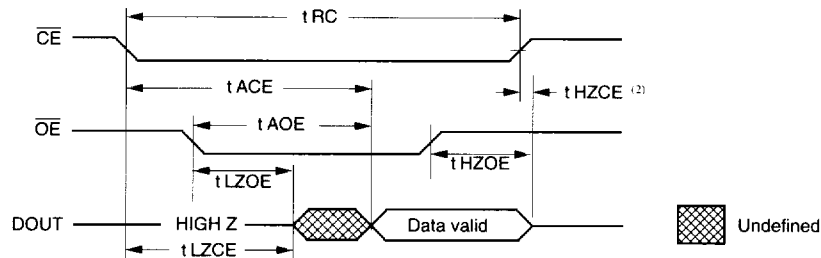
Description	Symbol	N341026-15		N341026-17		N341026-20		N341026-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
Write Cycle time	t _{WC}	15		17		20		25		ns
Chip enable to end of write	t _{CW}	11		12		13		15		ns
Address valid to end of write	t _{AW}	11		12		13		15		ns
Address set-up time	t _{AS}	0		0		0		0		ns
Address hold from end of write	t _{AH}	0		0		0		0		ns
Write pulse width ($\overline{OE} \geq V_{IH}$)	t _{WP1}	11		12		13		15		ns
Write pulse width ($\overline{OE} \leq V_{IL}$)	t _{WP2}	12		13		14		15		ns
Data set-up time	t _{DS}	7		8		8		10		ns
Data hold time	t _{DH}	0		0		0		0		ns
Write disable to output in low-Z	t _{LZWE}	0		0		0		0		ns
Write enable to output in high-Z	t _{HZWE}		7		7		8		10	ns

■ AC Timing Waveforms

Read Cycle No.1⁽¹⁾



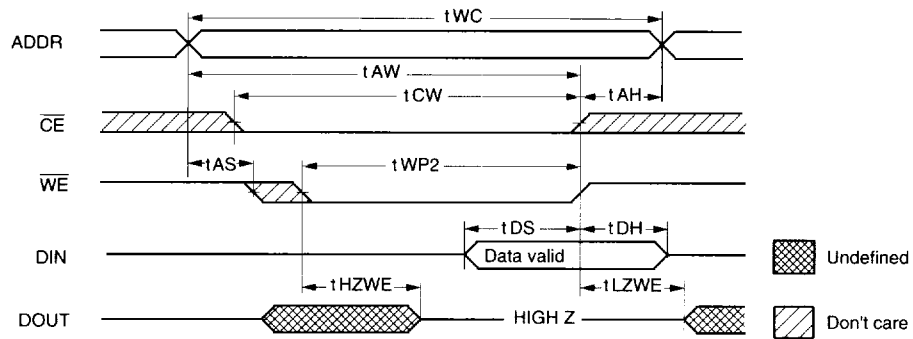
Read Cycle No.2⁽¹⁾



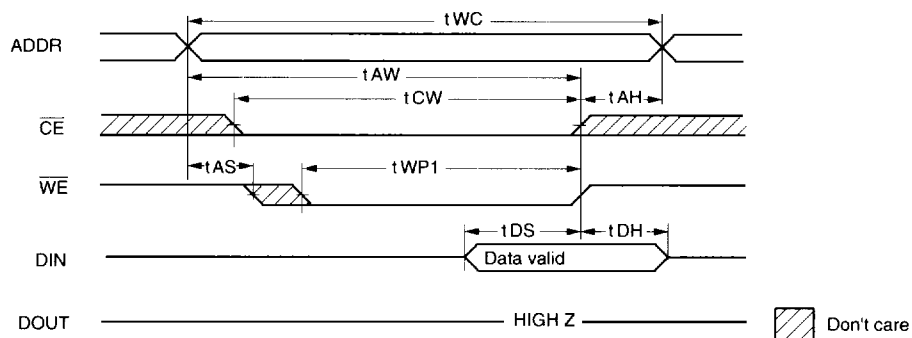
Note : (1) $\overline{WE}$ is High for READ cycle.

(2) At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .

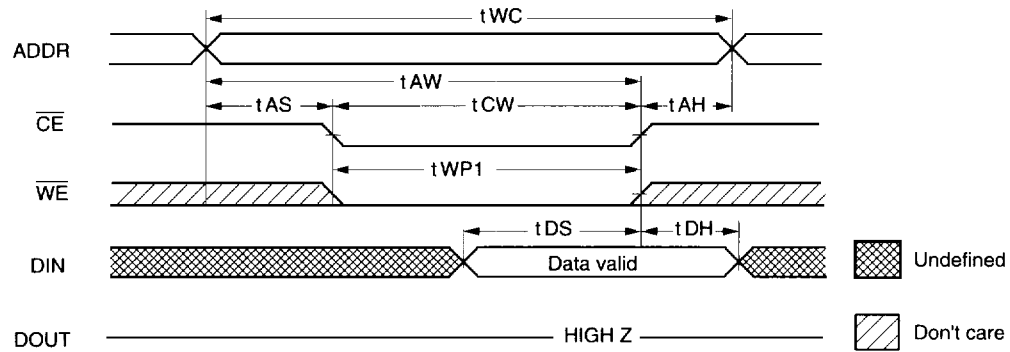
Write Cycle No.1(Write Enable Controlled)⁽⁴⁾



Write Cycle No.2(Write Enable Controlled)⁽⁴⁾



Write Cycle No.3(Chip Enable Controlled)⁽¹⁾

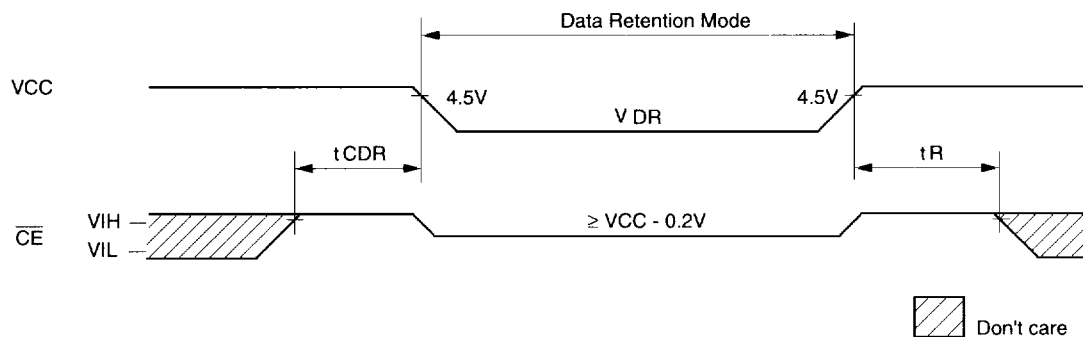


Note : (3) $\overline{OE}$ = High.
(4) $\overline{OE}$ = Low.

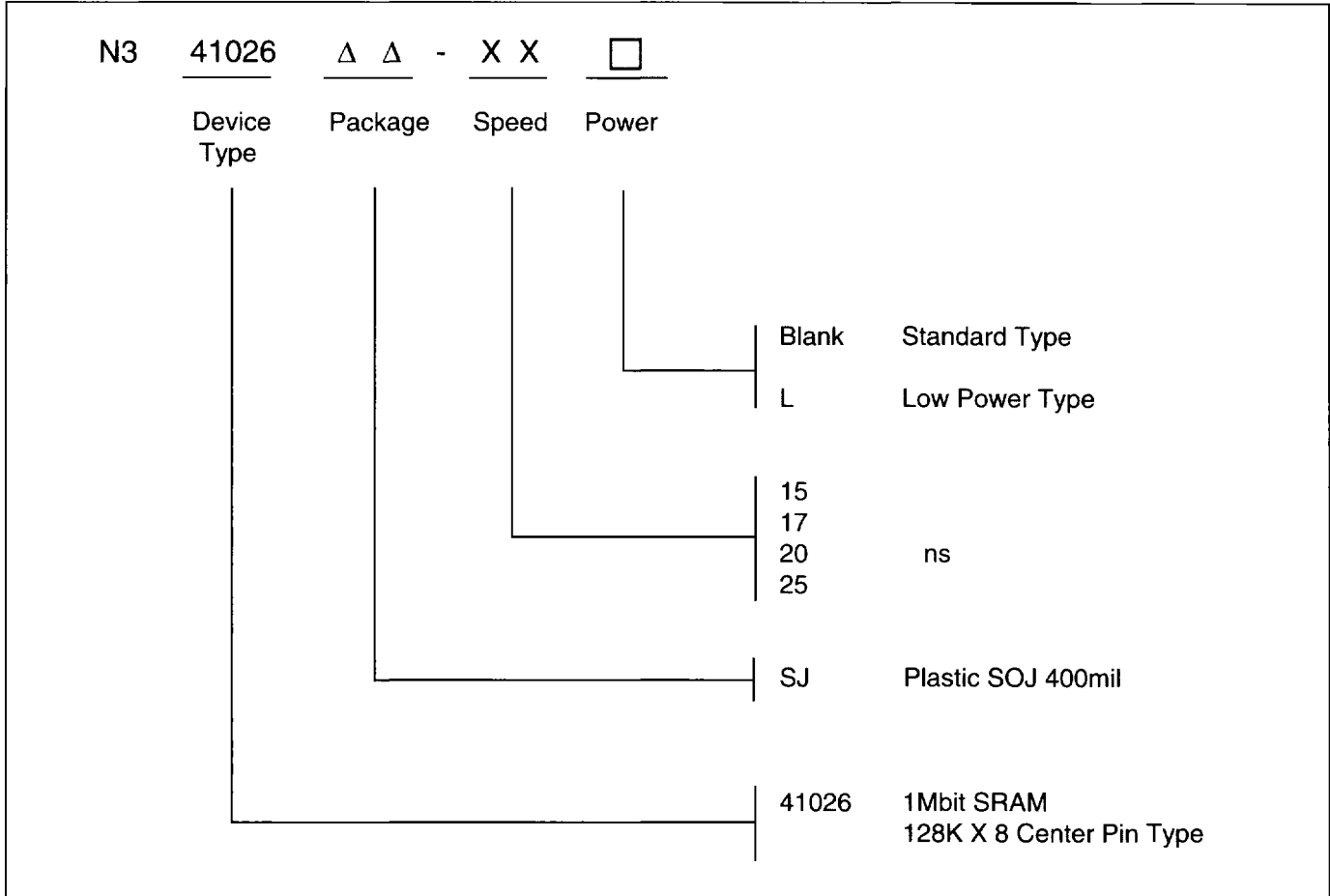
■ Data Retention Electrical Characteristics (Low Power type only)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDR	VCC for Retention data		2	-	-	V
ICCDR	Data retention current	$\overline{CE} \geq VCC-0.2V$ $V_{IN} \geq VCC-0.2V$ or $\leq 0.2V$				
		VCC = 2V	-	-	500	μA
		VCC = 3V	-	-	750	μA
tCDR	Chip deselect to data retention time		0	-	-	ns
tR	Operation recovery time		tRC	-	-	ns

Low VCC Data Retention Waveform



Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Power down Standby Current (mA)	Package
N341026SJ-15	15	185	55	32Pin Plastic SOJ
N341026SJ-17	17	165	50	32Pin Plastic SOJ
N341026SJ-20	20	155	45	32Pin Plastic SOJ
N341026SJ-25	25	145	40	32Pin Plastic SOJ
N341026SJ-15L	15	165	50	32Pin Plastic SOJ
N341026SJ-17L	17	155	45	32Pin Plastic SOJ
N341026SJ-20L	20	140	40	32Pin Plastic SOJ
N341026SJ-25L	25	135	35	32Pin Plastic SOJ