36Mb ZBT® SRAM

MT55L2MY18F, MT55V2MV18F, MT55L1MY32F, MT55V1MV32F, MT55L1MY36F, MT55V1MV36F

3.3V VDD, 3.3V or 2.5V I/O; 2.5V VDD, 2.5V I/O

Features

- High frequency and 100 percent bus utilization
- Single 3.3V ±5 percent or 2.5V ±5 percent power supply
- Separate 3.3V ±5 percent or 2.5V ±5 percent isolated output buffer supply (VDDQ)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin/ball
- CKE# pin/ball to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os, and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin and ball/function compatibility with 2Mb, 4Mb, 8Mb, and 18Mb ZBT SRAM
- Automatic power down

Options

	TQFP Marking
• Timing (Access/Cycle/MHz)	
6.5ns/8.8ns/113 MHz	-8.8
7.5ns/10ns/100 MHz	-10
8.5ns/11ns/90 MHz	-11
• Configurations	
3.3V VDD, 3.3V or 2.5V I/O	
2 Meg x 18	MT55L2MY18F
1 Meg x 32	MT55L1MY32F
1 Meg x 36	MT55L1MY36F
2.5V VDD, 2.5V I/O	
2 Meg x 18	MT55V2MV18F
1 Meg x 32	MT55V1MV32F
1 Meg x 36	MT55V1MV36F
• Packages	
100-pin, 16mm x 22.1mm TQFP	T
165-ball, 13mm x 15mm FBGA	F[1]
• Operating Temperature Range	
Commercial (0°C ≤ T_A ≤ +70°C)	None
Industrial (-40°C ≤ T_A ≤ +85°C)	IT[2]

NOTE:
1. A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/numberguide.
2. Contact factory for availability of Industrial Temperature devices.

Figure 1: 100-Pin TQFP
JEDEC-Standard MS-026 BHA (LQFP)

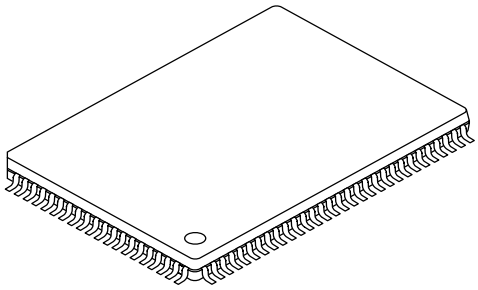
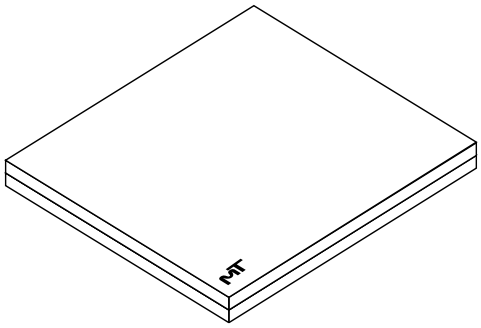


Figure 2: 165-Ball FBGA
JEDEC-Standard MO-216 (Var. CAB-1)



Part Number Example:

MT55L1MY36FT-11

General Description

The Micron® Zero Bus Turnaround™ (ZBT®) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 36Mb ZBT SRAMs integrate a 2 Meg x 18, 1 Meg x 32, or 1 Meg x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles for READ to WRITE, or WRITE to READ, transitions. All synchronous inputs pass through registers controlled

by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc#, and BWd#), and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin/ball (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE, and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the flow-through ZBT SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins/balls; BWb# controls DQb pins/balls; BWc# controls DQc pins/balls; and BWd# controls DQd pins/balls. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

Micron's 36Mb ZBT SRAMs operate from 3.3V or 2.5V V_{DD} power supply, and all inputs and outputs are LVTTL-compatible. Users can use either a 3.3V or 2.5V I/O, depending on the V_{DD} voltage. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

Dual Voltage I/O

The 3.3V V_{DD} device is tested for 3.3V and 2.5V I/O function. The 2.5V V_{DD} device is tested for only 2.5V I/O function.

Figure 3: Functional Block Diagram
2 Meg x 18

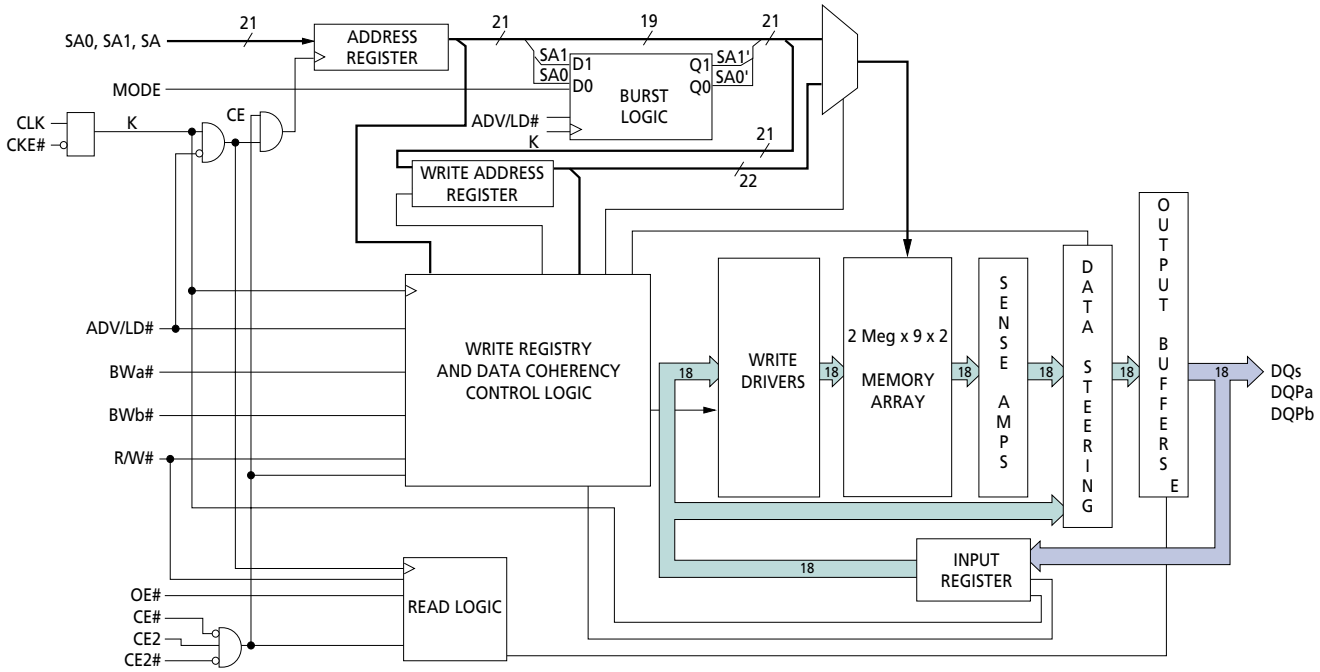
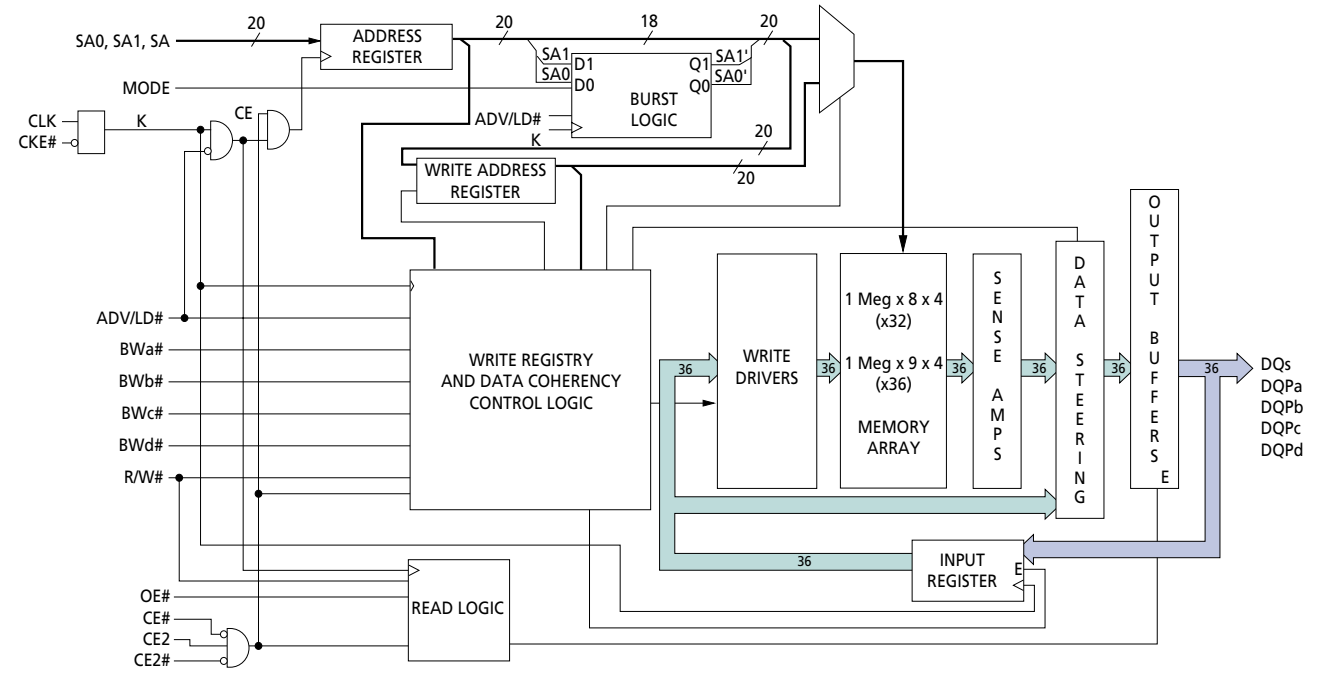
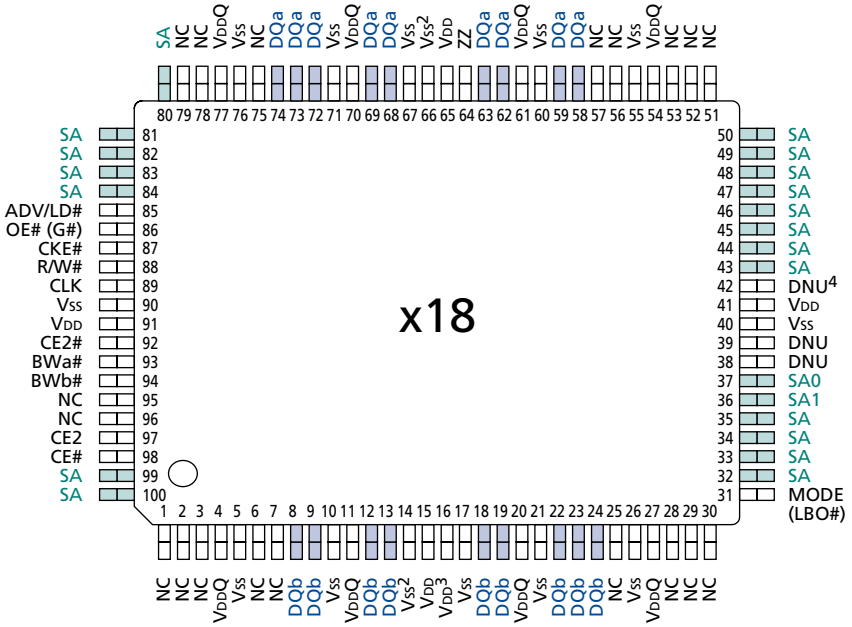


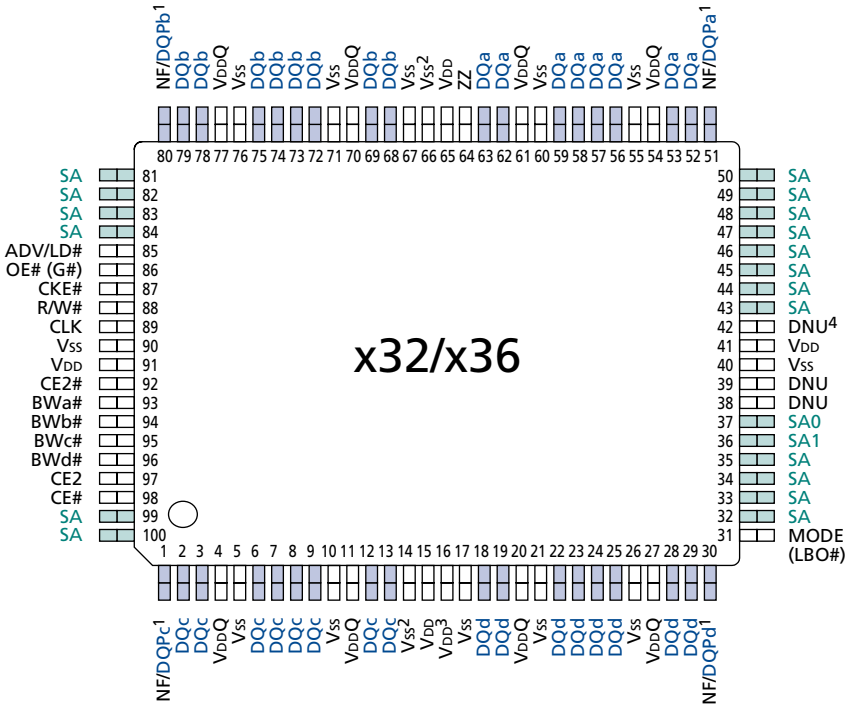
Figure 4: Functional Block Diagram
1 Meg x 32/36



NOTE:
Functional block diagrams illustrate simplified device operation. See truth tables, pin/ball descriptions, and timing diagrams for detailed information.

Figure 5: Pin Layout (Top View) 100-Pin TQFP





NOTE:
1. NF for x32 version, DQPx for x36 version.
2. Pins 14 and 66 do not have to be connected directly to VSS if another logic level can be applied that is ≤ VIL.
3. Pin 16 does not have to be connected directly to VDD if another logic level can be applied that is ≥ VIH.
4. Pin 42 isreserved for 72Mb address expansion.

Table 1: TQFP Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins. Parity is only available on the x18 and x36 versions.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: byte "a" is associated with DQa pins; byte "b" is associated with DQb pins; byte "c" is associated with DQc pins; byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge CLK.
MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This pin has an internal pull-down and can be left unconnected.
NF/DQPa NF/DQP NF/DQPc NF/DQPd	NF I/O	No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, byte "a" parity is DQPa; byte "b" parity is DQPb. On the x36 version, byte "a" parity is DQPa; byte "b" parity is DQPb; byte "c" parity is DQPc; byte "d" parity is DQPd. No Function pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.
V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

Table 1: TQFP Pin Descriptions (Continued)

SYMBOL	TYPE	DESCRIPTION
Vss	Supply	Ground: GND.
NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.

Figure 6: Ball Layout (Top View)
165-Ball FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	CKE#	ADV/LD#	SA	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	R/W#	OE# (G#)	SA	SA	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	VSS	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	NF	VSS	VSS	VDDQ	NC	NC
P	NC	NC[2]	SA	SA	TDI	SA1	TDO	SA	SA	SA	NF
R	MODE (LBO#)	SA	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	CKE#	ADV/LD#	SA	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	R/W#	OE# (G#)	SA	SA	NC
C	NF/DQPc[1]	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	NF/DQPb[1]
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	VSS	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	NF/DQPd[1]	NC	VDDQ	VSS	NC	NF	VSS	VSS	VDDQ	NC	NF/DQPa[1]
P	NC	NC[2]	SA	SA	TDI	SA1	TDO	SA	SA	SA	NF
R	MODE (LBO#)	SA	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

NOTE:
1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
2. Ball 2P is reserved for 72Mb address expansion.

Table 2: FBGA Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ingored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa balls and DQPa; BWb# controls DQb balls and DQPb. For the x32 and x36 versions, BWa# controls DQa balls and DQPa; BWb# controls DQb balls and DQPb; BWc# controls DQc balls and DQPc; BWd# controls DQd balls and DQPd. Parity is only available on the x18 and x36 versions.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded (ADV/LD# LOW).
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propogate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet the setup and hold times around the rising edge of CLK.
CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
MODE (LB0#)	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this ball permits BYTE WRITE operations to meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
TMS TDI TCK	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This ball has an internal pull-down and can be left unconnected.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, byte "a" is associated with DQa balls; byte "b" is associated with DQb balls. For the x32 and x36 versions, byte "a" is associated with DQa balls; byte "b" is associated with DQb balls; byte "c" is associated with DQc balls; byte "d" is associated with DQd balls. Input data must meet setup and hold times around the rising edge of CLK.

Table 2: FBGA Ball Descriptions (Continued)

SYMBOL	TYPE	DESCRIPTION
NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF I/O	No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, byte "a" parity is DQPa; byte "b" parity is DQPb. On the x36 version, byte "a" parity is DQPa; byte "b" parity is DQPb; byte "c" parity is DQPc; byte "d" parity is DQPd. No Function balls are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these balls unconnected or driven by signals.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
V_{SS}	Supply	Ground: GND.
NC	—	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

Table 3: Interleaved Burst Address Table (Mode = NC or HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

Table 4: Linear Burst Address Table (Mode = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

Table 5: Partial Truth Table for READ/WRITE Commands (x18)

FUNCTION	R/W#	BWa#	BWb#
READ	H	X	X
WRITE Byte “a”	L	L	H
WRITE Byte “b”	L	H	L
WRITE All Byte	L	L	L
WRITE ABORT/NOP	L	H	H

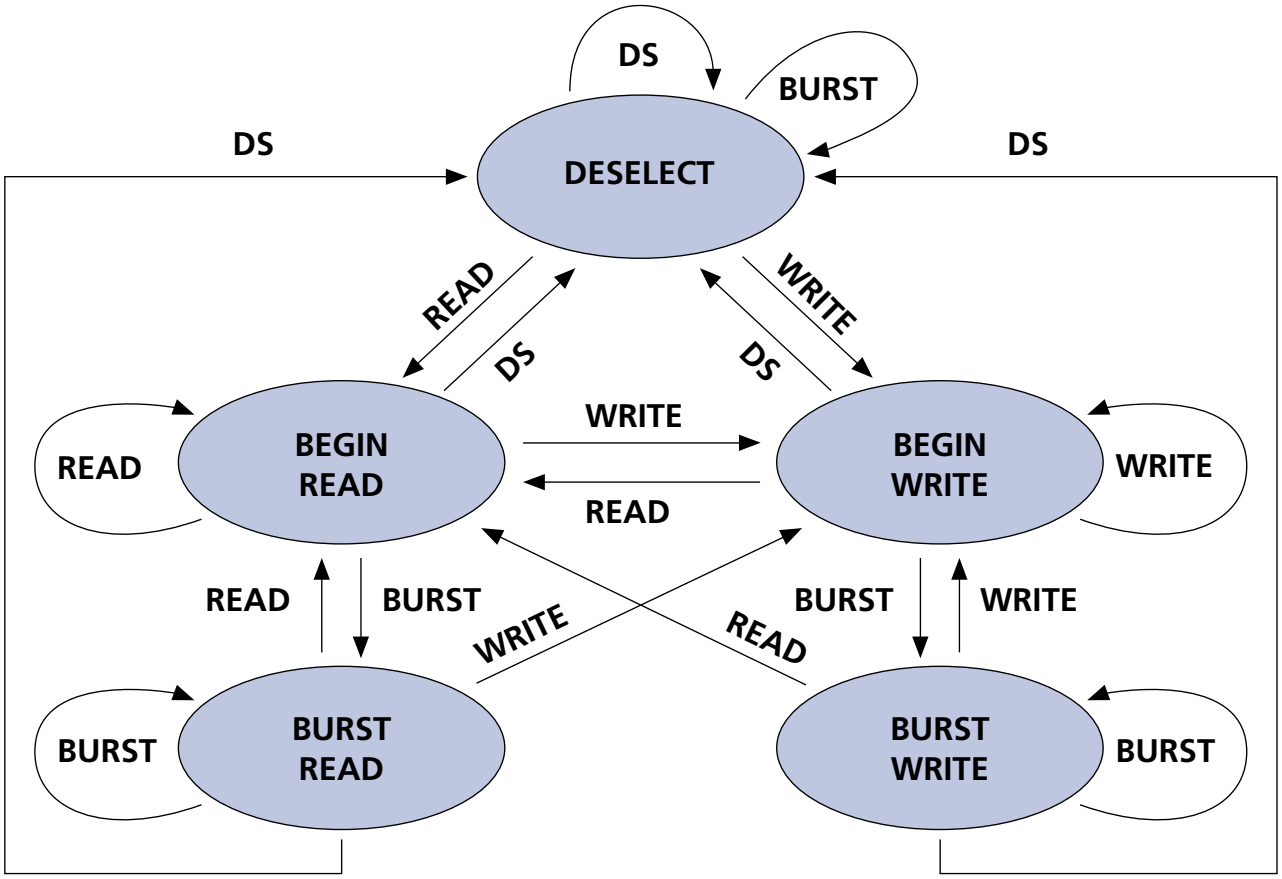
NOTE:
Using R/W# and byte write(s), any one or more bytes may be written.

Table 6: Partial Truth Table for READ/WRITE Commands (x32/x36)

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
READ	H	X	X	X	X
WRITE Byte “a”	L	L	H	H	H
WRITE Byte “b”	L	H	L	H	H
WRITE Byte “c”	L	H	H	L	H
WRITE Byte “d”	L	H	H	H	L
WRITE All Byte	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

NOTE:
Using R/W# and byte write(s), any one or more bytes may be written.

Figure 7:
State Diagram For ZBT SRAM



KEY:	COMMAND	OPERATION
	DS	DESELECT
	READ	New READ
	WRITE	New WRITE
	BURST	BURST READ, BURST WRITE, or CONTINUE DESELECT

NOTE:
1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK).

Table 7: Truth Table

Notes: 5–10

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADV/ LD#	R/W#	BWx	OE#	CKE#	CLK	DQ	NOTES
DESELECT CYCLE	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT Cycle	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
CONTINUE DESELECT Cycle	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	1
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	1, 11
NOP/DUMMY READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	2
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	1, 2, 11
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	3
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	1, 3, 11
NOP/WRITE ABORT (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	2, 3
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	1, 2, 3, 11
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	–	4
SNOOZE MODE	None	X	X	X	H	X	X	X	X	X	X	High-Z	

NOTE:

1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A Continue DESELECT cycle can only be entered if a DESELECT cycle is executed first.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. OE# may be used when the bus turn-on and turn-off times do not meet an application's requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWa#, BWb#, BWc#, and BWd#) are HIGH. BWx = L means one or more byte write signals are LOW.
6. BWa# enables WRITEs to byte "a" (DQa pins/balls); BWb# enables WRITEs to byte "b" (DQb pins/balls); BWc# enables WRITEs to byte "c" (DQc pins/balls); BWd# enables WRITEs to byte "d" (DQd pins/balls).
7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE# HIGH.
9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST CYCLE.
11. The address counter is incremented for all CONTINUE BURST CYCLES.

Absolute Maximum Ratings

3.3V VDD

Voltage on VDD Supply
Relative to VSS . . . . . -0.5V to +4.6V
Voltage on VDDQ Supply
Relative to VSS . . . . . -0.5V to VDD
VIN (DQs) . . . . . -0.5V to VDDQ + 0.5V
VIN (Inputs) . . . . . -0.5V to VDD + 0.5V
Storage Temperature (TQFP) . . . . . -55°C to +150°C
Storage Temperature (FBGA) . . . . . -55°C to +125°C
Junction Temperature . . . . . +150°C
Short Circuit Output Current 100mA

2.5V VDD

Voltage on VDD Supply
Relative to VSS . . . . . -0.3V to +3.6V
Voltage on VDDQ Supply Relative
to VSS . . . . . -0.3V to +3.6V
VIN (DQs) . . . . . -0.3V to VDDQ + 0.3V
VIN (Inputs) . . . . . -0.3V to VDD + 0.3V
Storage Temperature (TQFP) . . . . . -55°C to +150°C
Storage Temperature (FBGA) . . . . . -55°C to +125°C
Junction Temperature . . . . . +150°C
Short Circuit Output Current 100mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

Table 8: 3.3V VDD, 3.3V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; VDD and VDDQ = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4		V	1, 5
Output Low Voltage	IOL = 8.0mA	VOL		0.4	V	1, 5
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	3.135	VDD	V	1, 6

Table 9: 3.3V V_{DD}, 2.5V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; V_{DD} = 3.3V ±0.165V and $V_{DD}Q$ = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQ_X)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1, 5
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1, 5
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1, 5
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1, 5
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.625	V	1, 6

Table 10: 2.5V V_{DD}, 2.5V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; V_{DD} and $V_{DD}Q$ = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 3
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 3
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 3
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQ_X)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1, 5
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1, 5
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1, 5
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1, 5
Supply Voltage		V_{DD}	2.375	2.625	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.625	V	1, 6

Table 11: TQFP Capacitance

Note 11; notes appear following parameter tables on page 18

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Control Input Capacitance	T_A = 25°C; f = 1 MHz V_{DD} = 3.3V	C_I	4.2	5	pF
Input/Output Capacitance (DQ)		C_O	3.5	4	pF
Address Capacitance		C_A	4	5	pF
Clock Capacitance		C_{CK}	4.2	5	pF

Table 12: FBGA Capacitance

Note 11; notes appear following parameter tables on page 18

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	4	5	pF
Output Capacitance (Q)		C_O	4	4.5	pF
Clock Capacitance		C_{CK}	5	5.5	pF

Table 13: TQFP Thermal Resistance

Note 11; notes appear following parameter tables on page 18

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	TBD	°C/W
Thermal Resistance (Junction to Top of Case)		θ_{JC}	TBD	°C/W

Table 14: FBGA Thermal Resistance

Note 11; notes appear following parameter tables on page 18

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	TBD	°C/W
Junction to Case (Top)		θ_{JC}	TBD	°C/W
Junction to Balls (Bottom)		θ_{JB}	TBD	°C/W

Table 15: 3.3V VDD, IDD Operating Conditions and Maximum Limits (2 Meg x 18 and 1 Meg x 32/36)

Notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V and VDDQ = 3.3V ±0.165V or 2.5V ±0.125V unless otherwise noted

				MAX				
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-8.8**	**-10**	**-11**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	300	280	260	mA	7, 8, 9
Power Supply Current: Idle	Device selected; VDD = MAX; CKE# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	115	110	100	mA	7, 8, 9
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	mA	8, 9
Clock Running	Device deselected; VDD = MAX; ADV/LD# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	ISB4	TBD	115	110	100	mA	8, 9
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	mA	9

Table 16: 2.5V VDD, IDD Operating Conditions and Maximum Limits (2 Meg x 18 and 1 Meg x 32/36)

Notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V and VDDQ = 3.3V ±0.165V or 2.5V ±0.125V unless otherwise noted

				MAX				
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-8.8**	**-10**	**-11**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	265	255	230	mA	7, 8, 10
Power Supply Current: Idle	Device selected; VDD = MAX; CKE# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	75	70	55	mA	7, 8, 10
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	mA	7, 8, 10
Clock Running	Device deselected; VDD = MAX; ADV/LD# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	ISB4	TBD	75	70	55	mA	7, 8, 10
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	mA	10

Table 17: AC Electrical Characteristics and Recommended Operating Conditions

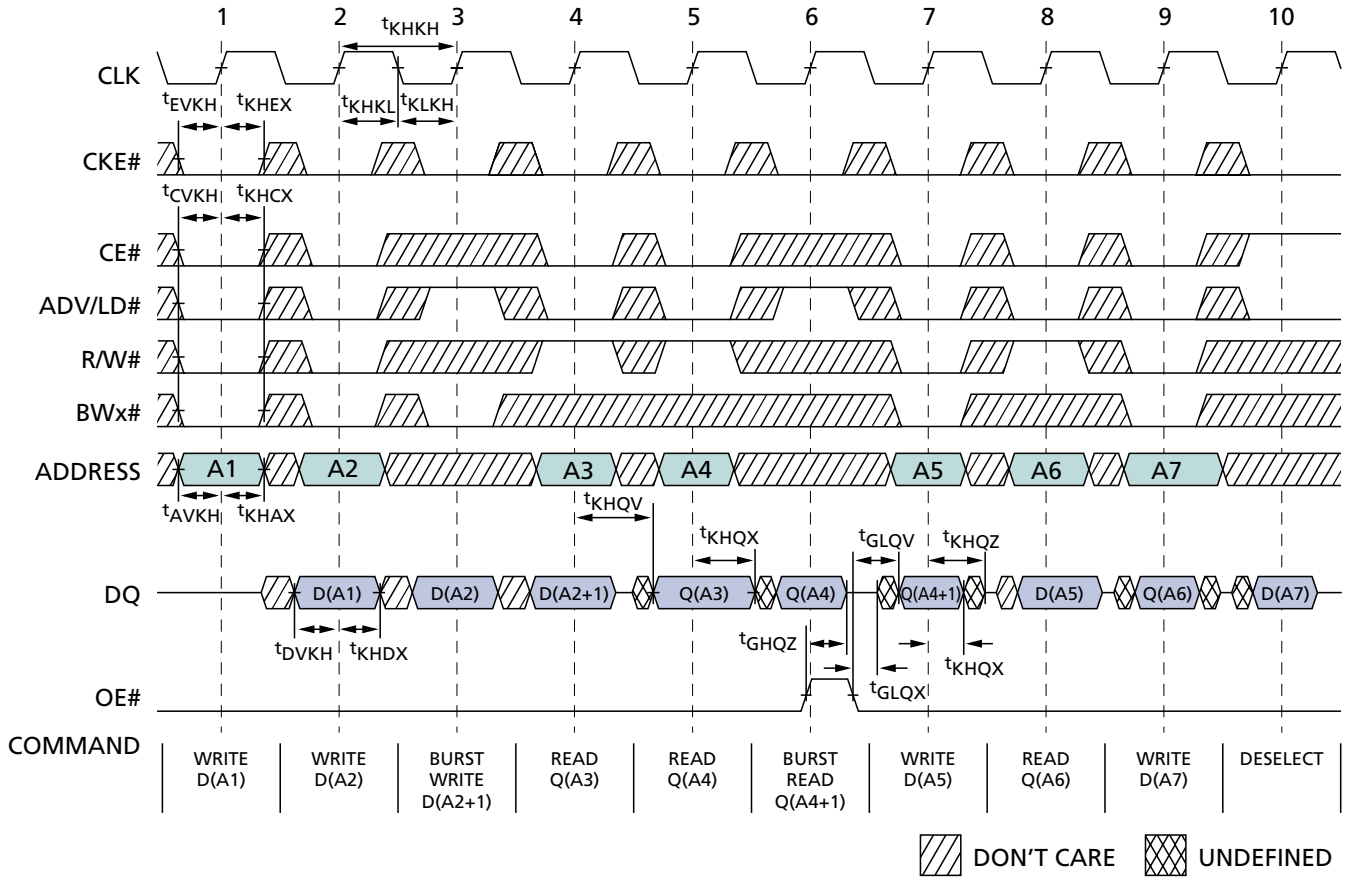
Notes 12-14 ; notes appear following parameter tables on page 18; 0°C ≤ T_A ≤ +70°C; V_{DD} = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	SYMBOL	-8.8		-10		-11		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	^tKHKH	8.8		10.0		11.0		ns	
Clock frequency	^fKF		113		100		90	MHz	
Clock HIGH time	^tKHKL	2.5		2.5		3.0		ns	15
Clock LOW time	^tKLKH	2.5		2.5		3.0		ns	15
Output Times									
Clock to output valid	^tKHQV		6.5		7.5		8.5	ns	
Clock to output invalid	^tKHQX	2.5		3.0		3.0		ns	16
Clock to output in Low-Z	^tKHQX	2.5		3.0		3.0		ns	11, 16, 17
Clock to output in High-Z	^tKHQZ		4.0		5.0		5.0	ns	11, 16, 17
OE# to output valid	^tGLQV		3.5		4.0		5.0	ns	12
OE# to output in Low-Z	^tGLQX	0		0		0		ns	11, 16, 17
OE# to output in High-Z	^tGHQZ		3.5		4.0		5.0	ns	11, 16, 17
Setup Times									
Address	^tAVKH	2.0		2.0		2.0		ns	18
Clock enable (CKE#)	^tEVKH	2.0		2.0		2.0		ns	18
Control signals	^tCVKH	2.0		2.0		2.0		ns	18
Data-in	^tDVKH	2.0		2.0		2.0		ns	18
Hold Times									
Address	^tKHAX	0.5		0.5		0.5		ns	18
Clock enable (CKE#)	^tKHEX	0.5		0.5		0.5		ns	18
Control signals	^tKHCX	0.5		0.5		0.5		ns	18
Data-in	^tKHDX	0.5		0.5		0.5		ns	18

Notes

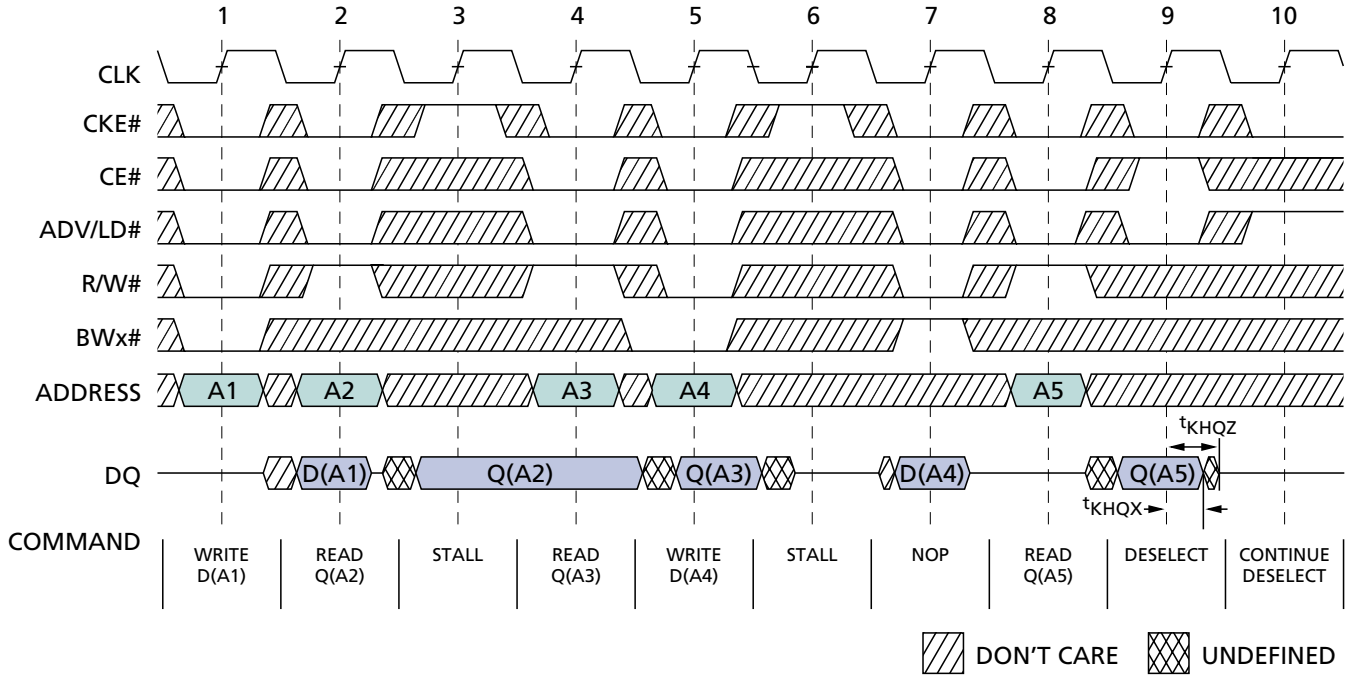
1. All voltages referenced to V_{SS} (GND).
2. For 3.3V V_{DD}:
   Overshoot: $V_{IH} \leq +4.6V$ for $t \leq {}^{t}KHKH/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.7V$ for $t \leq {}^{t}KHKH/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +3.6V$ and $V_{DD} \leq 3.135V$ for $t \leq 200ms$
3. For 2.5V V_{DD}:
   Overshoot: $V_{IH} \leq +3.6V$ for $t \leq {}^{t}KHKH/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.5V$ for $t \leq {}^{t}KHKH/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +2.65V$ and $V_{DD} \leq 2.375V$ for $t \leq 200ms$
4. The MODE pin/ball has an internal pull-up, and input leakage = ±10µA.
5. The load used for V_{OH}, V_{OL} testing is shown in Figures 11 and 12 for 3.3V I/O and Figures 13 and 14 for 2.5V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be externally wired together to the same power supply.
7. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
8. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
9. Typical values are measured at 3.3V, 25°C, and 12ns cycle time.
10. Typical values are measured at 2.5V, 25°C, and 12ns cycle time.
11. This parameter is sampled.
12. OE# can be considered a "Don't Care" during WRITEs; however, controlling OE# can help fine-tune a system for turnaround timing.
13. Test conditions as specified with the output loading shown in Figures 11 and 12 for 3.3V I/O and Figures 13 and 14 for 2.5V I/O unless otherwise noted.
14. A WRITE cycle is defined by R/W# LOW, having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.
15. Measured as HIGH above V_{IH} and LOW below V_{IL}.
16. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion of these parameters.
17. This parameter is measured with the output loading shown in Figure 12 for 3.3V I/O and Figure 14 for 2.5V I/O.
18. This is a synchronous device. All addresses must meet the specified setup and hold times with stable logic levels for all rising edges of CLK when the chip is enabled. To remain enabled, chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW.

Figure 8:
READ/WRITE Timing



NOTE:
1. For these waveforms, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

Figure 9:
NOP, STALL, AND DESELECT Cycles



NOTE:
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
2. For these waveforms, ZZ and OE# are tied LOW.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

SNOOZE MODE

SNOOZE MODE is a low-current, power-down mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

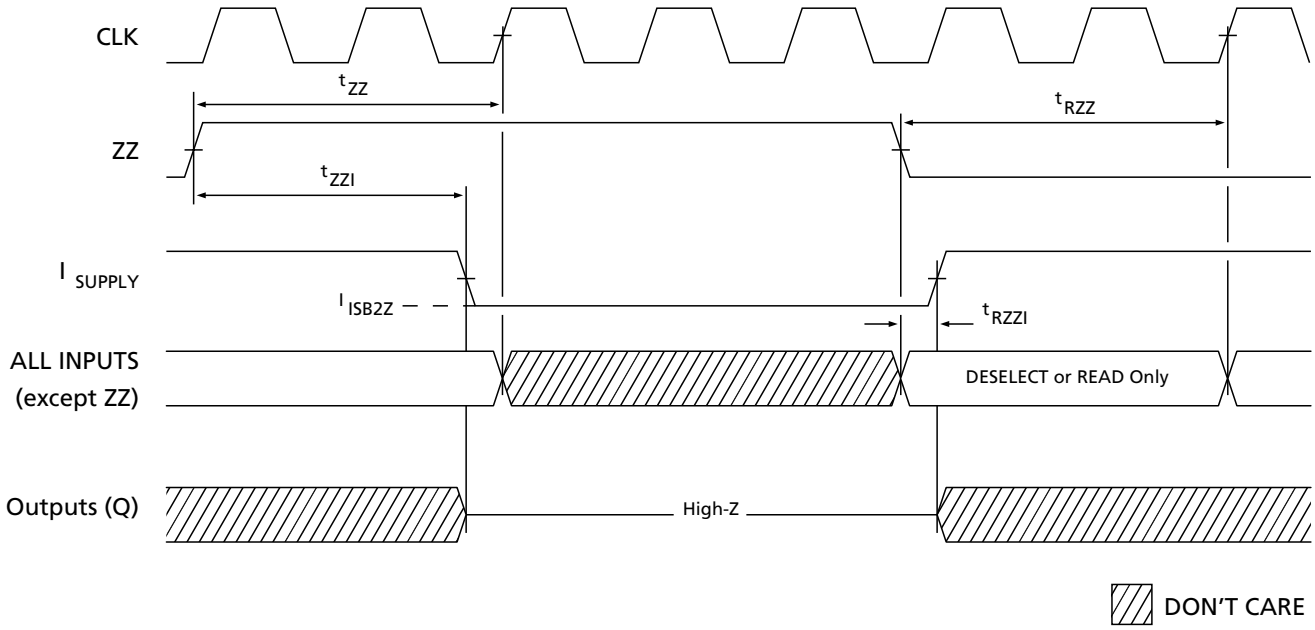
The ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the time ^{t}ZZI is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during ^{t}RZZ, only a DESELECT or READ cycle should be given.

Table 18: SNOOZE MODE Electrical Characteristics

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		30	mA	
ZZ active to input ignored		^{t}ZZ		$^{t}KHKH$	ns	1
ZZ inactive to input sampled		^{t}RZZ	$^{t}KHKH$		ns	1
ZZ active to snooze current		^{t}ZZI		$^{t}KHKH$	ns	1
ZZ inactive to exit snooze current		$^{t}RZZI$	0		ns	1

NOTE:
1. This parameter is sampled.

Figure 10: SNOOZE MODE Waveform



3.3V VDD, 3.3V I/O AC Test Conditions

Input pulse levels ..... VIH = (VDD/2.2) + 1.5V
..... VIL = (VDD/2.2) - 1.5V
Input rise and fall times 1ns
Input timing reference levels.....VDD/2.2
Output reference levels.....VDDQ/2.2
Output load..... See Figures 11 and 12

3.3V VDD, 2.5V I/O AC Test Conditions

Input pulse levels .....VIH = (VDD/2.64) + 1.25V
..... VIL = (VDD/2.64) - 1.25V
Input rise and fall times 1ns
Input timing reference levels.....VDD/2.64
Output reference levels.....VDDQ/2
Output load..... See Figures 13 and 14

2.5V VDD, 2.5V I/O AC Test Conditions

Input pulse levels .....VIH = (VDD/2) + 1.25V
..... VIL = (VDD/2) - 1.25V
Input rise and fall times 1ns
Input timing reference levels.....VDD/2
Output reference levels.....VDDQ/2
Output load..... See Figures 13 and 14

Load Derating Curves

Micron 2 Meg x 18, 1 Meg x 32, and 1 Meg x 36 ZBT SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

3.3V I/O Output Load Equivalents

Figure 11:

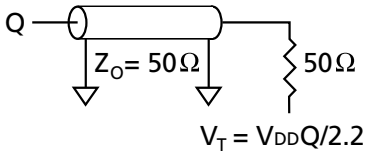
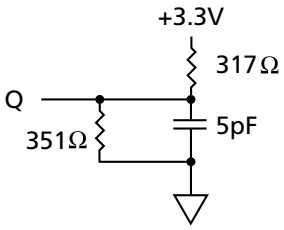


Figure 12:



2.5V I/O Output Load Equivalents

Figure 13:

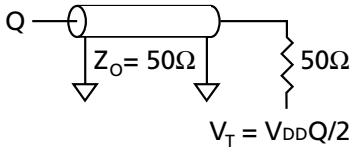
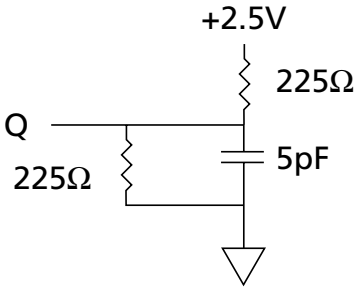


Figure 14:



IEEE 1149.1 Serial Boundary Scan (JTAG)

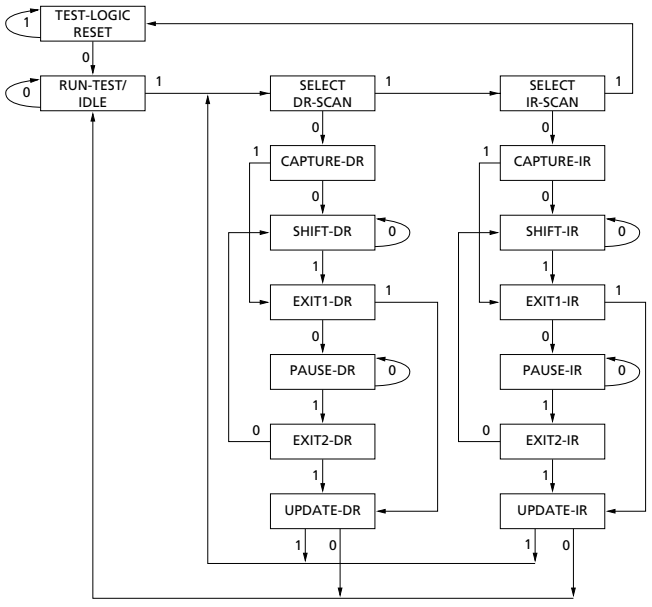
The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

These balls can be left floating (unconnected), if the JTAG function is not to be implemented. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Figure 15: TAP Controller State Diagram



NOTE:
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (Tap)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

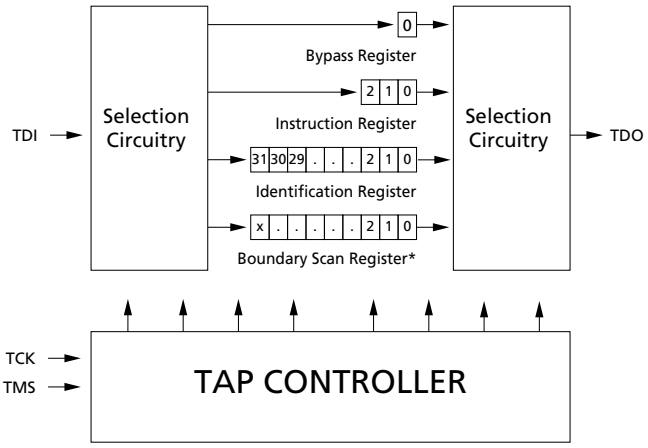
Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 16.)

Figure 16: TAP Controller Block Diagram



NOTE:
X = 75 for all configurations.

Test Data-Out (TDO)

The TDO outputball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 15.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 16.)

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in Figure 16. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The SRAM has a 76-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins/balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 17:
TAP Timing

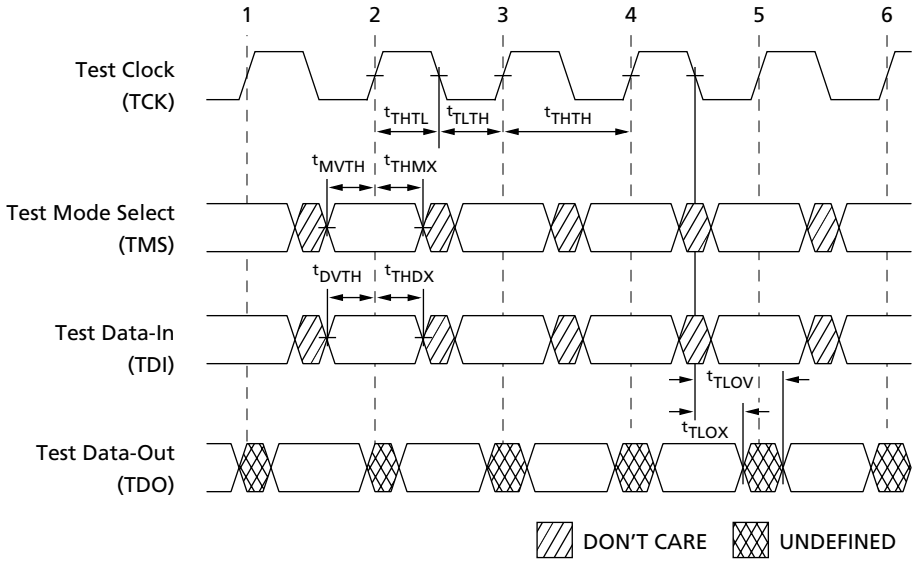


Table 19: TAP AC Electrical Characteristics

Notes 1, 2; 0°C ≤ T_A ≤ +70°C; V_{DD} = 3.3V ±0.165V or 2.5V ±0.125V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE:
1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 18.

TAP AC Test Conditions

Input Pulse Levels .....Vss to 2.5V
Input rise and fall times 1ns
Input timing reference levels.....1.25V
Output reference levels.....1.25V
Test load termination supply voltage 1.25V

Figure 18: TAP AC Output Load Equivalent

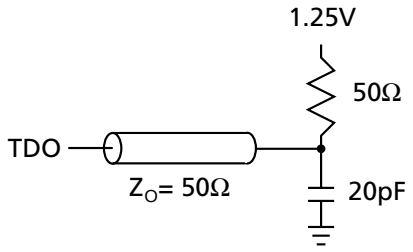


Table 20: 3.3V VDD, TAP DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.7	V	1
	IOLT = 2mA	VOL2		0.8	V	1
Output High Voltage	IOHC = -100µA	VOH1	2.9		V	1
	IOHT = -2mA	VOH2	2.0		V	1

Table 21: 2.5V VDD, TAP DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1
	IOLT = 2mA	VOL2		0.7	V	1
Output High Voltage	IOHC = -100µA	VOH1	2.1		V	1
	IOHT = -2mA	VOH2	1.7		V	1

NOTE:
1. All voltages referenced to VSS (GND).
2. Overshoot: VIH (AC) ≤ VDD + 1.5V for t ≤ ^{t}KHKH/2
   Undershoot:VIL (AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ +2.6V and VDD ≤ 2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals (LD#, R/W#, etc.) may not have pulse widths less than ^{t}KHKL (MIN) or operate at frequencies exceeding ^{f}KF (MAX).

Table 22: Identification Register Definitions

INSTRUCTION FIELD	BIT CONFIGURATION	DESCRIPTION
Revision Number (31:28)	0000	Reserved for version number.
Device Depth (27:23)	01000 00111	Defines depth of 2Mb. Defines depth of 1Mb.
Device Width (22:18)	00011 00100	Defines width of x18 bits. Defines width of x32 or x36 bits.
Micron Device ID (17:12)	xxxxxx	Reserved for future use.
Micron JEDEC ID Code (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 23: Scan Register Sizes

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan: x18, x32, x36	76

Table 24: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Table 25: 165-Ball FBGA Boundary Scan Order (x18)

BIT#	SIGNAL NAME	BALL ID
1	NF	11P
2	SA	2R
3	SA	8R
4	SA	8P
5	SA	9R
6	SA	9P
7	SA	10R
8	SA	10P
9	NF	6N
10	ZZ	11H
11	NC	11N
12	NC	11M
13	NC	11L
14	NC	11K
15	NC	11J
16	DQa	10M
17	DQa	10L
18	DQa	10K
19	DQa	10J
20	DQa	11G
21	DQa	11F
22	DQa	11E
23	DQa	11D
24	DQPa	11C
25	NC	10G
26	NC	10F
27	NC	10E
28	NC	10D
29	SA	11A
30	NC	11B
31	SA	10B
32	SA	10A
33	SA	9A
34	SA	9B
35	ADV/LD#	8A
36	OE#	8B
37	CKE#	7A
38	R/W#	7B

BIT#	SIGNAL NAME	BALL ID
39	CLK	6B
40	CE2#	6A
41	BW1#	5B
42	NC	5A
43	BW2#	4A
44	NC	4B
45	CE2	3B
46	CE#	3A
47	SA	2A
48	SA	2B
49	NC	1B
50	NC	1A
51	NC	1C
52	NC	1D
53	NC	1E
54	NC	1F
55	NC	1G
56	DQb	2D
57	DQb	2E
58	DQb	2F
59	DQb	2G
60	DQb	1J
61	DQb	1K
62	DQb	1L
63	DQb	1M
64	DQPb	1N
65	NC	2H
66	NC	2K
67	NC	2L
68	NC	2M
69	SA	11R
70	MODE (LBO#)	1R
71	SA	3P
72	SA	3R
73	SA	4P
74	SA	4R
75	SA1	6P
76	SA0	6R

Table 26: 165-Ball FBGA Boundary Scan Order (x32)

BIT#	SIGNAL NAME	BALL ID
1	NF	11P
2	SA	2R
3	SA	8R
4	SA	8P
5	SA	9R
6	SA	9P
7	SA	10R
8	SA	10P
9	NF	6N
10	ZZ	11H
11	NF	11N
12	DQa	11M
13	DQa	11L
14	DQa	11K
15	DQa	11J
16	DQa	10M
17	DQa	10L
18	DQa	10K
19	DQa	10J
20	DQb	11G
21	DQb	11F
22	DQb	11E
23	DQb	11D
24	DQb	10G
25	DQb	10F
26	DQb	10E
27	DQb	10D
28	NF	11C
29	NC	11A
30	NC	11B
31	SA	10B
32	SA	10A
33	SA	9A
34	SA	9B
35	ADV/LD#	8A
36	OE#	8B
37	CKE#	7A
38	R/W#	7B

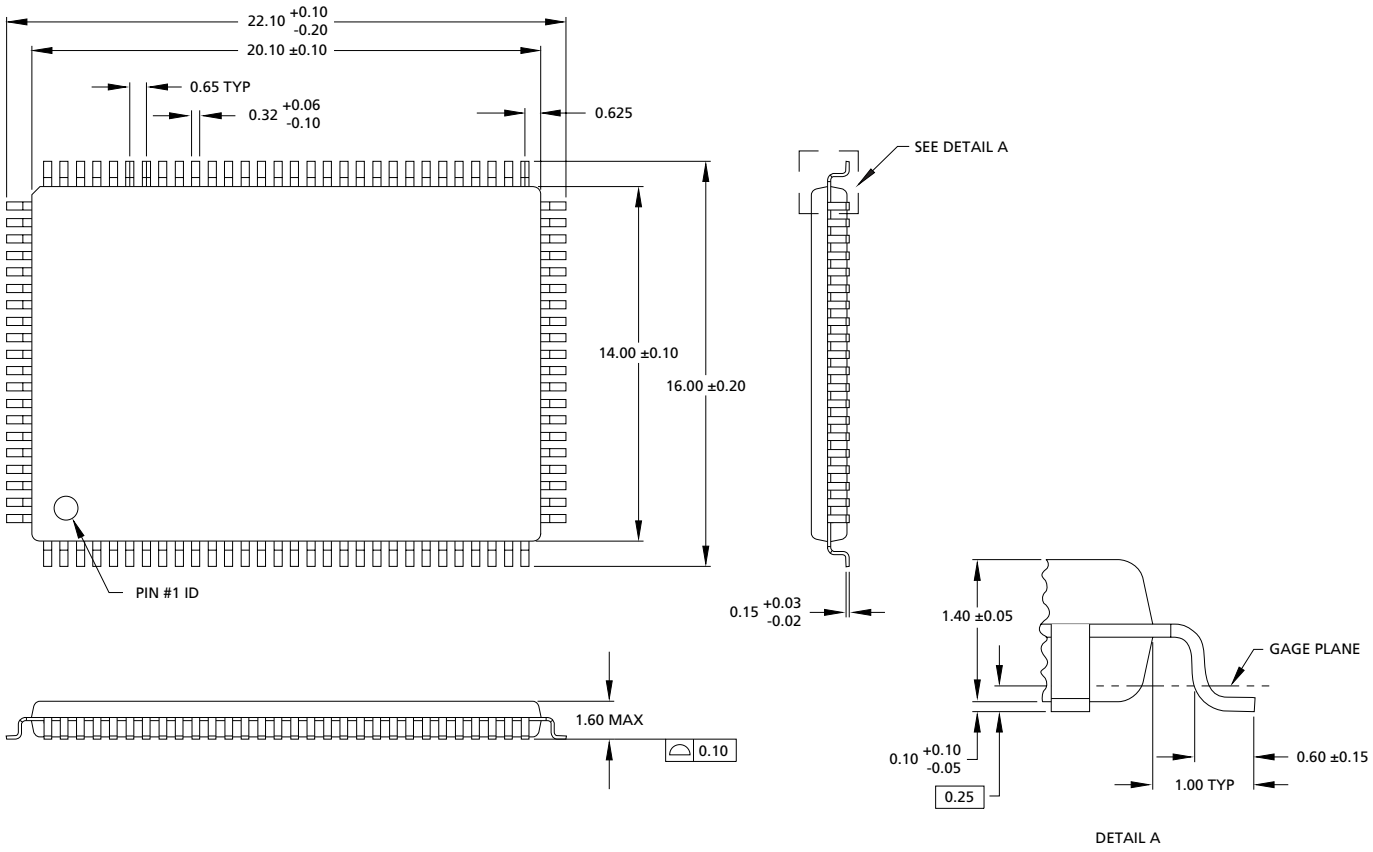
BIT#	SIGNAL NAME	BALL ID
39	CLK	6B
40	CE2#	6A
41	BW1#	5B
42	BW2#	5A
43	BW3#	4A
44	BW4#	4B
45	CE2	3B
46	CE#	3A
47	SA	2A
48	SA	2B
49	NC	1B
50	NC	1A
51	NF	1C
52	DQc	1D
53	DQc	1E
54	DQc	1F
55	DQc	1G
56	DQc	2D
57	DQc	2E
58	DQc	2F
59	DQc	2G
60	DQc	1J
61	DQd	1K
62	DQd	1L
63	DQd	1M
64	DQd	2J
65	DQd	2K
66	DQd	2L
67	DQd	2M
68	NF	1N
69	SA	11R
70	MODE (LBO#)	1R
71	SA	3P
72	SA	3R
73	SA	4P
74	SA	4R
75	SA1	6P
76	SA0	6R

Table 27: 165-Ball FBGA Boundary Scan Order (x36)

BIT#	SIGNAL NAME	BALL ID
1	NF	11P
2	SA	2R
3	SA	8R
4	SA	8P
5	SA	9R
6	SA	9P
7	SA	10R
8	SA	10P
9	NF	6N
10	ZZ	11H
11	DQPa	11N
12	DQa	11M
13	DQa	11L
14	DQa	11K
15	DQa	11J
16	DQa	10M
17	DQa	10L
18	DQa	10K
19	DQa	10J
20	DQb	11G
21	DQb	11F
22	DQb	11E
23	DQb	11D
24	DQb	10G
25	DQb	10F
26	DQb	10E
27	DQb	10D
28	DQPb	11C
29	NC	11A
30	NC	11B
31	SA	10B
32	SA	10A
33	SA	9A
34	SA	9B
35	ADV/LD#	8A
36	OE#	8B
37	CKE#	7A
38	R/W#	7B

BIT#	SIGNAL NAME	BALL ID
39	CLK	6B
40	CE2#	6A
41	BW1#	5B
42	BW2#	5A
43	BW3#	4A
44	BW4#	4B
45	CE2	3B
46	CE#	3A
47	SA	2A
48	SA	2B
49	NC	1B
50	NC	1A
51	DQPc	1C
52	DQc	1D
53	DQc	1E
54	DQc	1F
55	DQc	1G
56	DQc	2D
57	DQc	2E
58	DQc	2F
59	DQc	2G
60	DQd	1J
61	DQd	1K
62	DQd	1L
63	DQd	1M
64	DQd	2J
65	DQd	2K
66	DQd	2L
67	DQd	2M
68	DQPd	1N
69	SA	11R
70	MODE (LBO#)	1R
71	SA	3P
72	SA	3R
73	SA	4P
74	SA	4R
75	SA1	6P
76	SA0	6R

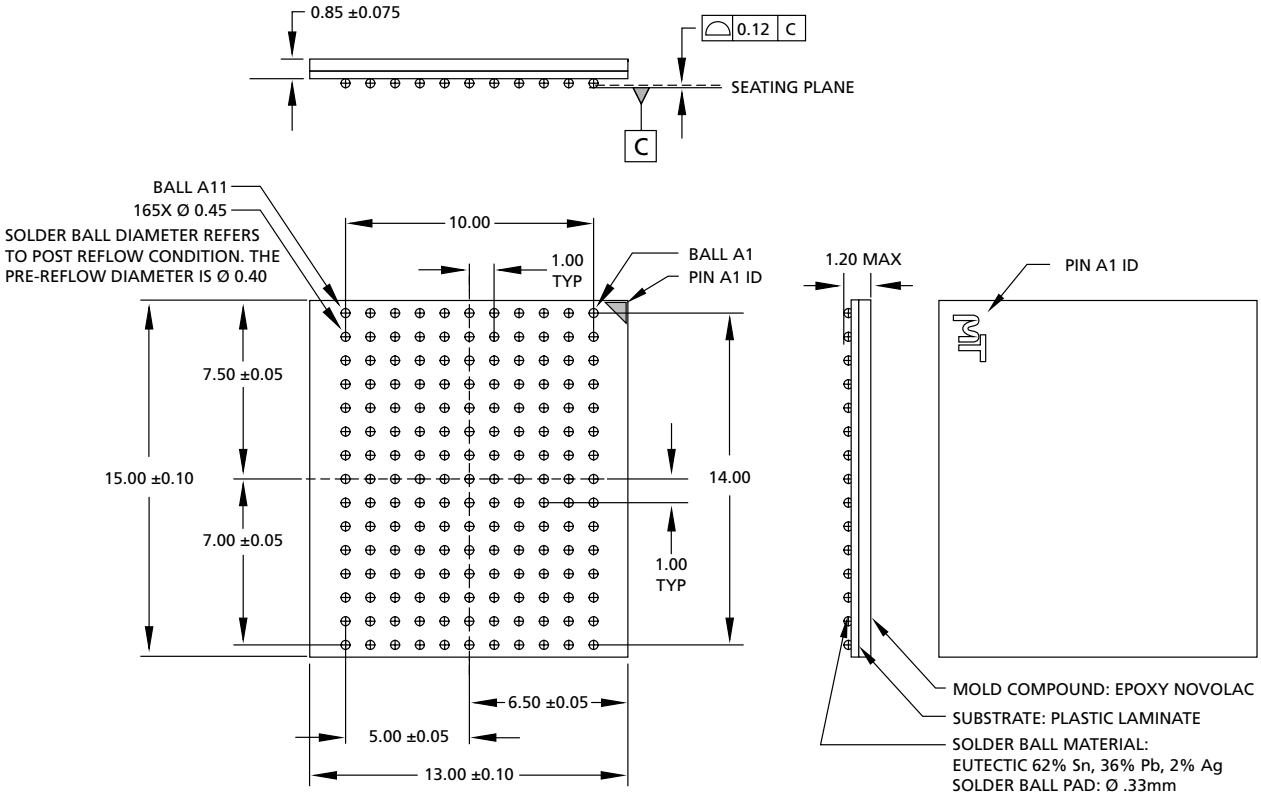
Figure 19: 100-Pin Plastic TQFP (JEDEC LQFP)



NOTE:

1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Figure 20:
165-Ball FBGA



NOTE:

1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Advance: This data sheet contains initial descriptions of products still under development.

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Revision History

- Revised FBGA dimensions for 165-ball FBGA 1/03
- New ADVANCE data sheet for 0.13µm process; Rev A; Pub. 11/02 ..... 11/02