

Document Title

256Kx18-Bit Synchronous Burst SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	May. 15. 1997	Preliminary
0.1	Modify power down cycle timing & Interleaved read timing, Insert Note 4 at AC timing characteristics. Change I _{SB1} value from 10mA to 30mA. Change I _{SB2} value from 10mA to 20mA.	February. 11. 1998	Preliminary
0.2	Change Undershoot spec from -3.0V(pulse width≤20ns) to -2.0V(pulse width≤tc _{yc} /2) Add Overshoot spec 4.6V((pulse width≤tc _{yc} /2) Change V _{IH} max from 5.5V to V _{DD} +0.5V	April. 14. 1998	Preliminary
0.3	Change I _{SB2} value from 20mA to 30mA. Change V _{DD} condition from V _{DD} =3.3V+10%/-5% to V _{DD} =3.3V+0.3V/-0.165V.	May 13. 1998	Preliminary
1.0	Final spec Release	May 15. 1998	Final
2.0	Add V _{DDQ} Supply voltage(2.5V)	Dec. 02. 1998	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

256Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V \pm 0.3V / -0.165V$ Power Supply.
- V_{DDQ} Supply Voltage $3.3V \pm 0.3V / -0.165V$ for 3.3V I/O or $2.5V \pm 0.4V / -0.125V$ for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

FAST ACCESS TIMES

PARAMETER	Symbol	-75	-80	-90	Unit
Cycle Time	t_{CYC}	8.5	10	12	ns
Clock Access Time	t_{CD}	7.5	8	9	ns
Output Enable Access Time	t_{OE}	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B401825M is a 4,718,592 bit Synchronous Static Random Access Memory designed for support zero wait state performance for advanced Pentium/Power PC address pipelining. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signal.

It is organized as 256K words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementation of high performance cache RAM applications.

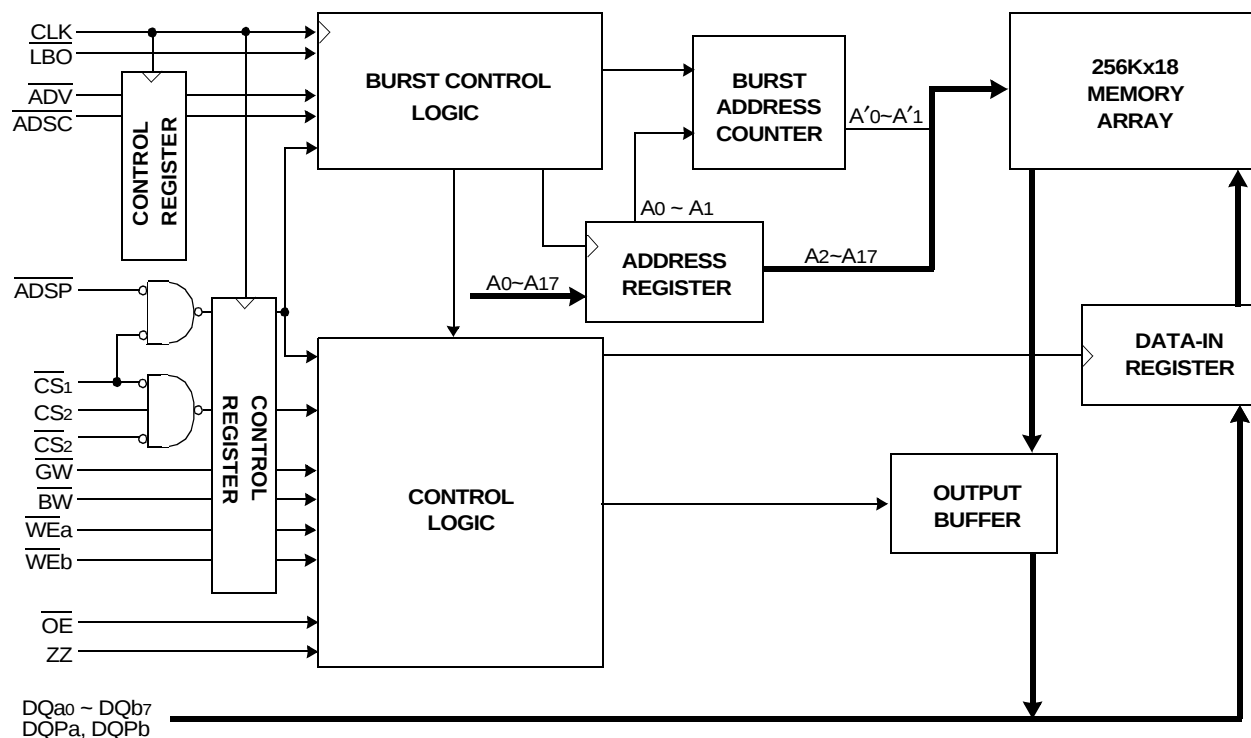
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

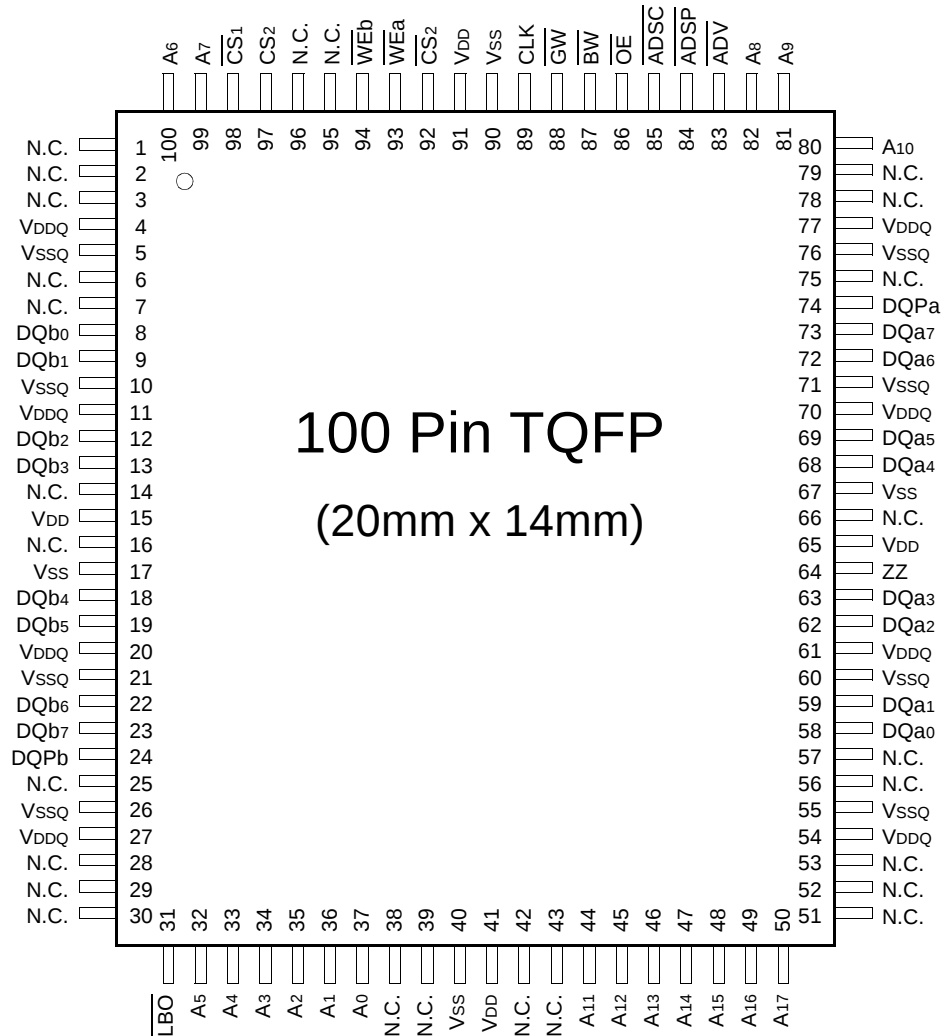
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input. ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B401825M is implemented in SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29,30,38,39,42,43,51,52,53,56,57,66,75,78,79,95,96
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
ADSP	Address Status Processor	84	DQb0~b7		8,9,12,13,18,19,22,23
ADSC	Address Status Controller	85	DQPa, Pb		74,24
CLK	Clock	89	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS1	Chip Select	98	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	97			
CS2	Chip Select	92			
WEx	Byte Write Inputs	93,94			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The K7B401825M is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ and Chip Select pins.

When $\overline{ZZ}$ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2 cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and both $\overline{WEa}$ and $\overline{WEb}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation. All byte write occurs by enabling $\overline{GW}$ (in dependent of $\overline{BW}$ and $\overline{WEx}$), and individual byte write is performed only when $\overline{GW}$ is High and $\overline{BW}$ is Low. $\overline{WEa}$ controls $DQa0 \sim DQa7$ and $DQPa$, $\overline{WEb}$ controls $DQb0 \sim DQb7$ and $DQ Pb$.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{\text{LBO PIN}}$	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0
Fourth Address									

(Linear Burst)

$\overline{\text{LBO}}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	$\overline{ZZ}$	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. $\overline{ZZ}$ pin is pulled down internally.
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	None	Not Selected
L	L	X	L	X	X	X	↑	None	Not Selected
L	X	H	L	X	X	X	↑	None	Not Selected
L	L	X	X	L	X	X	↑	None	Not Selected
L	X	H	X	L	X	X	↑	None	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.

$\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins($\overline{ZZ}$ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.3 to 6.0	V
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	PD	1.2	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	3.135	3.3	3.6	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE* (TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDI-	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOU=0V	-	8	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Leakage Current(except ZZ)	I _{IL}	$V_{DD}=\text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	2	μA
Output Leakage Current	I _{OL}	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	2	μA
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ $\leq$ V _{IL} , All Inputs=V _{IL} or V _{IH} Cycle Time $\geq$ t _{CYC} Min	-75	-	350
			-80	-	325
			-90	-	300
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ $\leq$ V _{IL} , f=Max, All Inputs $\leq$ 0.2V or $\geq$ V _{DD} -0.2V	-75	-	100
			-80	-	90
			-90	-	80
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ $\leq$ 0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	30	mA
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ $\geq$ V _{DD} -0.2V, f=Max, All Inputs $\leq$ V _{IL} or $\geq$ V _{IH}	-	30	mA
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} = 8.0mA	-	0.4	V
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} = -4.0mA	2.4	-	V
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} = 1.0mA	-	0.4	V
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} = -1.0mA	2.0	-	V
Input Low Voltage(3.3V I/O)	V _{IL}		-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.5**	V
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.5**	V

* V_{IL}(Min)=-2.0(Pulse Width $\leq$ t_{CYC}/2)** V_{IH}(Max)=4.6(Pulse Width $\leq$ t_{CYC}/2)** In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.5V**TEST CONDITIONS**(V_{DD}=3.3V+0.3V/-0.165V, V_{DDQ}=3.3V+0.3/-0.165V or V_{DD}=3.3V+0.3V/-0.165V, V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0 to 70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1

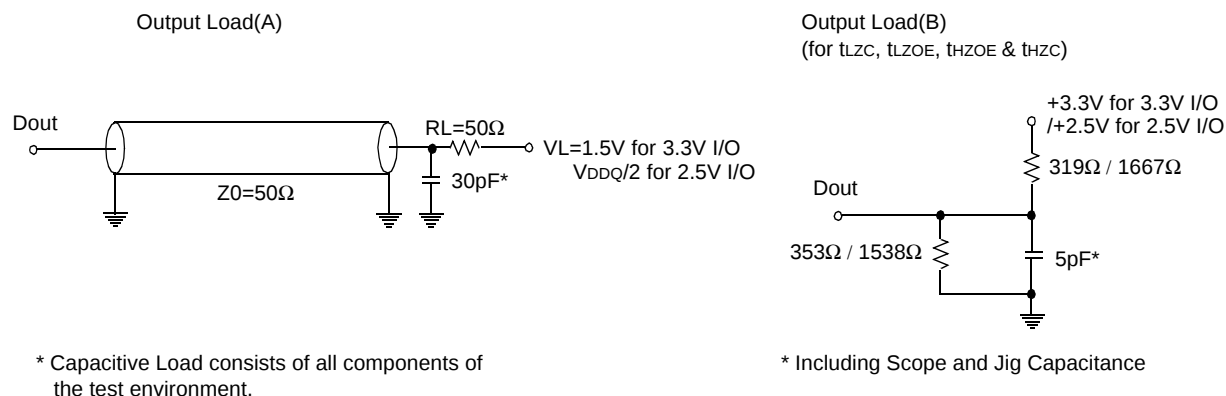


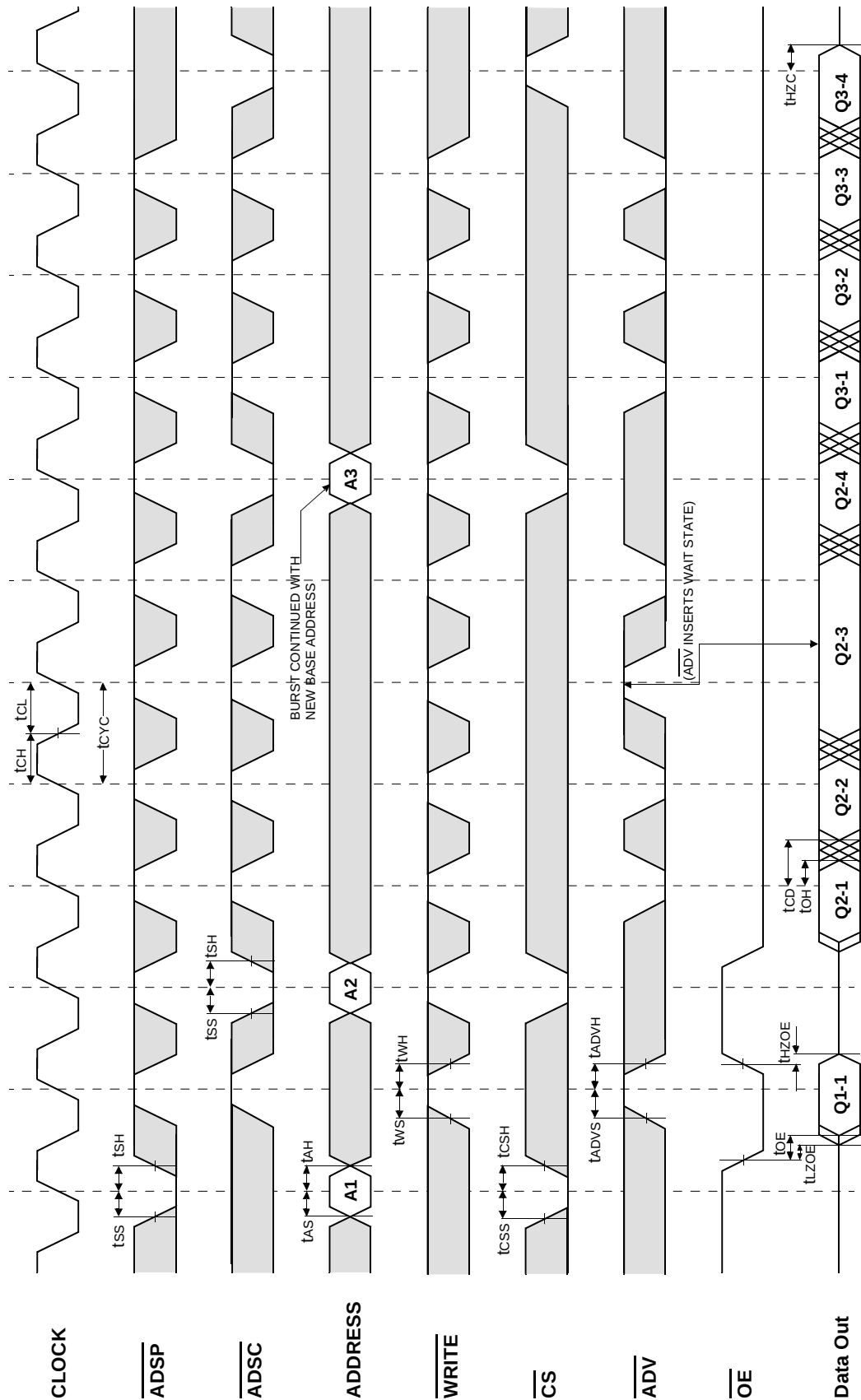
Fig. 1

AC TIMING CHARACTERISTICS($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$)

PARAMETER	SYMBOL	-75		-80		-90		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t _{CYC}	8.5	-	10	-	12	-	ns
Clock Access Time	t _{CD}	-	7.5	-	8	-	9	ns
Output Enable to Data Valid	t _{OE}	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t _{LZC}	0	-	0	-	0	-	ns
Output Hold from Clock High	t _{OH}	2	-	2	-	2	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	3.5	-	3.5	-	3.5	ns
Clock High to Output High-Z	t _{HZC}	2	3.5	2	3.5	2	3.5	ns
Clock High Pulse Width	t _{CH}	3	-	4	-	4.5	-	ns
Clock Low Pulse Width	t _{CL}	3	-	4	-	4.5	-	ns
Address Setup to Clock High	t _{AS}	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t _{SS}	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t _{DS}	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t _{WS}	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t _{ADVS}	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t _{CSS}	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t _{SH}	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t _{WH}	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PD}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	2	-	cycle

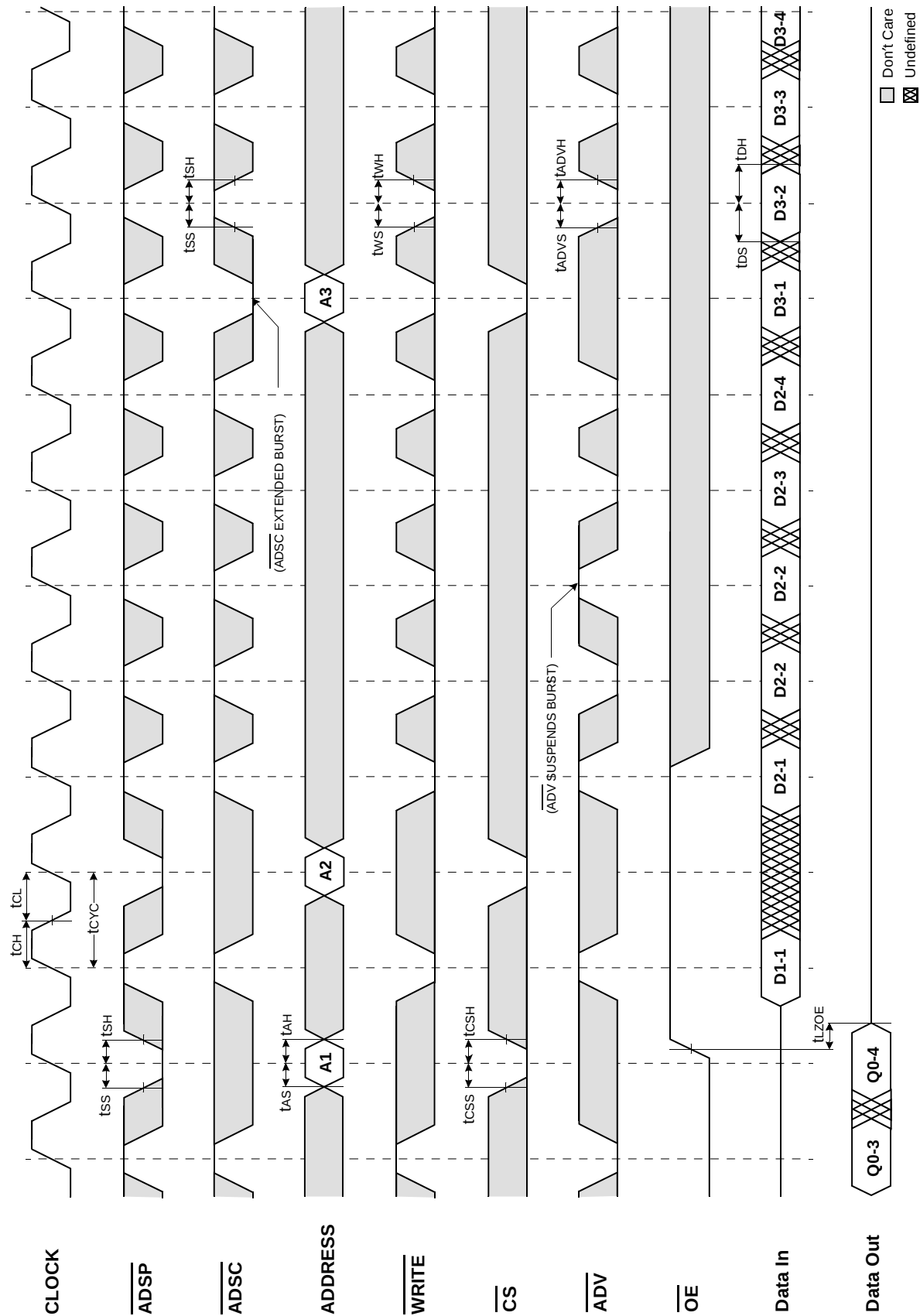
- Notes :**
1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
 3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.
 4. At any given voltage and temperature, t_{hzc} is less than t_{lzc}.

TIMING WAVEFORM OF READ CYCLE

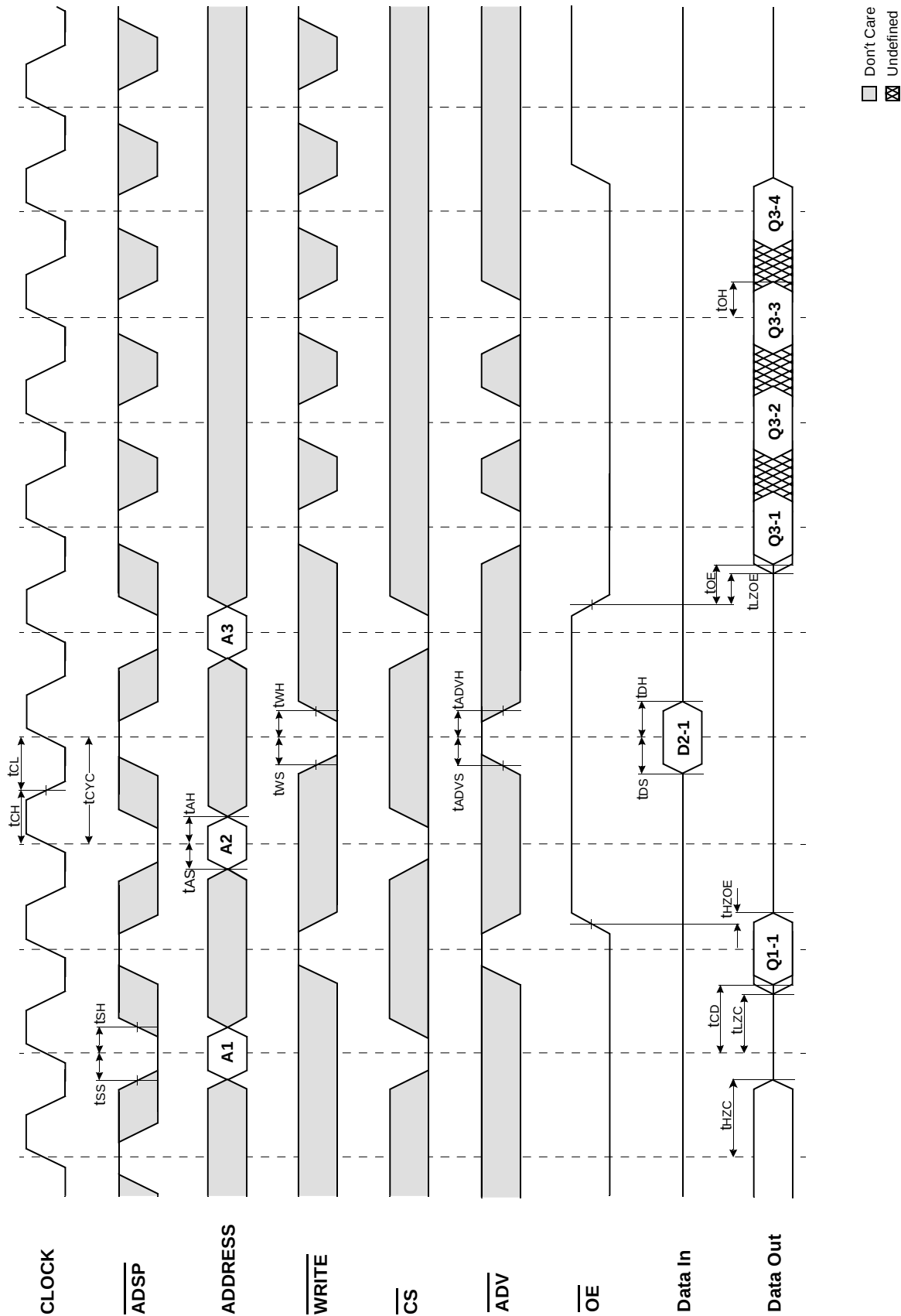


NOTES : $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE}_x = L$
 $\overline{CS} = L$ means $\overline{CS}_1 = L$, $\overline{CS}_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $\overline{CS}_2 = L$

TIMING WAVEFORM OF WRTE CYCLE



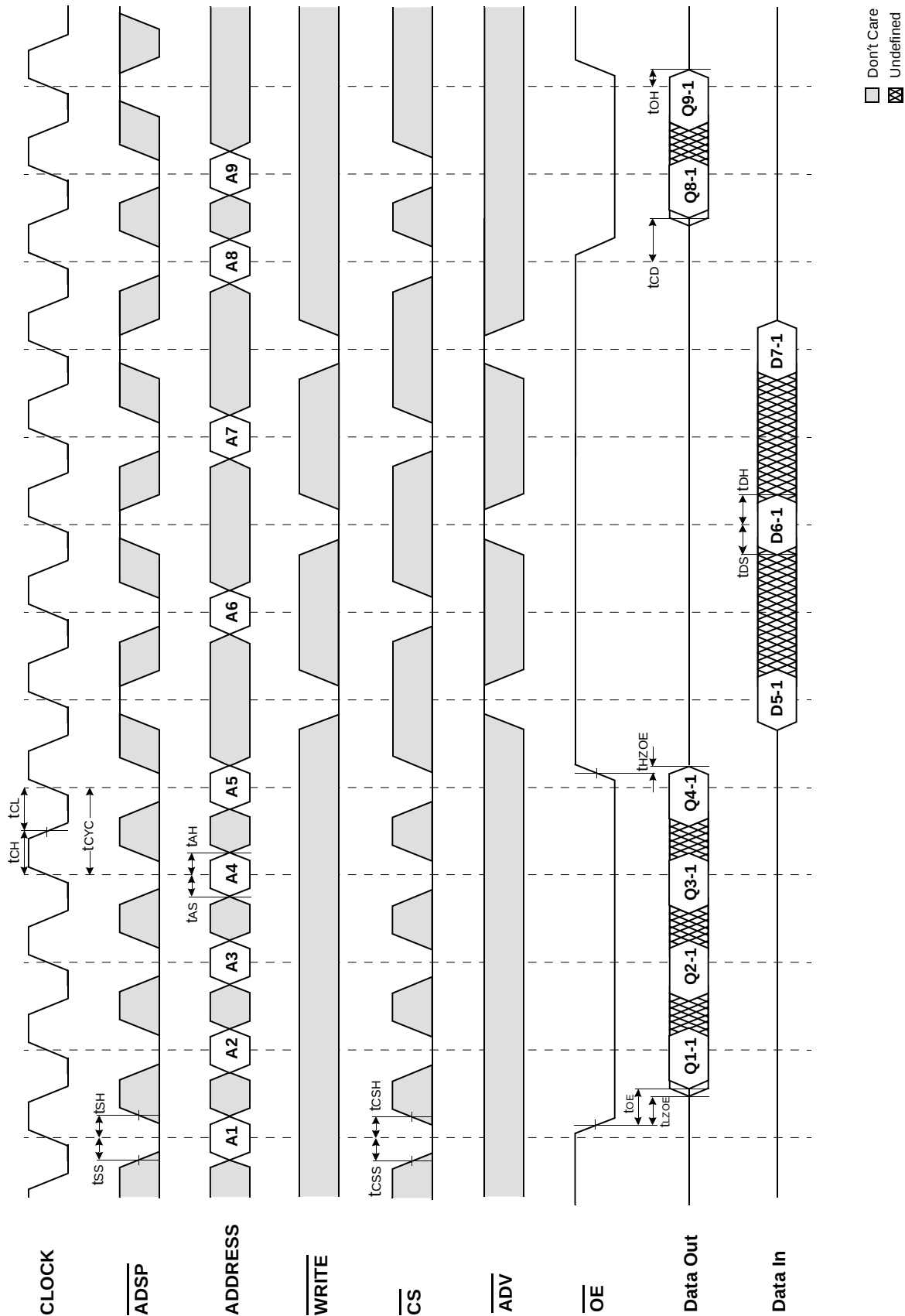
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



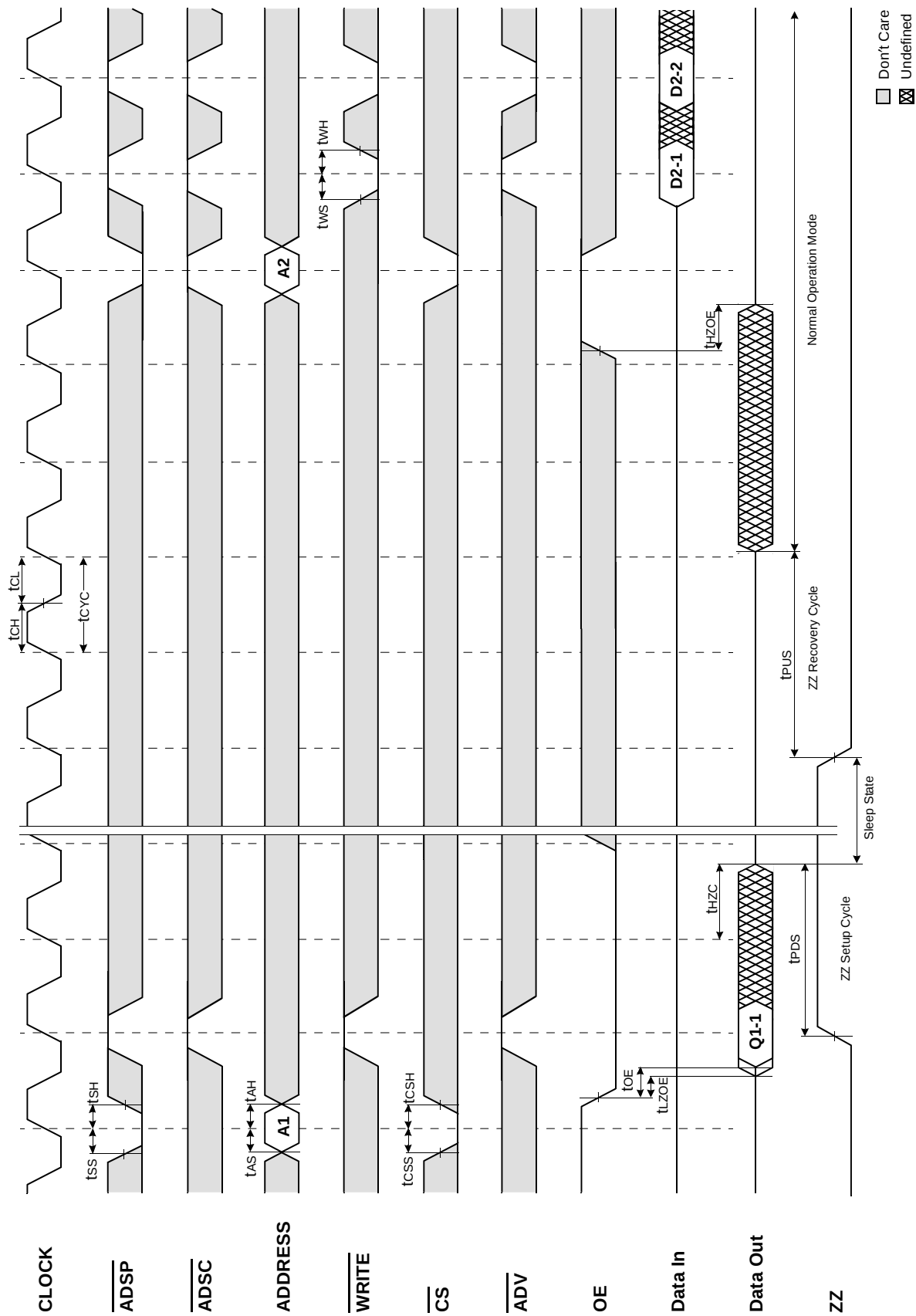
☐ Don't Care

☒ Undefined

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



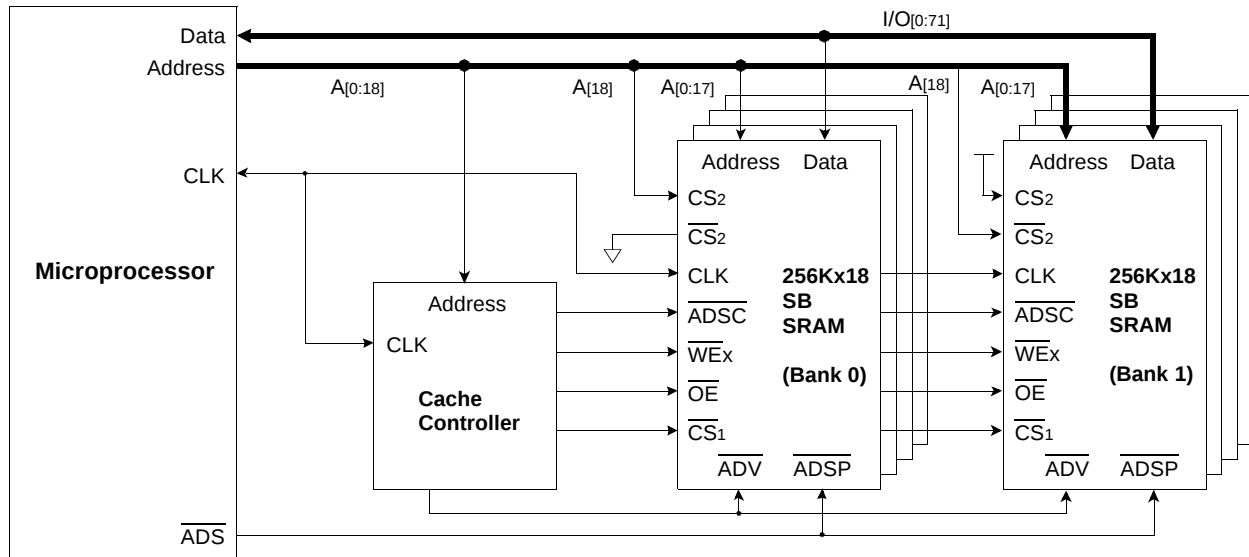
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

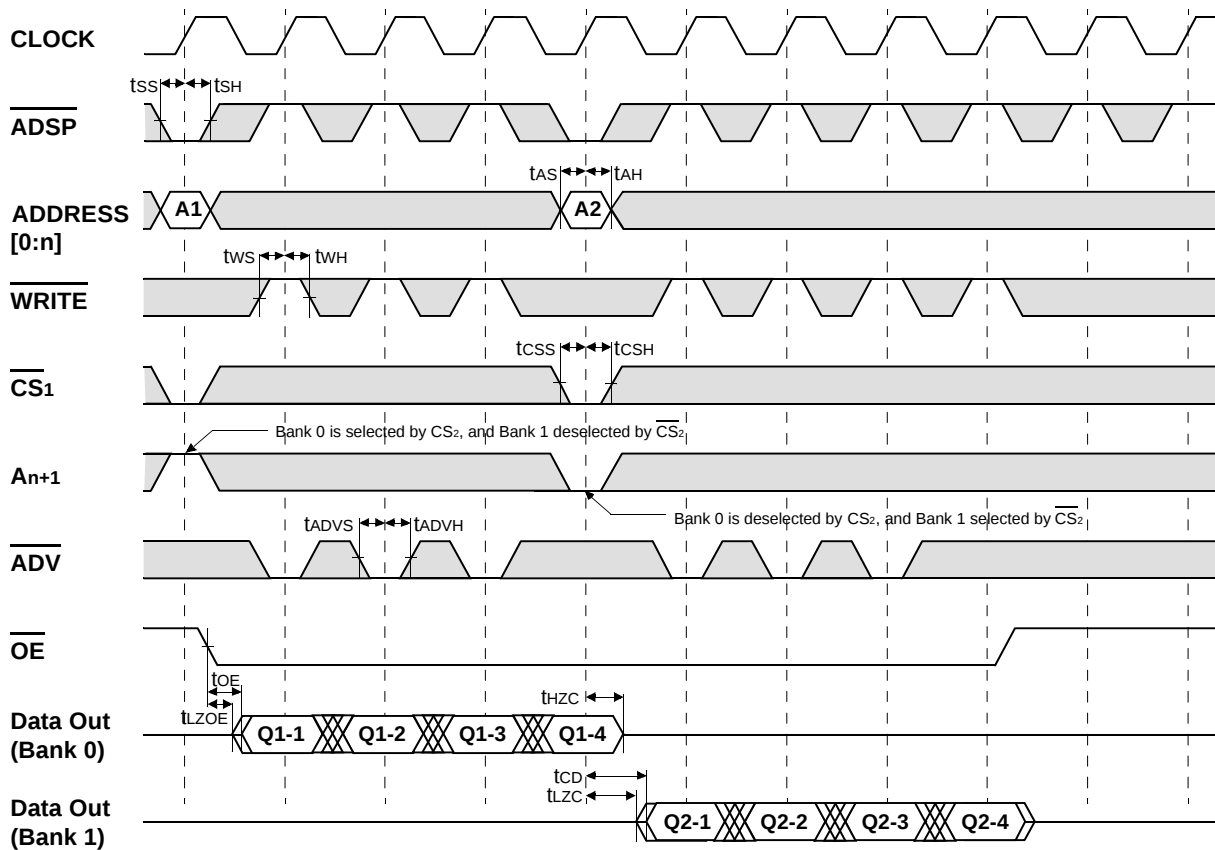
DEPTH EXPANSION

The Samsung 256Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



*Notes : n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

□ Don't Care ⊗ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units: millimeters/inches

