

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	RAS Access Time	60ns	70ns
t_{CAC}	CAS Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 18Mb DRAMS (1M x 18)

- Single 5V, $\pm 0.5V$ Power Supply
- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: RAS-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications.
- Au and Sn/Pb versions available

Description

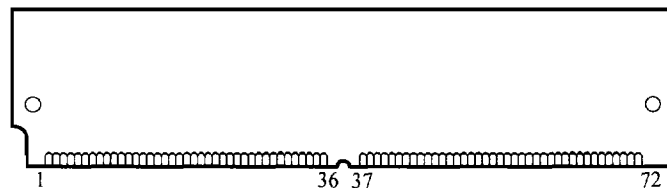
The IBM11D1360L is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array that is intended for use in 18, 36 and 72 bit applications. It is manufactured with 2 1Mx18 devices, each in a 400mil TSOP package, and is compatible with the JEDEC 72-Pin SIMM standard.

This assembly is intended as a direct replacement for 1Mx4-based SIMMs, while significantly reducing power dissipation. The use of TSOP packages allows tighter SIMM spacing (.3" on center). Input

loading is consistent with 4Mb-based assemblies due to the addition of discrete capacitors - maximizing compatibility at the system-level.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx36 parity SIMM, IBM11D1360B, as well as higher density, parity and ECC-optimized SIMMs.

Card Outline





Pin Description

$\overline{\text{RAS0}}$, RAS2	Row Address Strobe
$\overline{\text{CAS0}}$ - CAS3	Column Address Strobe
$\overline{\text{WE}}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

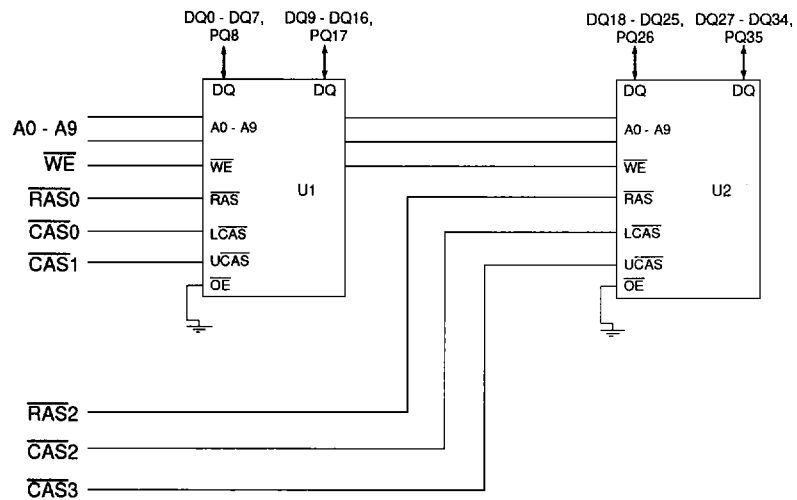
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{\text{WE}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360LA-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .104"	
IBM11D1360LA-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .104"	
IBM11E1360LA-60	1M x 36	60ns	Au	4.25" x 1" x .104"	
IBM11E1360LA-70	1M x 36	70ns	Au	4.25" x 1" x .104"	

Block Diagram



Truth Table

Function	RAS	CAS	WE	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
RAS-Only Refresh	L	H	X	Row	N/A	High Impedance
CAS-Before-RAS Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V _{SS}	V _{SS}
PD2	V _{SS}	V _{SS}
PD3	NC	V _{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V _{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V _{IN}	Input Voltage	-0.5 to min (V _{CC} + 0.5, 7.0)	V	1
V _{OUT}	Output Voltage	-0.5 to min (V _{CC} + 0.5, 7.0)	V	1
T _{OPR}	Operating Temperature	0 to +70	°C	1
T _{STG}	Storage Temperature	-55 to +125	°C	1
P _D	Power Dissipation	2.3	W	1
I _{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V _{IH}	Input High Voltage	2.4	—	V _{CC} + 0.5	V	1
V _{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C _{I1}	Input Capacitance (A0-A9)	47	pF	
C _{I2}	Input Capacitance ($\overline{\text{RAS}}$)	32	pF	
C _{I3}	Input Capacitance ($\overline{\text{CAS}}$)	17	pF	
C _{I4}	Input Capacitance ($\overline{\text{WE}}$)	50	pF	
C _{I/O}	Output Capacitance (DQ0-DQ34, PQ8, PQ17, PQ26, PQ35)	15	pF	

DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5 \pm 0.5\text{V}$)

Symbol	Parameter	Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC} = t_{RC \text{ min}}$)	-60	—	mA	1, 2, 3
		-70	—		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (RAS = CAS $\geq V_{IH}$)	—	4	mA	
I_{CC3}	RAS Only Refresh Current Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS $\geq V_{IH}$; $t_{RC} = t_{RC \text{ min}}$)	-60	—	mA	1, 3
		-70	—		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode (RAS = V_{IL} , CAS, Address Cycling: $t_{PC} = t_{PC \text{ min}}$)	-60	—	mA	1, 2, 3
		-70	—		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (RAS = CAS = $V_{CC} - 0.2\text{V}$)	—	2	mA	
I_{CC6}	CAS Before RAS Refresh Current Average Power Supply Current, CAS Before RAS Mode (RAS, CAS, Cycling: $t_{RC} = t_{RC \text{ min}}$)	-60	—	mA	1, 3
		-70	—		
$I_{(IL)}$	Input Leakage Current Input Leakage Current, any input ($0.0 \leq V_{IN} \leq (V_{CC} - 6.0\text{V})$) All Other Pins Not Under Test = 0V	RAS	-10	μA	
		CAS	-10		
		All others	-20		
$I_{O(IL)}$	Output Leakage Current (D_{OUT} is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$)	-10	+10	μA	
V_{OH}	Output High Level Output "H" Level Voltage ($I_{OUT} = -5\text{mA}$ @ 2.4V)	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage ($I_{OUT} = +4.2\text{mA}$ @ 0.4V)	—	0.4	V	
1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate. 2. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open. 3. Address can be changed once or less while RAS = V_{IL} . In the case of I_{CC4} , it can be changed once or less when CAS = V_{IH} .					



AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200μs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	50	—	ns	
t _{CP}	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	ns	
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	16K	70	16K	ns	
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	15	—	20	—	ns	
t _{ASR}	Row Address Setup Time	0	—	0	—	ns	
t _{RAH}	Row Address Hold Time	10	—	10	—	ns	
t _{ASC}	Column Address Setup Time	0	—	0	—	ns	
t _{CAH}	Column Address Hold Time	15	—	15	—	ns	
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	45	20	50	ns	1
t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	—	15	—	ns	2
t _{RSH}	$\overline{\text{RAS}}$ Hold Time	15	—	20	—	ns	
t _{CSH}	$\overline{\text{CAS}}$ Hold Time	60	—	70	—	ns	
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	
t _{DZC}	$\overline{\text{CAS}}$ Delay Time from D _{IN}	0	—	0	—	ns	
t _T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t _{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	—	—	—	—	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.



Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{CPA} , t_{AA} .
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.



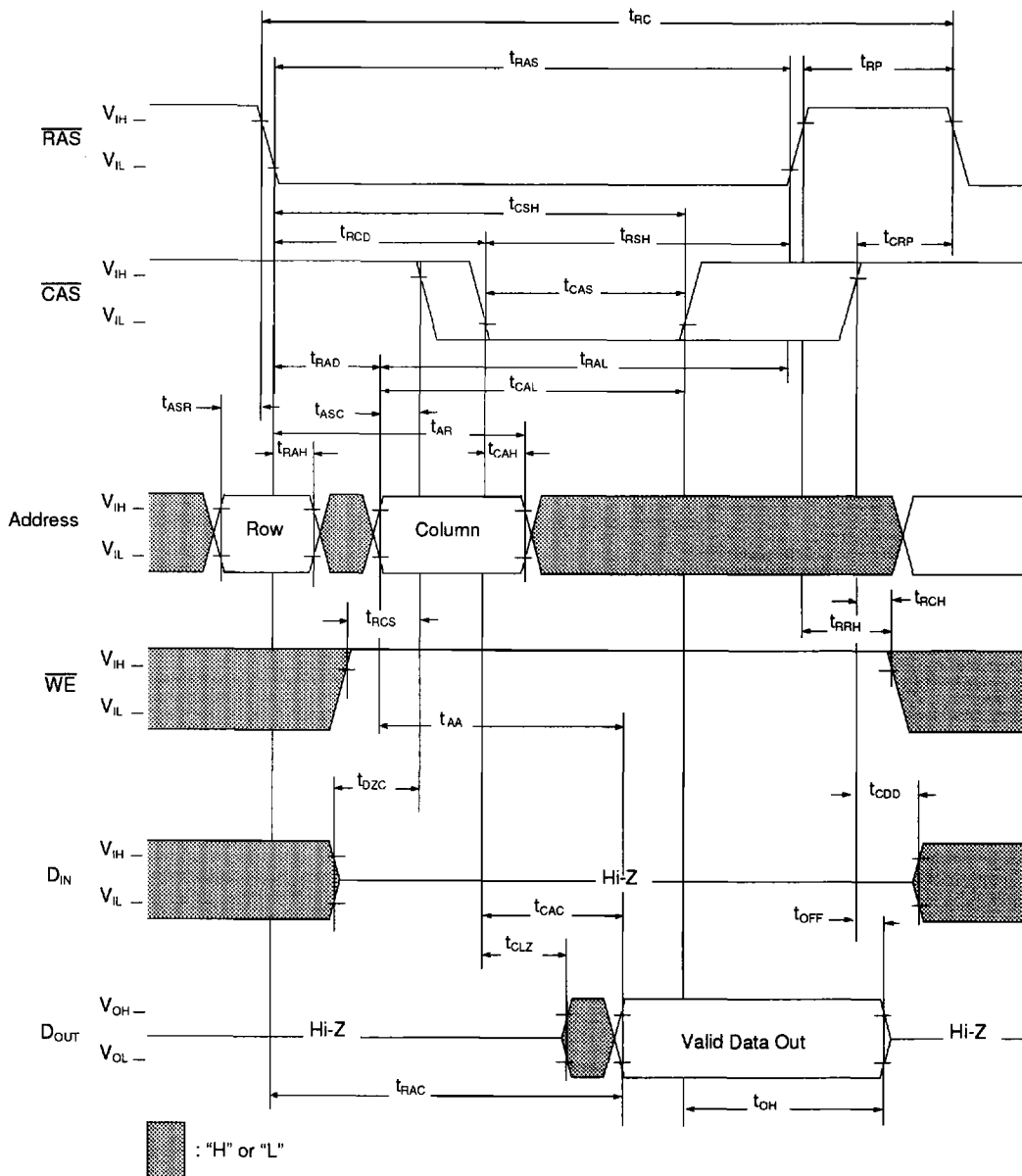
Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}. 2. Access time assumes a load of 100pF.							

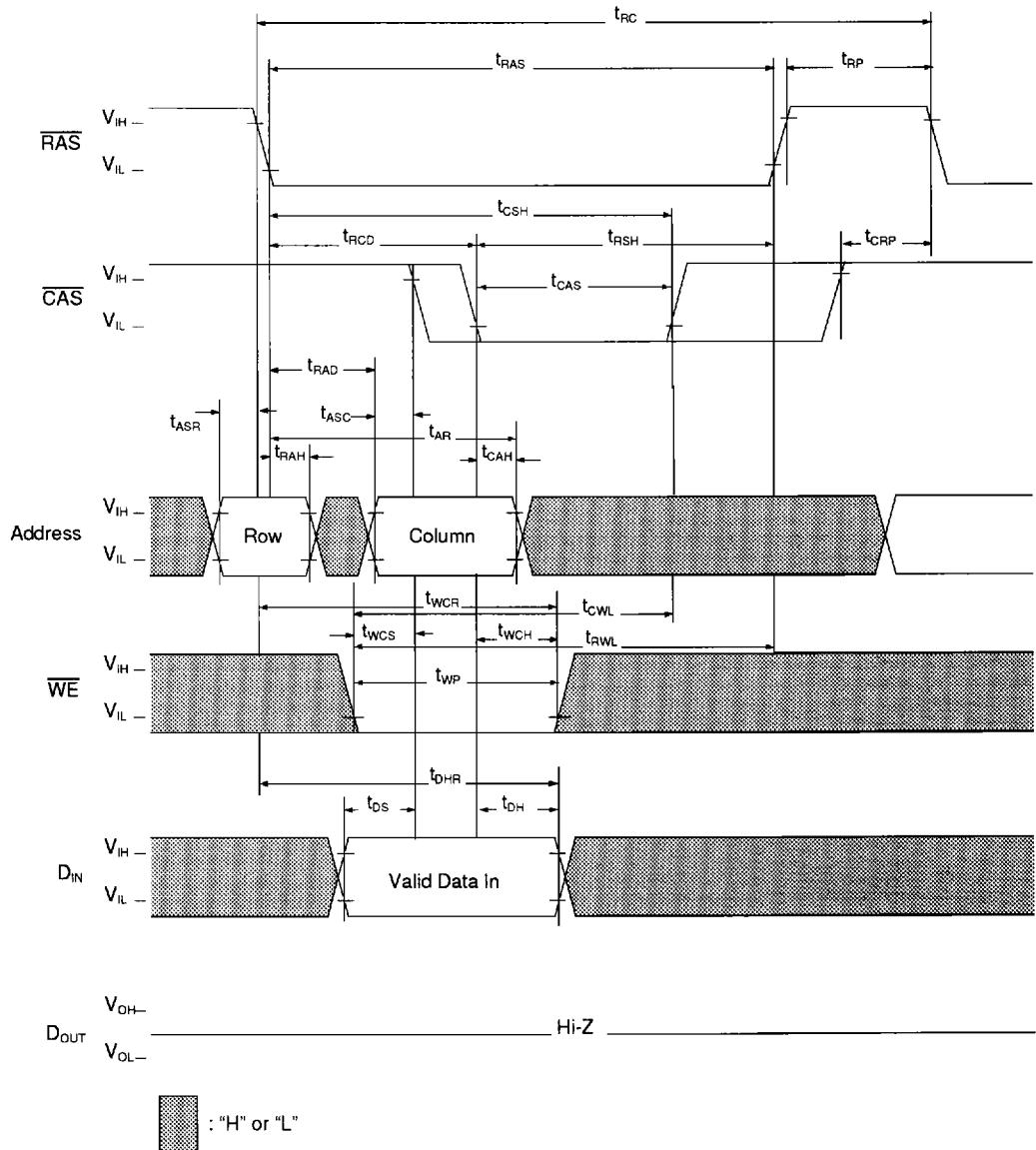
Refresh Cycle

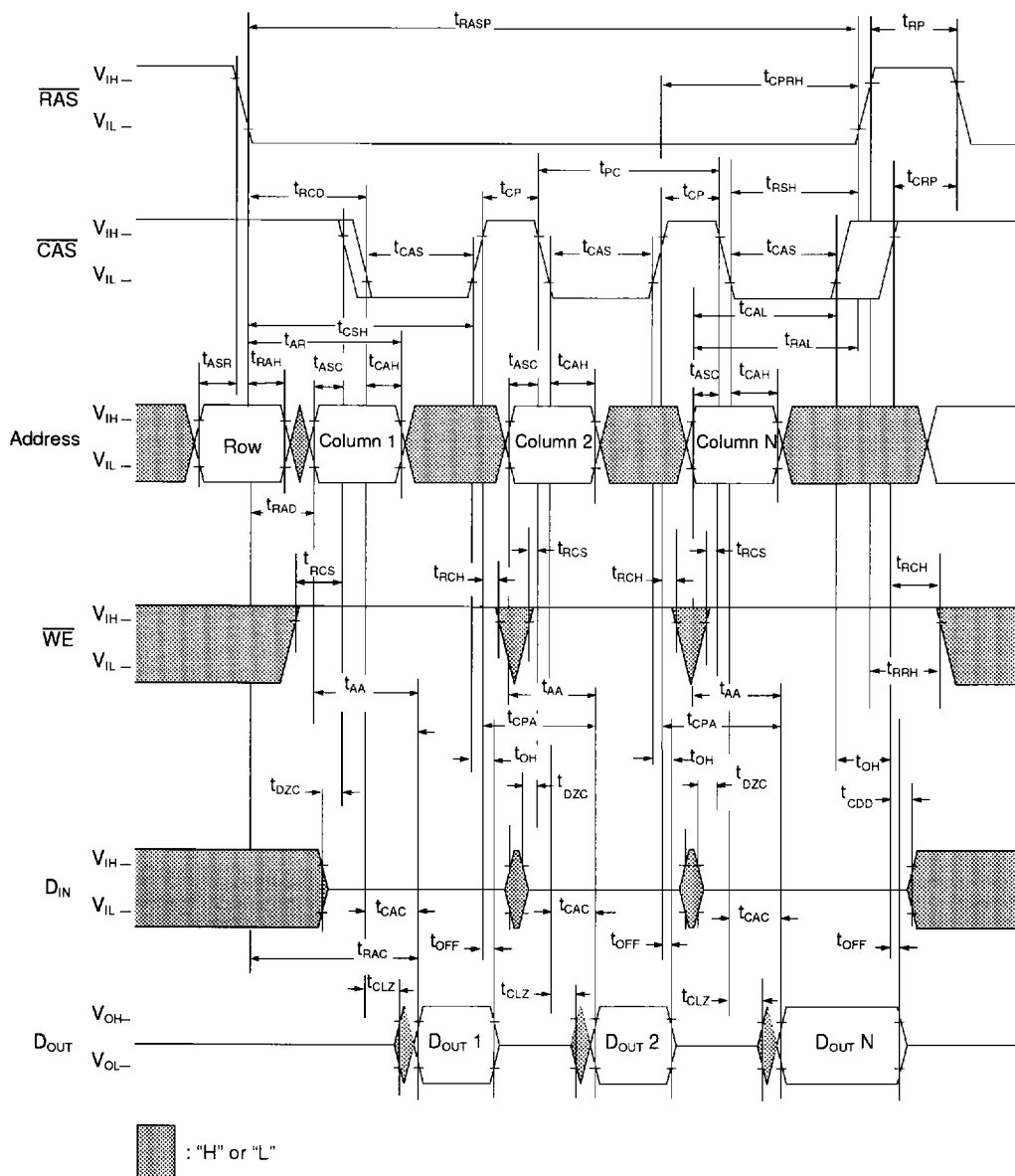
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1
1. 1024 refreshes are required every 16ms.							

Read

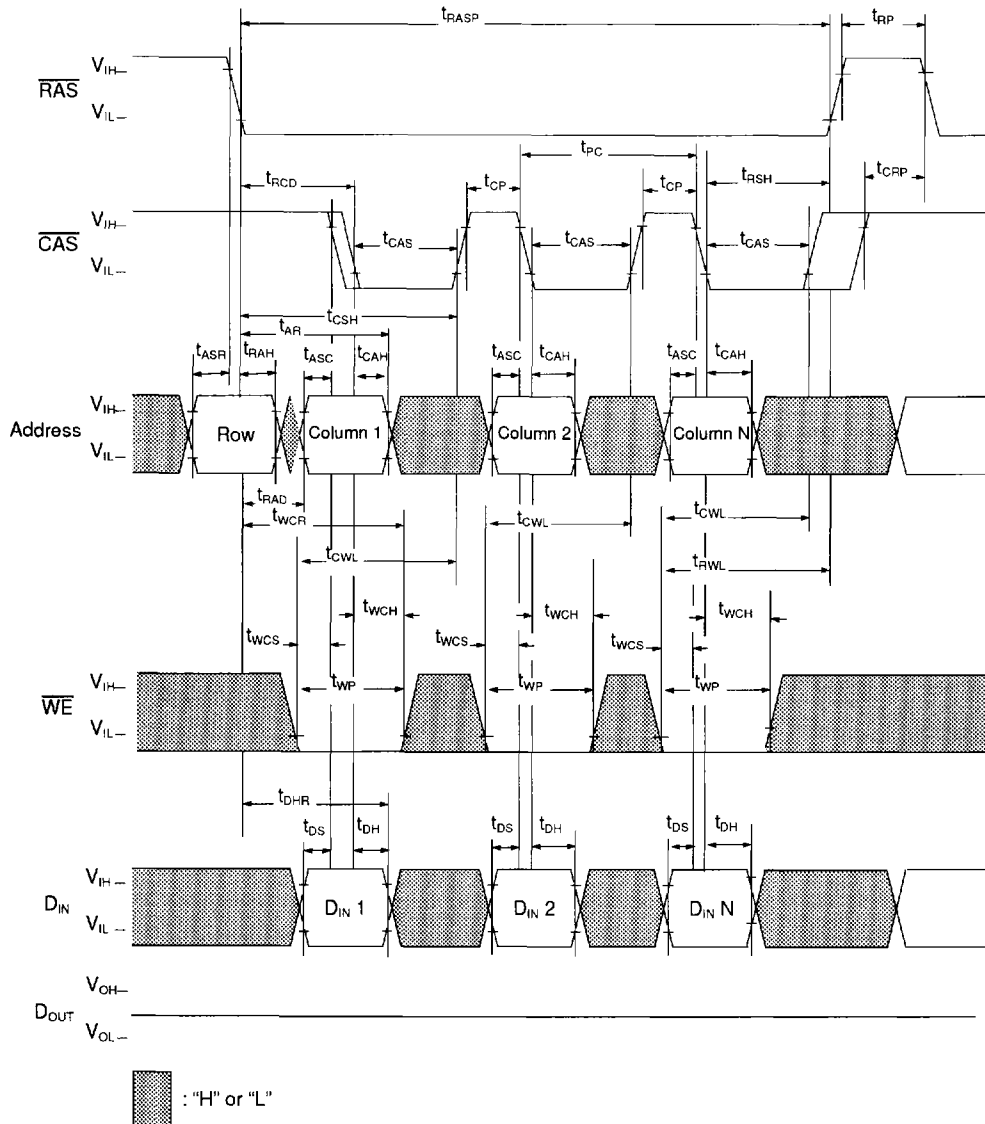


Write Cycle (Early Write)

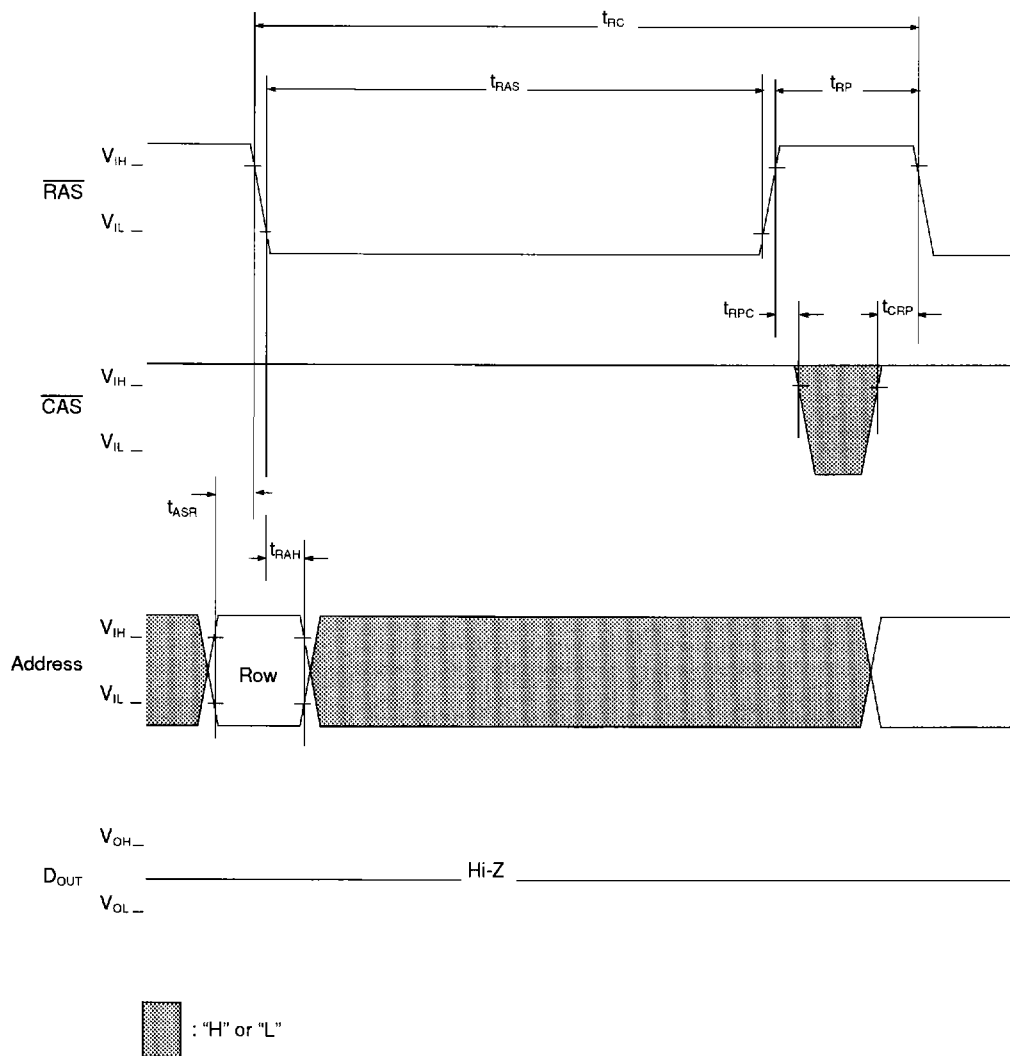




Fast Page Mode Write Cycle

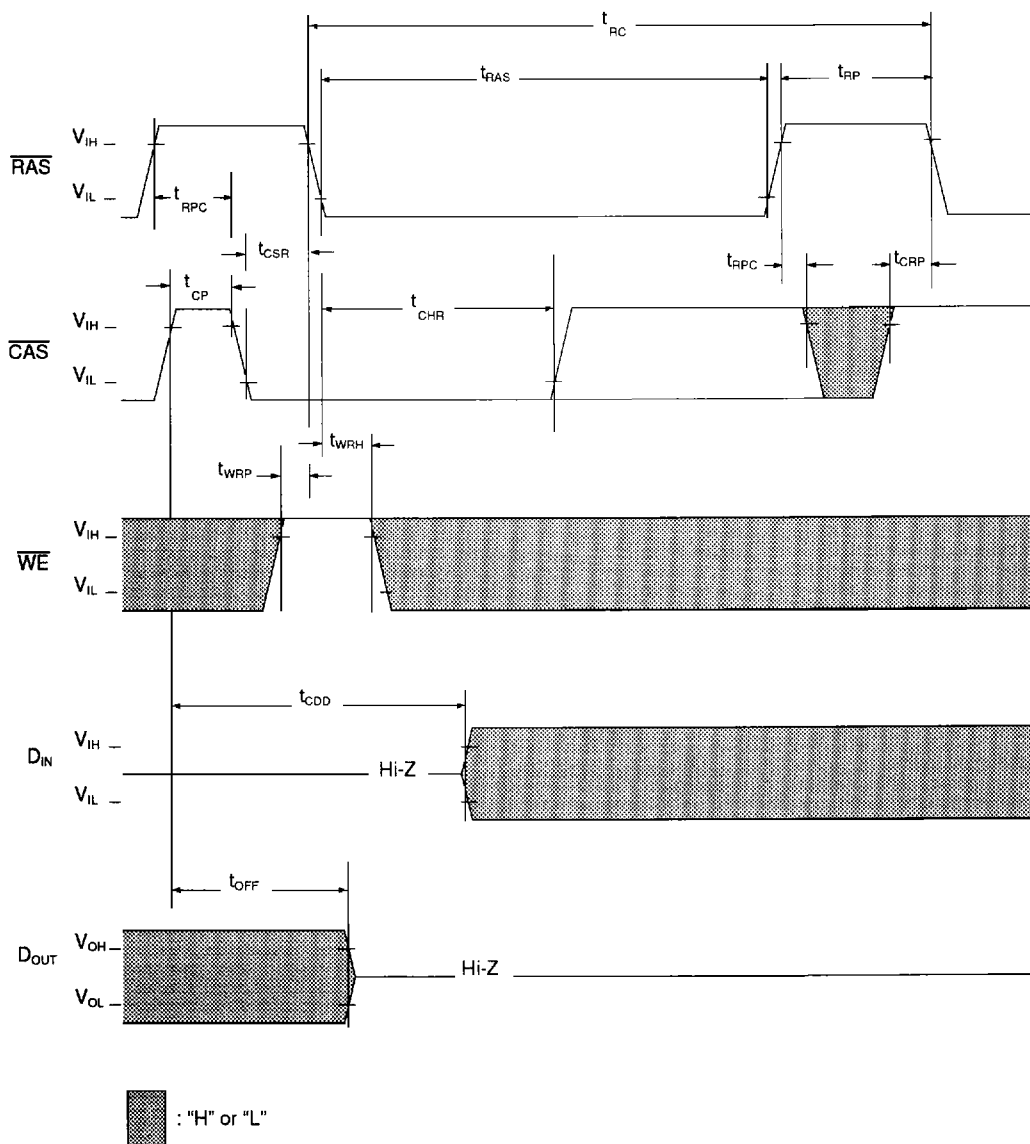


$\overline{\text{RAS}}$ Only Refresh Cycle



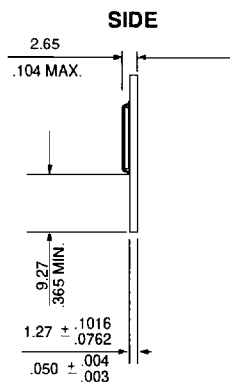
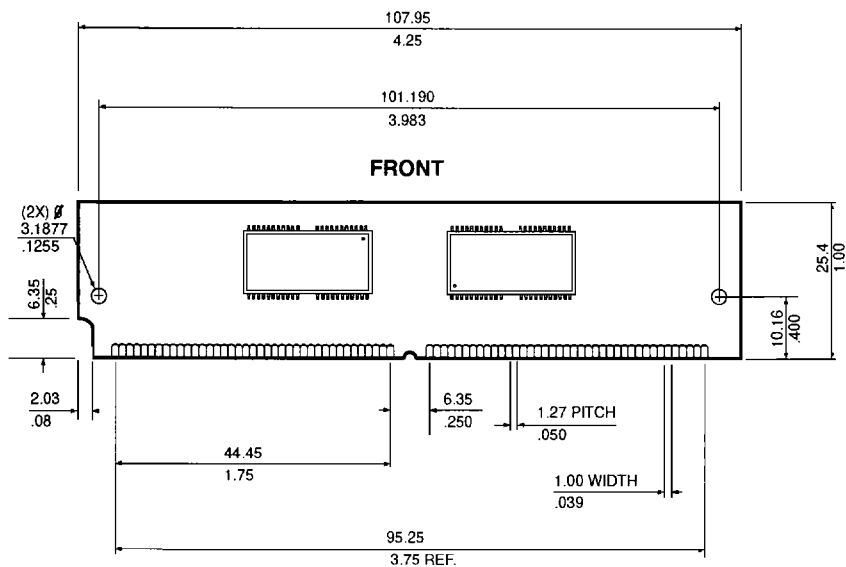
Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

CAS Before RAS Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



NOTE: All dimensions are typical unless otherwise stated. $\frac{\text{MILLIMETERS}}{\text{INCHES}}$