



# Differential Clock Buffer/Driver DDR333/PC2700-Compliant

## Features

- Operating frequency: 60 MHz to 200 MHz
- Supports 266, 333-MHz DDR SDRAM
- 10 differential outputs from 1 differential input
- Spread-Spectrum-compatible
- Low jitter (cycle-to-cycle): < 75
- Very low skew: < 100 ps
- Power management control input
- High-impedance outputs when input clock < 10 MHz
- 2.5V operation
- Pin-compatible with CDC857-2 and -3
- 48-pin TSSOP package
- Industrial temp. of -40° to +85°C
- Conforms to JEDEC DDR specification

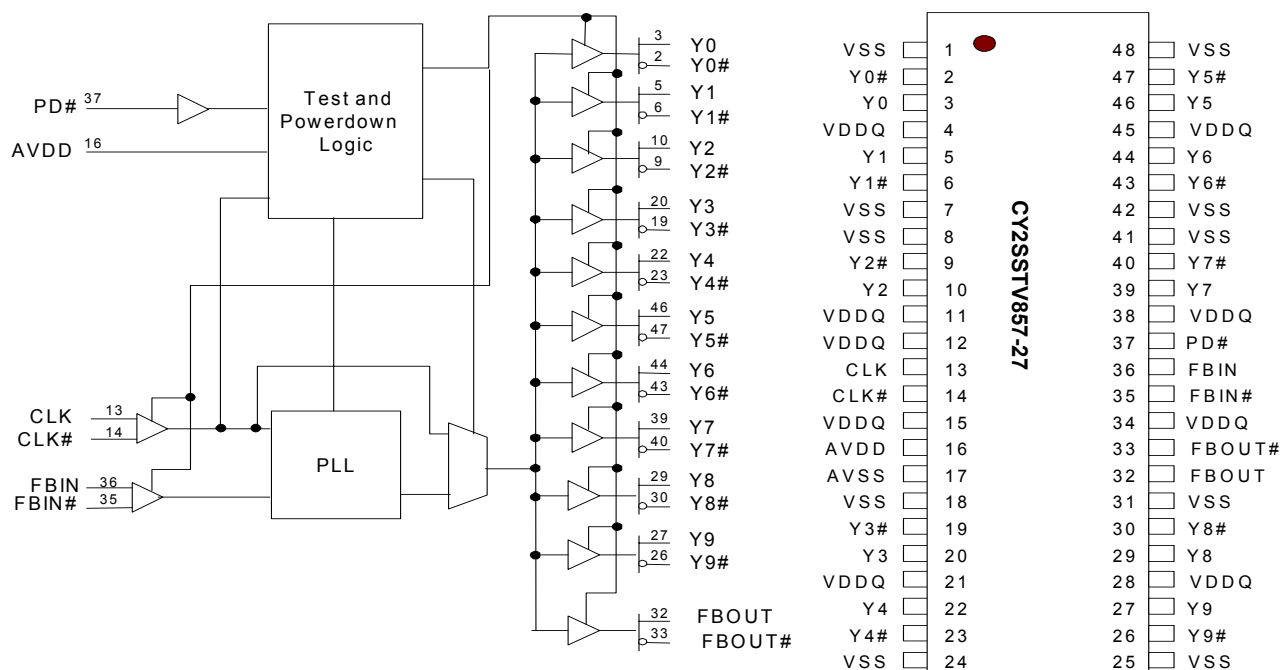
## Description

The CY2SSTV857-27 is a high-performance, low-skew, low-jitter zero-delay buffer designed to distribute differential clocks in high-speed applications. The CY2SSTV857-27 generates ten differential pair clock outputs from one differential pair clock input. In addition, the CY2SSTV857-27 features differential feedback clock outputs and inputs. This allows the CY2SSTV857-27 to be used as a zero-delay buffer.

When used as a zero-delay buffer in nested clock trees, the CY2SSTV857-27 locks onto the input reference and translates with near-zero delay to low-skew outputs.

## Block Diagram

## Pin Configuration



## Pin Description

Pin Number	Pin Name	I/O <sup>[1]</sup>	Pin Description	Electrical Characteristics
13, 14	CLK, CLK#	I	<b>Differential Clock Input.</b>	LV Differential Input
35	FBIN#	I	<b>Feedback Clock Input.</b> Connect to FBOUT# for accessing the PLL.	Differential Input
36	FBIN	I	<b>Feedback Clock Input.</b> Connect to FBOUT for accessing the PLL.	
3, 5, 10, 20, 22	Y(0:4)	O	<b>Clock Outputs</b>	Differential Outputs
2, 6, 9, 19, 23	Y#(0:4)	O	<b>Clock Outputs</b>	
27, 29, 39, 44, 46	Y(9:5)	O	<b>Clock Outputs</b>	Differential Outputs
26, 30, 40, 43, 47	Y#(9:5)	O	<b>Clock Outputs</b>	
32	FBOUT	O	<b>Feedback Clock Output.</b> Connect to FBIN for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	Differential Outputs
33	FBOUT#	O	<b>Feedback Clock Output.</b> Connect to FBIN# for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.	
37	PD#	I	<b>Power Down# Input.</b> When PD# is set HIGH, all Q and Q# outputs are enabled and switch at the same frequency as CLK. When set LOW, all Q and Q# outputs are disabled Hi-Z and the PLL is powered down.	
4, 11, 12, 15, 21, 28, 34, 38, 45	VDDQ		<b>2.5V Power Supply for Output Clock Buffers.</b>	2.5V Nominal
16	AVDD		<b>2.5V Power Supply for PLL.</b> When VDDA is at GND, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (PD# = 0), the PLL is powered down.	2.5V Nominal
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	VSS		<b>Common Ground</b>	0.0V Ground
17	AVSS		<b>Analog Ground</b>	0.0V Analog Ground

## Zero-delay Buffer

When used as a zero-delay buffer the CY2SSTV857-27 will likely be in a nested clock tree application. For these applications the CY2SSTV857-27 offers a differential clock input pair as a PLL reference. The CY2SSTV857-27 then can lock onto the reference and translate with near-zero delay to low-skew outputs. For normal operation, the external feedback input, FBIN, is connected to the feedback output, FBOUT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near-zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

### Note:

1. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces.

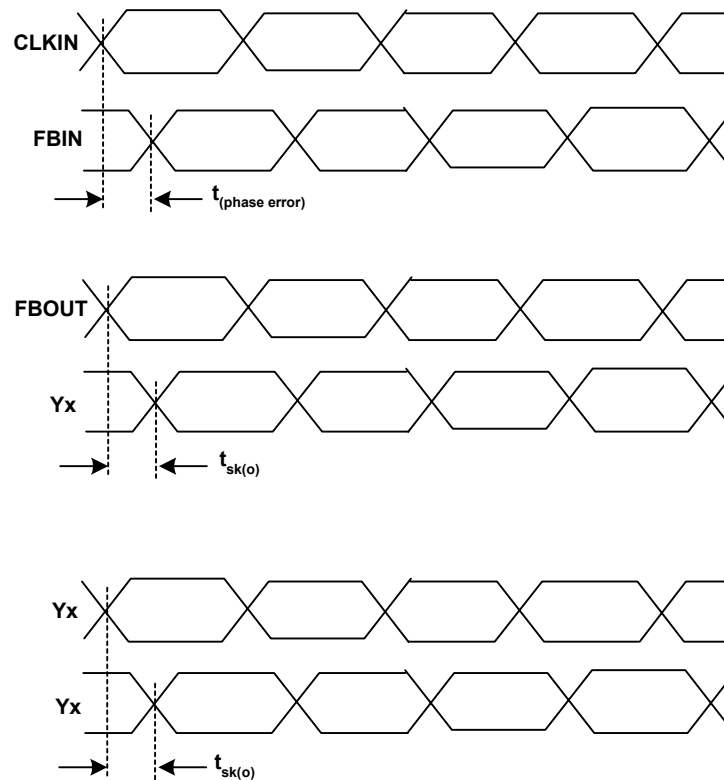
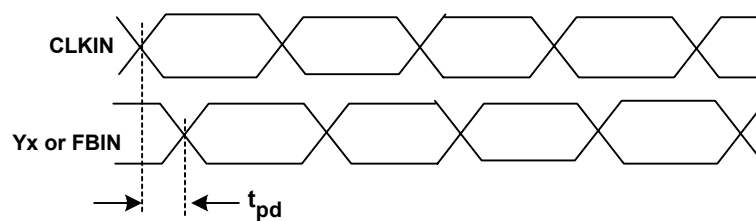
When VDDA is strapped LOW, the PLL is turned off and bypassed for test purposes.

## Power Management

Output enable/disable control of the CY2SSTV857-27 allows the user to implement power management schemes into the design. Outputs are three-stated/disabled when PD# is asserted low (see *Table 1*).

**Table 1. Function Table**

Inputs				Outputs				PLL
AVDD	PD#	CLK	CLK#	Y	Y#	FBOUT	FBOUT#	
GND	H	L	H	L	H	L	H	BYPASSED/OFF
GND	H	H	L	H	L	H	L	BYPASSED/OFF
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	OFF
2.5V	H	L	H	L	H	L	H	On
2.5V	H	H	L	H	L	H	L	On
2.5V	H	< 10 MHz	< 10 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off


**Figure 1. Phase Error and Skew Waveforms**

**Figure 2. Propagation Delay Time  $t_{PLH}$ ,  $t_{PHL}$**

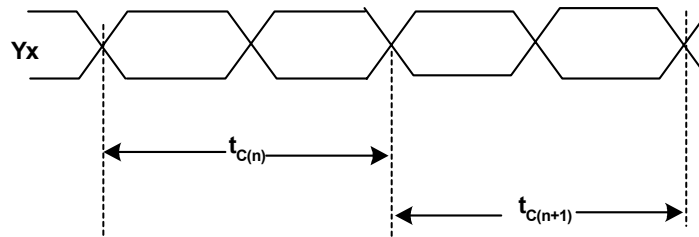


Figure 3. Cycle-to-cycle Jitter

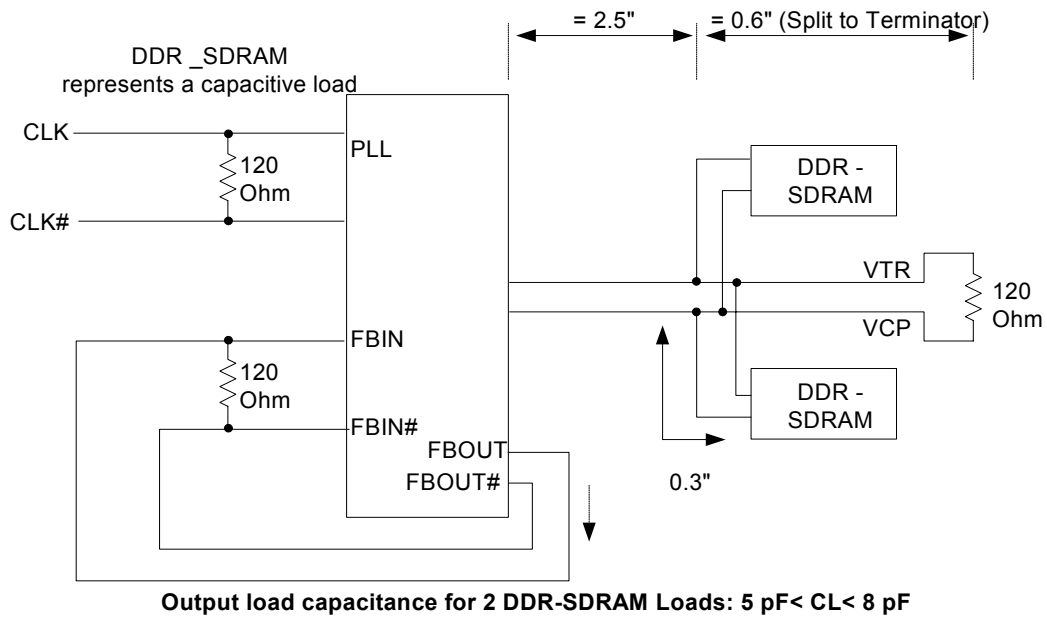


Figure 4. Clock Structure # 1

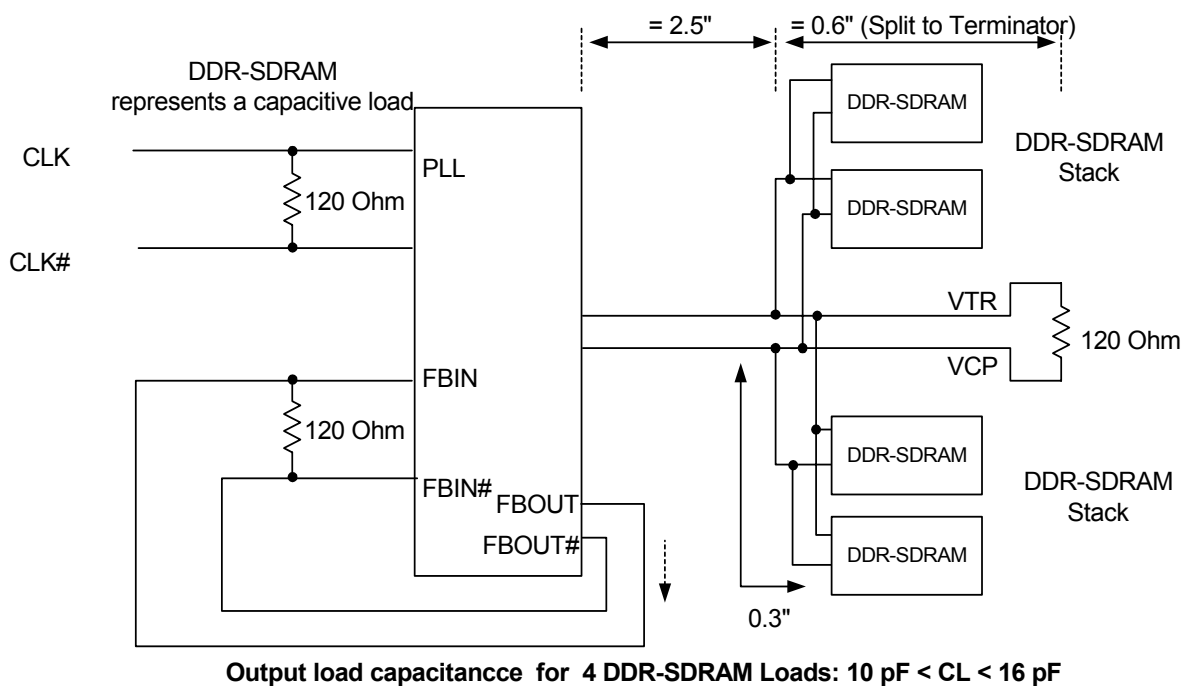
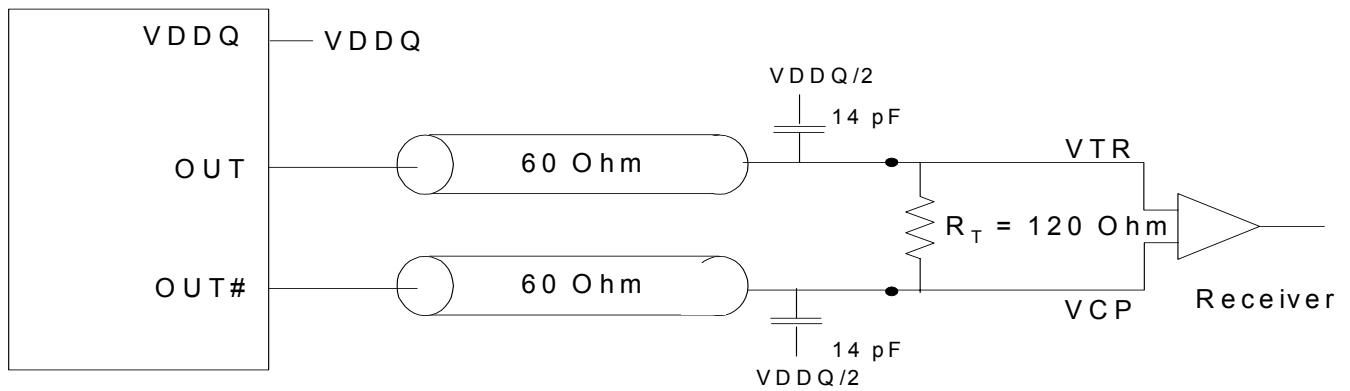


Figure 5. Clock Structure # 1



**Figure 6. Differential Signal Using Direct Termination Resistor**

**Absolute Maximum Conditions**<sup>[2]</sup>

Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Input Voltage Relative to  $V_{DDQ}$  or  $AV_{DD}$ : .....  $V_{DDQ} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $0^{\circ}C$  to  $+85^{\circ}C$   
 Maximum Power Supply: .....  $3.5V$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DDQ}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DDQ}$ ).

**DC Electrical Specifications** ( $AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ )<sup>[3]</sup>

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$V_{DDQ}$	Supply Voltage	Operating	2.38	2.5	2.63	V
$V_{IL}$	Input Low Voltage	PD#			$0.3 \times V_{DDQ}$	V
$V_{IH}$	Input High Voltage		$0.7 \times V_{DDQ}$			V
$V_{ID}$	Differential Input Voltage <sup>[4]</sup>	CLK, FBIN	0.36		$V_{DDQ} + 0.3$	V
$V_{IX}$	Differential Input Crossing Voltage <sup>[5]</sup>	CLK, FBIN	$(V_{DDQ}/2) - 0.2$	$V_{DDQ}/2$	$(V_{DDQ}/2) + 0.2$	V
$I_{IN}$	Input Current [CLK, FBIN, PD#]	$V_{IN} = 0V$ or $V_{IN} = V_{DDQ}$	-10		10	$\mu A$
$I_{OL}$	Output Low Current	$V_{DDQ} = 2.375V$ , $V_{OUT} = 1.2V$	26	35		mA
$I_{OH}$	Output High Current	$V_{DDQ} = 2.375V$ , $V_{OUT} = 1V$	-28	-32		mA
$V_{OL}$	Output Low Voltage	$V_{DDQ} = 2.375V$ , $I_{OL} = 12\text{ mA}$			0.6	V
$V_{OH}$	Output High Voltage	$V_{DDQ} = 2.375V$ , $I_{OH} = -12\text{ mA}$	1.7			V
$V_{OUT}$	Output Voltage Swing <sup>[6]</sup>		1.1		$V_{DDQ} - 0.4$	V
$V_{OC}$	Output Crossing Voltage <sup>[7]</sup>		$(V_{DDQ}/2) - 0.2$	$V_{DDQ}/2$	$(V_{DDQ}/2) + 0.2$	V
$I_{OZ}$	High-Impedance Output Current	$V_O = GND$ or $V_O = V_{DDQ}$	-10		10	$\mu A$
$I_{DDQ}$	Dynamic Supply Current <sup>[8]</sup>	All $V_{DDQ}$ , $F_O = 170\text{ MHz}$		235	300	mA
$I_{DD}$	PLL Supply Current	$V_{DDA}$ only		9	12	mA
$I_{DDS}$	Standby Supply Current	PD# = 0 and CLK/CLK# < 10 MHz			100	$\mu A$
Cin	Input Pin Capacitance				4	pF

**AC Electrical Specifications** ( $AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ )<sup>[9, 10]</sup>

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$f_{CLK}$	Operating Clock Frequency	$AV_{DD}$ , $V_{DDQ} = 2.5V \pm 0.2V$	60		200	MHz
$t_{DC}$	Input Clock Duty Cycle		40		60	%
$t_{LOCK}$	Maximum PLL lock Time				100	$\mu s$
$D_{TYC}$	Duty Cycle <sup>[11]</sup>	60 MHz to 100 MHz	49.5	50	50.5	%
		101 MHz to 170 MHz	49		51	%
$tsl(o)$	Output Clocks Slew Rate	20%–80% of VOD	1		2	V/ns

**Notes:**

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Unused inputs must be held HIGH or LOW to prevent them from floating.
- Differential input signal voltage specifies the differential voltage  $V_{TR} - V_{CPI}$  required for switching, where  $V_{TR}$  is the true input level and  $V_{CPI}$  is the complementary input level. See Figure 6.
- Differential cross-point input voltage is expected to track  $V_{DDQ}$  and is the voltage at which the differential signal must be crossing.
- For load conditions see Figure 6.
- The value of  $V_{OC}$  is expected to be  $(V_{TR} + V_{CPI})/2$ . In case of each clock directly terminated by a  $120\Omega$  resistor. See Figure 6.
- All outputs switching load with 14 pF in  $60\Omega$  environment. See Figure 6.
- Parameters are guaranteed by design and characterization. Not 100% tested in production.
- PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30kHz and 50 kHz with a down spread or  $-0.5\%$ .
- While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle =  $t_{WHC}/t_C$ , where the cycle time( $t_C$ ) decreases as the frequency goes up.

**AC Electrical Specifications** ( $AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ )(continued)<sup>[9, 10]</sup>

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$t_{PZL}, t_{PZH}$	Output Enable Time <sup>[12]</sup> (all outputs)			3	25	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time <sup>[12]</sup> (all outputs)			3	8	ns
$t_{CCJ}$	Cycle to Cycle Jitter <sup>[10]</sup>	$f > 66\text{ MHz}$	-75	—	75	ps
$t_{jit(h-per)}$	Half-period jitter <sup>[10, 13]</sup>	$f > 66\text{ MHz}$	-100	—	100	ps
$t_{PLH}(t_{PD})$	Low-to-High Propagation Delay, CLK to Y	Test Mode only	1.5	3.5	7.5	ns
$t_{PHL}(t_{PD})$	High-to-Low Propagation Delay, CLK to Y		1.5	3.5	7.5	ns
$t_{SK(O)}$	Any Output to Any Output Skew <sup>[14]</sup>				100	ps
$t_{PHASE}$	Phase Error <sup>[14]</sup>		-50		50	ps

**Ordering Information**

Part Number	Package Type	Product Flow
CY2SSTV857ZC-27	48-pin TSSOP	Commercial, $0^\circ$ to $70^\circ\text{C}$
CY2SSTV857ZC-27T	48-pin TSSOP—Tape and Reel	Commercial, $0^\circ$ to $70^\circ\text{C}$
CY2SSTV857ZI-27	48-pin TSSOP	Industrial, $-40^\circ$ to $+85^\circ\text{C}$
CY2SSTV857ZI-27T	48-pin TSSOP—Tape and Reel	Industrial, $-40^\circ$ to $+85^\circ\text{C}$

**Package Drawing and Dimension**

**48-lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z48**

51-85059-1B

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**Notes:**

12. Refers to transition of non-inverting output.

13. Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.

14. All differential input and output terminals are terminated with  $120\Omega/16\text{ pF}$ , as shown in *Figure 5*.

**Document History Page**

<b>Document Title: CY2SSTV857-27 Differential Clock Buffer/Driver</b> <b>DDR333/PC2700-Compliant,DDR333/PC2700-Compliant</b> <b>Document #: 38-07464</b>				
<b>Rev.</b>	<b>ECN No.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	117657	09/09/02	HWT	New Data Sheet
*A	118942	10/21/02	RGL	Overlooked in initial release needed to add Pin 15 to the Pin Description table
*B	121274	11/12/02	RGL	Corrected the typo error in the title
*C	122937	12/21/02	RBI	Add power up requirements to maximum rating information
*D	127010	05/27/03	RGL	Changed the operating frequency from 60–170 MHz to 60–200 MHz Added 333-MHz DDR SDRAM support Changed OE pin to PD#
*E	129270	10/22/03	RGL	Changed PD to PD# Removed the “and DDR266/PC2100” from the title Changed the part number from “CY2SSTV857” to “CY2SSTV857-27” Changed “Commercial Temp of 0°C to 70° C” to “Industrial Temp of –40° to +85° C” Added Industrial Temp part numbers to Ordering information
*F	202540	See ECN	RGL	Corrected typo error -Cycle-to-cycle Jitter ( $T_{CCJ}$ ) max. value from 7.5ps to 75ps