

High Performance 256x8 PROM TiW PROM Family

53/63S280 53/63S281 53/63S281A

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Features/Benefits

- 28 ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantees greater than 98% programming yields
- Low-voltage generic programming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current
- Open collector or three-state outputs

Applications

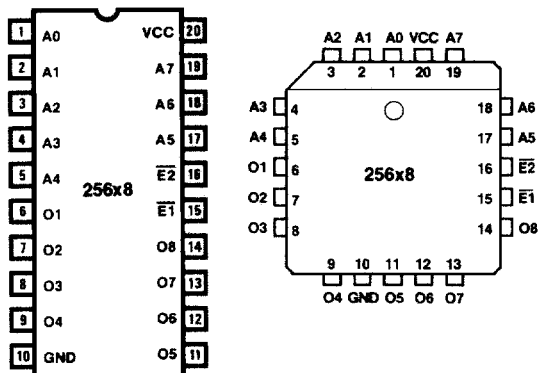
- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 inputs, 8 outputs, and 256 product terms per output

Selection Guide

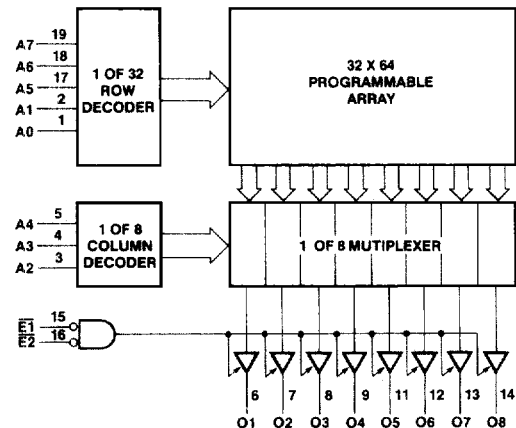
MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
2K	256x8	20	N,J NLL* W*	TS	Enhanced	63S281A	53S281A
				OC	Standard	63S281	53S281
						63S280	53S280

*Contact factory for package dimensions.

Pin Configurations



Block Diagram



PLE™ is a trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT	
V_{IL}	Low-level input voltage	Guaranteed input logical low voltage for all inputs††				0.8	V	
V_{IH}	High-level input voltage	Guaranteed input logical high voltage for all inputs††		2			V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	Com		0.45	V	
				Mil		0.5		
V_{OH}	High-level output voltage*	$V_{CC} = \text{MIN}$	Com $I_{OH} = -3.2 \text{ mA}$	2.4			V	
			Mil $I_{OH} = -2 \text{ mA}$					
I_{OZL}	Off-state output current*	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	μA	
I_{OZH}			$V_O = 2.4 \text{ V}$			40		
I_{CEX}	Open collector output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$			40	μA	
			$V_O = 5.5 \text{ V}$			100		
I_{OS}	Output short-circuit current**	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$			-20	-90	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$. All inputs grounded. All outputs open.				90	140	mA

Switching Characteristics Over Operating Conditions (See standard test load)

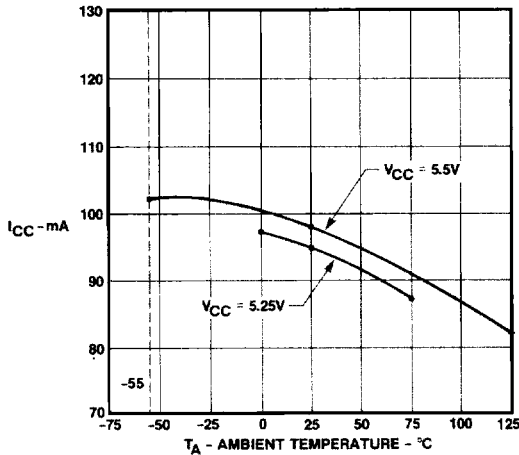
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
		COMMERCIAL	63S281A	21	28	
	63S280, 63S281	21	45	18	25	
MILITARY	53S281A	21	40	18	30	
	53S280, 53S281	21	50	18	30	

* Three-state only. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

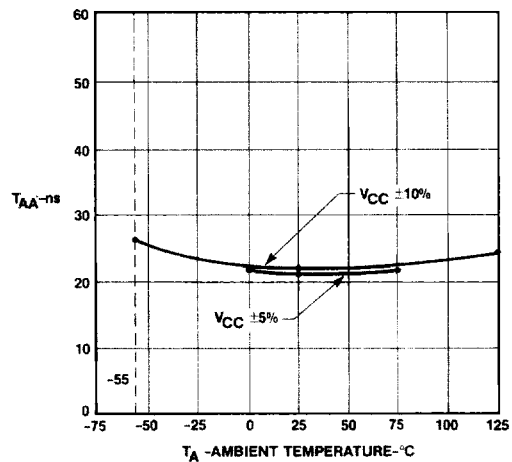
† Typical at 5.0 V V_{CC} and 25°C T_A .

†† V_{IL} and V_{IH} limits are absolute values with respect to the device ground pin(s) and includes all overshoots due to test equipment noise.

Typical I_{CC} vs Temperature

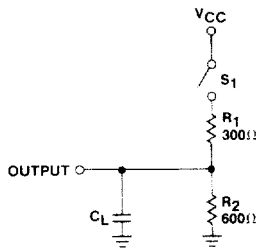


Typical T_{AA} vs Temperature



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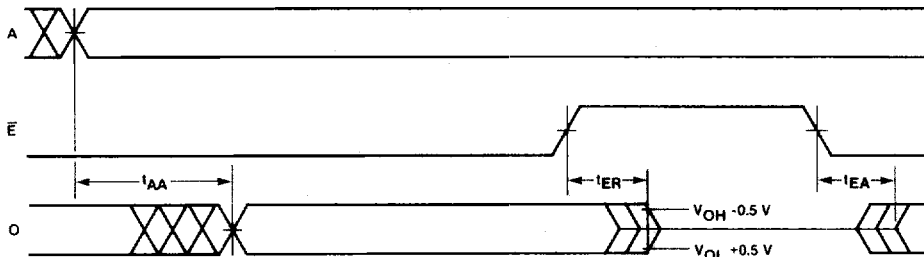
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



- NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 3. Input access measured at the 1.5 V level.
 4. t_{AA} is tested with switch S_1 closed, $C_L = 30$ pF and measured at 1.5 V output level.
 5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and $C_L = 30$ pF.
 6. For three-state devices, TEA is measured at the 1.5 V output level with $C_L = 30$ pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
 TER is tested with $C_L = 5$ pF. S_1 is open for "1" to high-impedance test, measured at $V_{OH} = -0.5$ V output level, S_1 is closed for "0" to high-impedance test measured at $V_{OL} = -0.5$ V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular

routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94063

Digitec Inc.
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089

Metal Mask Layout

