8-Input universal shift/storage register (3-State) 54F299

FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes; Shift left, shift right, load and store
- 3-State outputs for bus-oriented applications

DESCRIPTION

The 54F299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 54F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. the type of operation is determined by S0 and S1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

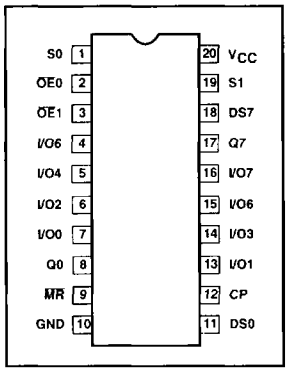
A High signal on either OE0 or OE1 disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S0 and S1 in preparation for a parallel load operation.

ORDERING INFORMATION

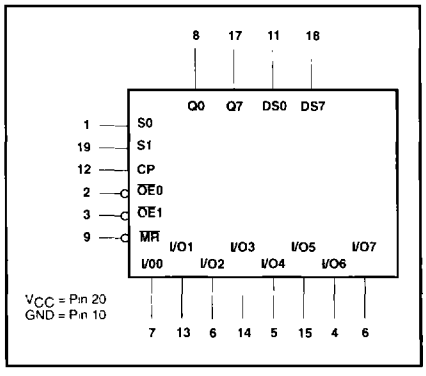
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54F299/BRA	GDIP1-T20
20-Pin Flat Pack	54F299/BSA	GDFP2-F20
20-Pin Ceramic LLCC	54F299/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

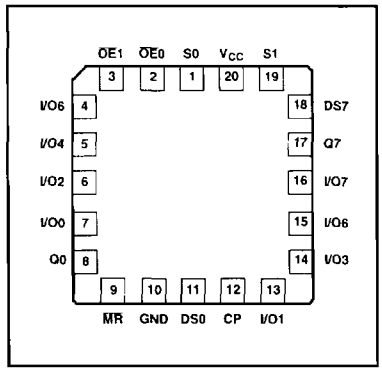
PIN CONFIGURATION



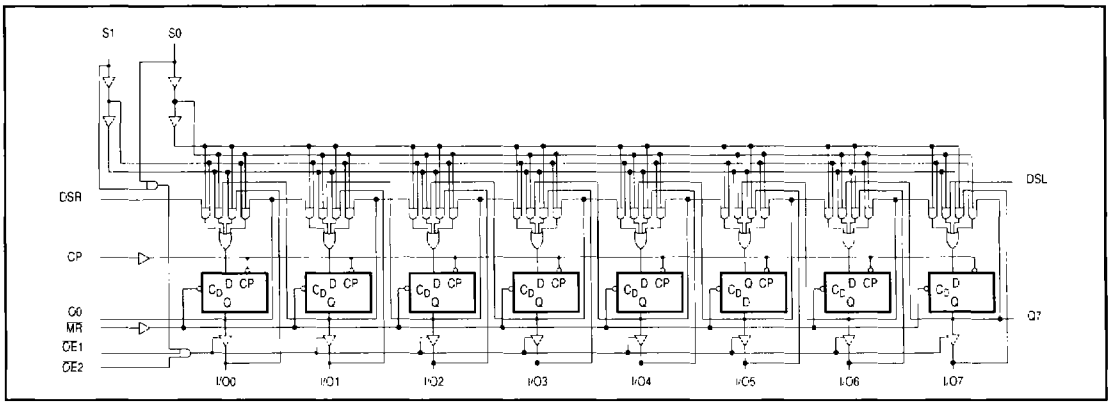
LOGIC SYMBOL



LLCC LEAD CONFIGURATION



LOGIC DIAGRAM



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
DS0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S0, S1	Mode select inputs	1.0/2.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
I/On	Parallel data inputs or 3-State parallel outputs	3.5/1.0 150/33	70µA/0.6mA 3.0mA/20mA
Q0, Q7	Serial outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High State and 0.6mA in the Low state.

FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{MR}$	$\overline{OE}$n	S1	S0	CP	
L	L	X	X	X	Asynchronous Reset; Q0 - Q7 = Low
H	L	H	H	↑	Parallel load; I/On → Qn
H	L	L	H	↑	Shift right; DS0 → Q0, Q0 → Q1, etc.
H	L	H	L	↑	Shift left; DS7 → Q7, Q7 → Q6, etc.
H	L	L	L	X	Hold
X	H	X	X	X	Outputs Disabled

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	Q0 - Q7	40	mA
		I/On	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q0, Q7			-1	mA
		I/On			-3	mA
I_{OL}	Low-level output current	Q0, Q7			28	mA
		I/On			20	mA
T_{amb}	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Q0, Q7	V_{CC} = MIN, V_{IL} = MAX	I_{OH} = -1mA	2.5			V
		I/On	V_{IH} = MIN	I_{OH} = -3mA	2.4			V
				I_{OH} = -1mA	2.5	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN			.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	others	V_{CC} = 0V, V_I = 7.0V				100	µA
		I/On	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others				-0.4	-0.6	mA
I_{OZH} + I_{IH}	Off-state output current High-level voltage applied	I/On only	V_{CC} = MAX, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current Low-level voltage applied	I/On only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	85	mA
		I_{CCL}				64	85	mA
		I_{CCZ}				60	85	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	85	115		85[4]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q0 or Q7	Waveform 1	3.5 4.5	5.0 6.0	7.0 8.0	3.5 4.5	9.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to I/On	Waveform 1	4.0 5.0	6.0 6.5	9.0 9.0	4.0 5.0	11.0 11.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q0 or Q7	Waveform 2	5.5	7.5	9.5	5.5	11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/On	Waveform 2	5.5	7.5	10.0	5.5	11.5	ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/On	Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	10.0 12.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/On	Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	9.0 7.5	ns ns

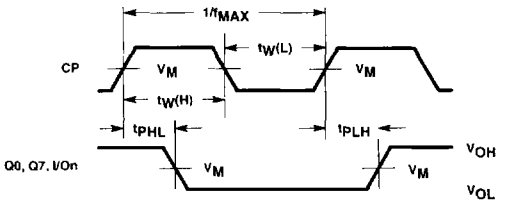
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low S0 or S1 to CP	Waveform 3	7.0 5.0			8.5 7.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low S0 or S1 to CP	Waveform 3	0 0			0 0		ns ns
t_s(H) t_s(L)	Set-up time, High or Low I/On, DS0 or DS1 to CP	Waveform 3	3.0 3.0			3.0 4.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low I/On, DS0, or DS1 to CP	Waveform 3	0 0			1.5 1.5		ns ns
t_w[5]	CP Pulse width	Waveform 1	4.0			4.0		ns
t_w(L)[5]	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

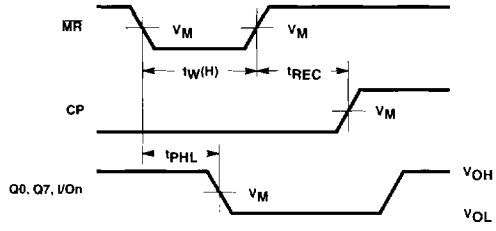
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Guaranteed and not tested parameter.
5. Pulse widths are guaranteed to 4.0ns, but are tested only to 7.0ns.

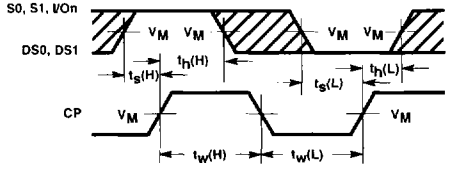
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency

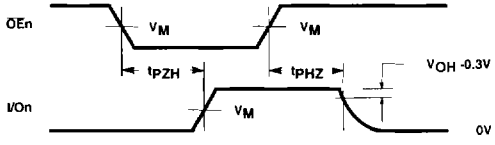


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.

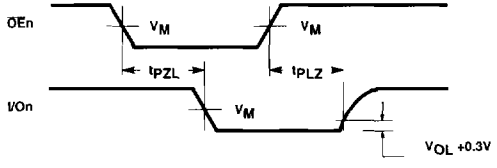


The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data and Select Setup and Hold Times



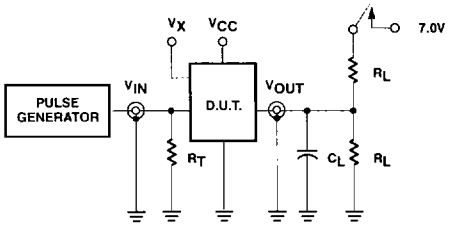
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



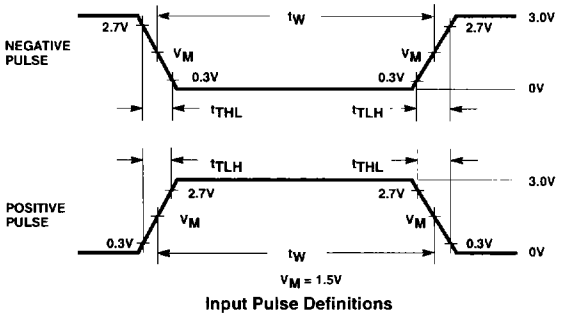
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.