Document Title

1Mx16 bit Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	October 17, 2002	Advanced

1M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 1M x16 bit
- Power Supply Voltage: 1.7V~2.2V
- Three State Outputs
- Compatible with Low Power SRAM
- Dual Chip selection support
- Package Type: 48-TBGA-6.00x7.00

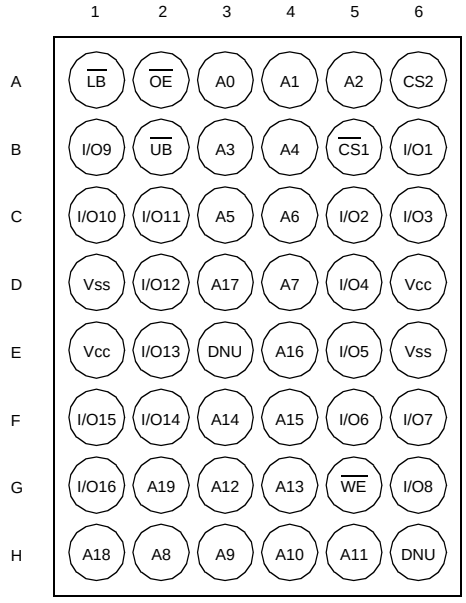
GENERAL DESCRIPTION

The K1S1616B1M is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports Industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports dual chip selection for user interface.

PRODUCT FAMILY

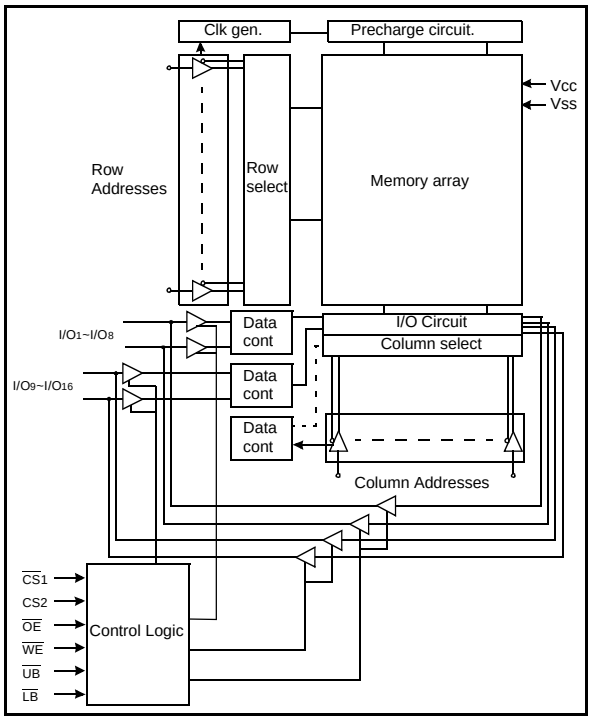
Product Family	Operating Temp.	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)	
K1S1616B1M-I	Industrial(-40~85°C)	1.7V~2.2V	70/85ns	60µA	25mA	48-TBGA-6.00x7.00

PIN DESCRIPTION



48-TBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS}$1,CS2	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
A_0~A_{19}	Address Inputs	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
I/O_1~I/O_{16}	Data Inputs/Outputs	DNU	Do Not Use[1)]

1) Reserved for future use.

PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	**Function**
K1S1616B1M-EI70 K1S1616B1M-EI85	48-TBGA-6.00x7.00, 70ns 48-TBGA-6.00x7.00, 85ns

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=1.7V) for a minimum 200μs with $\overline{CS1}$=high.or CS2=low.
3. Issue read operation at least twice.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	X[1)]	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	1.7V	1.8V	2.2V	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	1.4	-	V_{CC}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

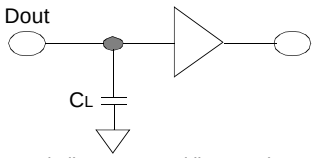
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	5	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS1}$=V_{IL}, CS2=V_{IH} $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}	-	-	25	mA
Output low voltage	V_{OL}	I_{OL} = 0.1mA	-	-	0.2	V
Output high voltage	V_{OH}	I_{OH} = -0.1mA	1.4	-	-	V
Standby Current(CMOS)	I_{SB1}	Other inputs=0~Vcc 1) $\overline{CS1}$≥V_{CC}-0.2V, CS2≥V_{CC}-0.2V($\overline{CS1}$ controlled) or 2) 0V ≤ CS2 ≤ 0.2V(CS2 controlled)	-	-	60	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to Vcc-0.2V
Input rising and falling time: 5ns
Input and output reference voltage: 0.5 x V_{CC}
Output load (See right): C_L=50pF



1. Including scope and jig capacitance

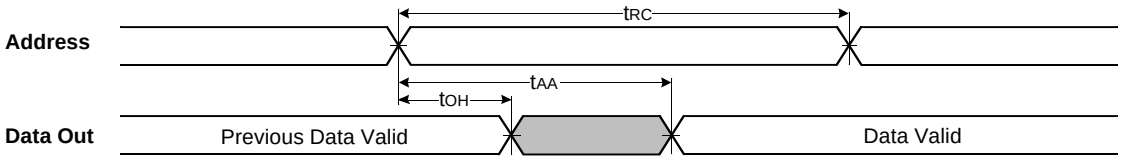
AC CHARACTERISTICS(V_{CC}=1.7~2.2V, T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	85	-	ns
	Address Access Time	t_{AA}	-	70	-	85	ns
	Chip Select to Output	t_{CO}	-	70	-	85	ns
	Output Enable to Valid Output	t_{OE}	-	35	-	40	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	-	85	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	70	-	85	-	ns
	Chip Select to End of Write	t_{CW}	60	-	70	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	70	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	60[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

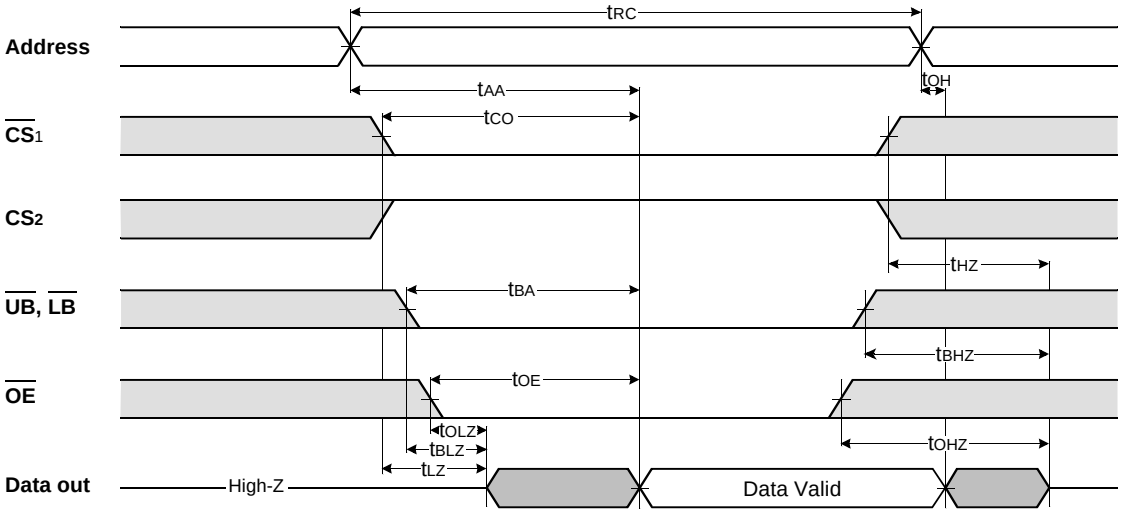
1. t_{WP}(min)=70ns for continuous write operation over 50 times.(Only in case of $\overline{WE}$ controlled write operation)

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



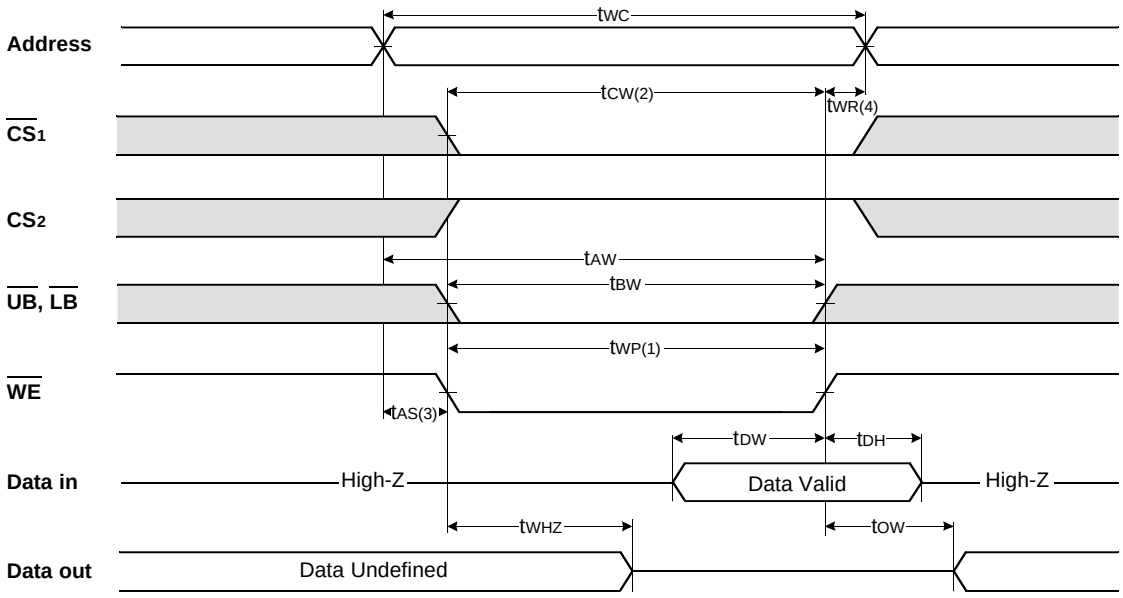
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



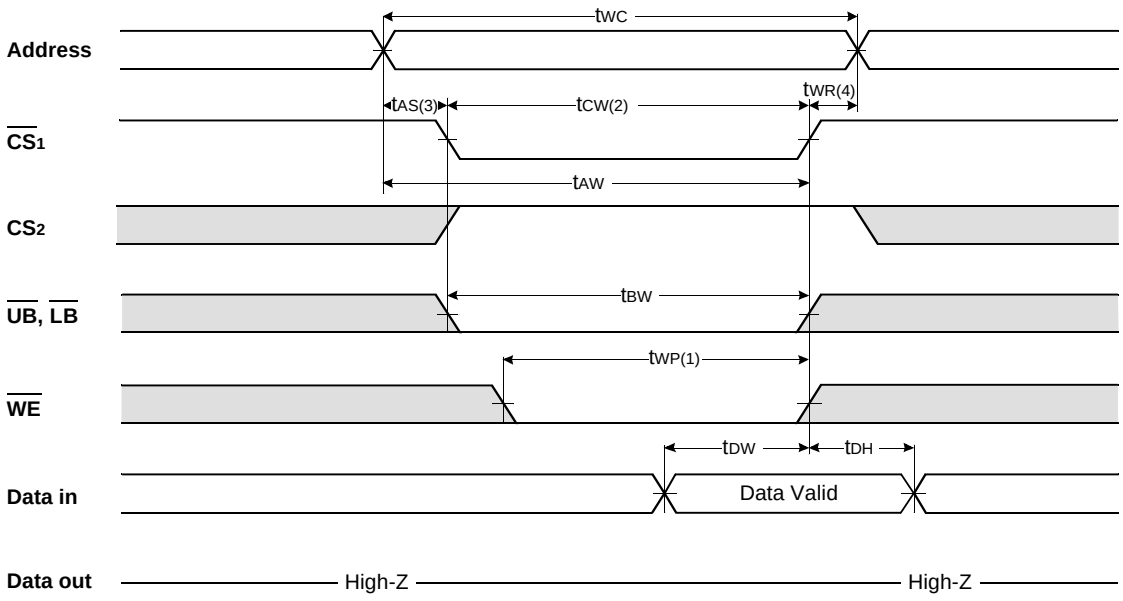
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

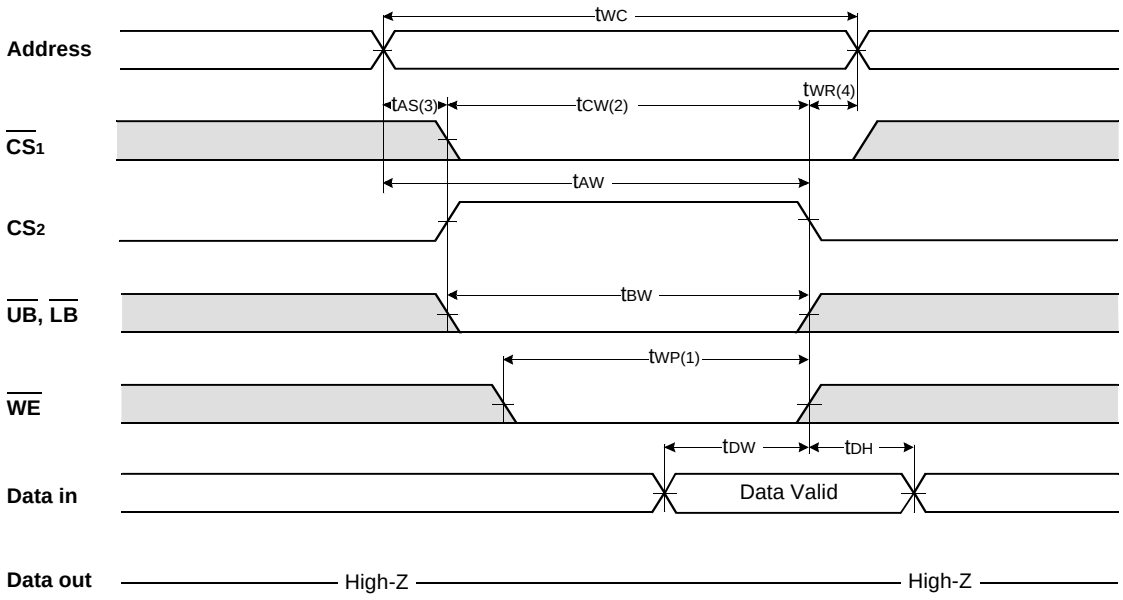
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



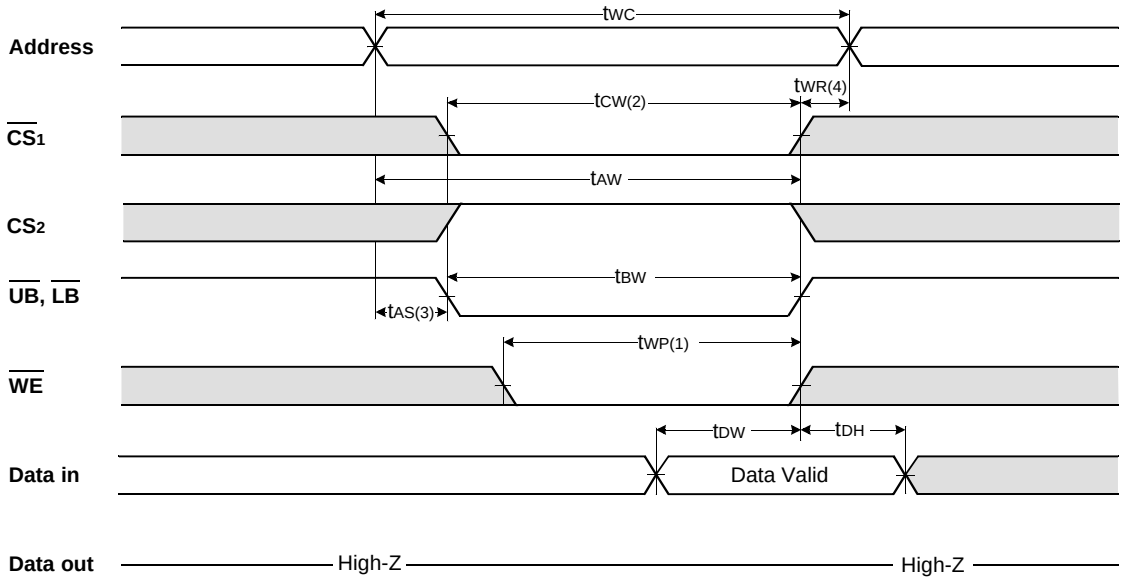
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



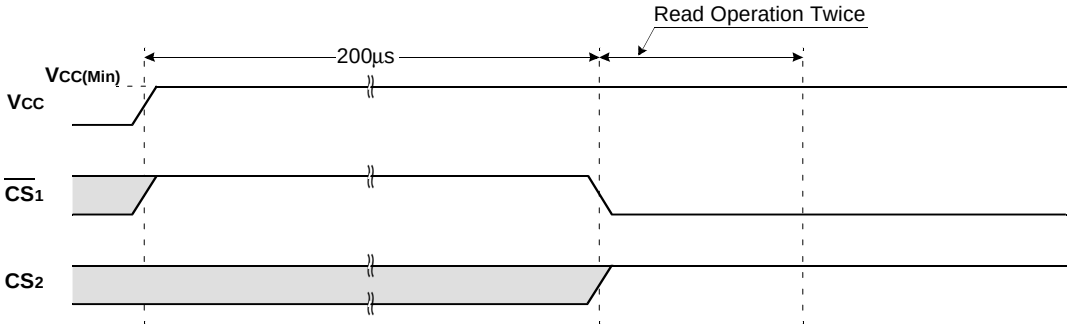
TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or $\overline{WE}$ going high.

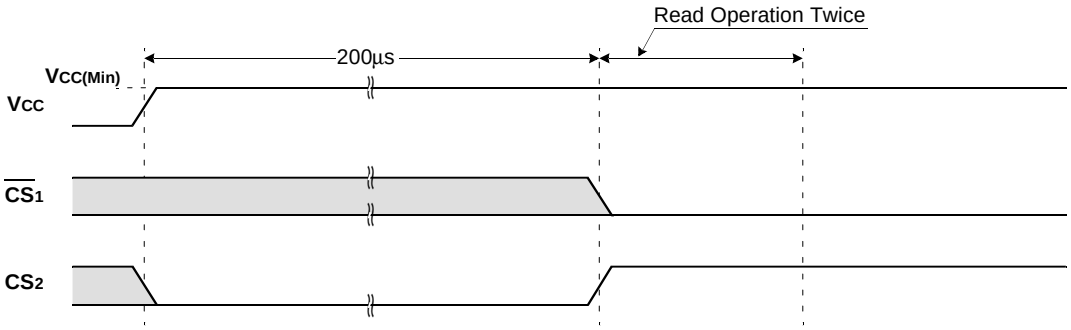
TIMING WAVEFORM OF POWER UP(1) ($\overline{CS_1}$ controlled)



POWER UP(1)

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs with $\overline{CS_1}$ high and then toggle $\overline{CS_1}$ low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed after toggling $\overline{CS_1}$ pin low.
3. The read operation must satisfy the specified t_{RC}.

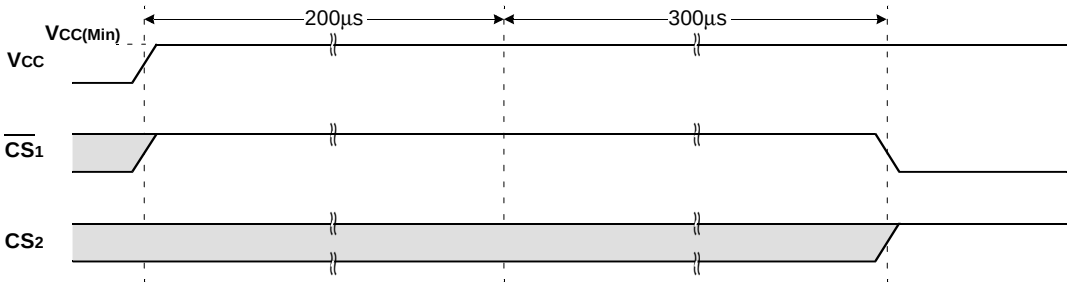
TIMING WAVEFORM OF POWER UP(2) (CS_2 controlled)



POWER UP(2)

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs with CS_2 high and then toggle CS_2 low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed after toggling CS_2 pin low.
3. The read operation must satisfy the specified t_{RC}.

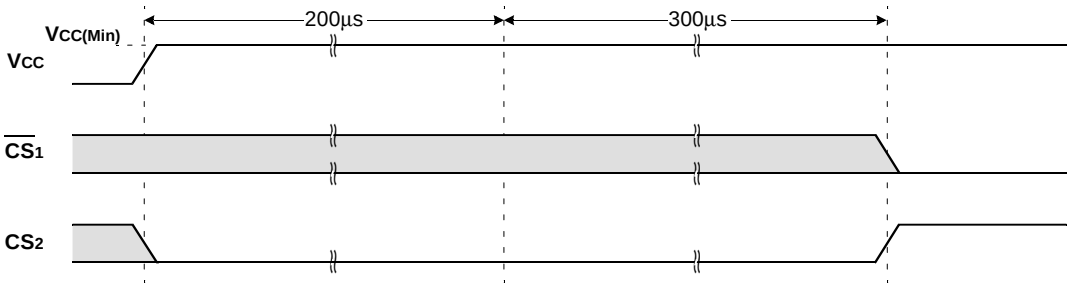
TIMING WAVEFORM OF POWER UP(3) ($\overline{CS_1}$ controlled)



POWER UP(3)

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs and wait another 300µs with $\overline{CS_1}$ high if you dont want to commit dummy read cycle. After total 500µs wait, toggle $\overline{CS_1}$ low, then you get into the normal mode.

TIMING WAVEFORM OF POWER UP(4) (CS_2 controlled)



POWER UP(4)

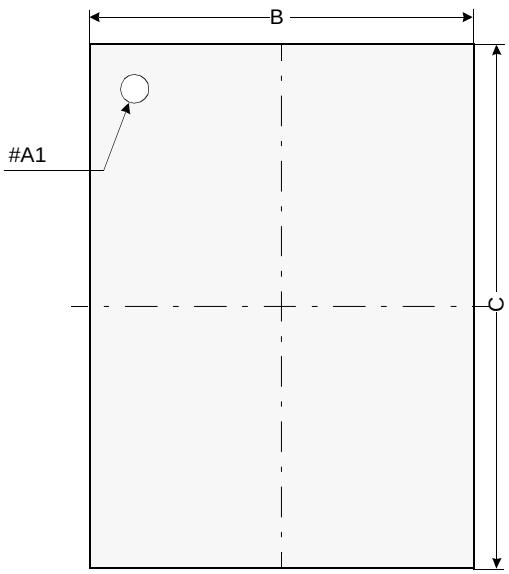
1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs and wait another 300µs with CS_2 low if you dont want to commit dummy read cycle. After total 500µs wait, toggle CS_2 high, then you get into the normal mode.

PACKAGE DIMENSION

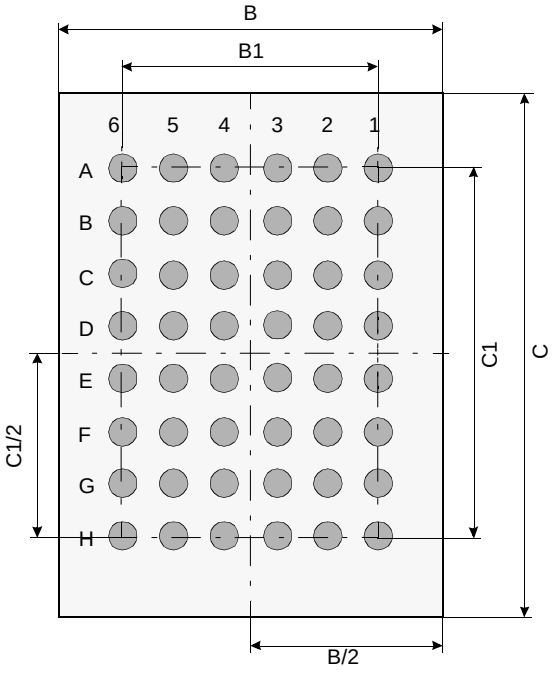
Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)

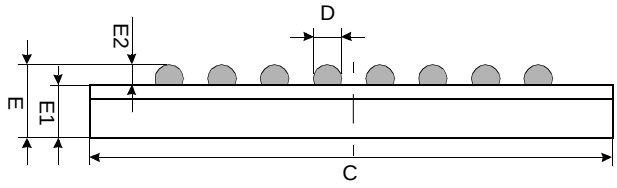
Top View



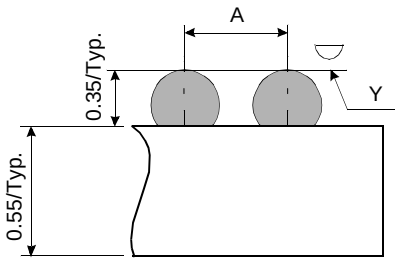
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)