FAIRCHILD

SEMICONDUCTOR®

November 2009

SuperFET ™

FCP11N60 / FCPF11N60 / FCPF11N60T

General Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.

Features

- 650V @ Tj = 150°C
- Typ. Rds(on) = 0.32Ω
- Ultra low gate charge (typ. Qg=40nC)
- Low effective output capacitance (typ. Coss.eff = 95pF)
- 100% avalanche tested
- RoHS Compliant

TO-220AB
FCP Series

G D S

TO-220F
FCPF Series

G D S

D

G

S
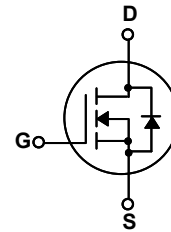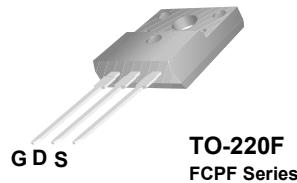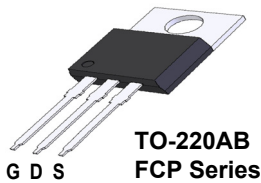
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FCP11N60	FCPF11N60(T)	Units
I_D	Drain Current	- Continuous (T_C = 25°C)		11	11*	A
		- Continuous (T_C = 100°C)		7	7*	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	33	33*	A
V_{GSS}	Gate-Source Voltage			± 30		V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	340		mJ
I_{AR}	Avalanche Current		(Note 1)	11		A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	12.5		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25°C)			125	36	W
	- Derate above 25°C			1.0	0.29	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300		°C

* Drain current limited by maximum junction termperature.

Thermal Characteristics

Symbol	Parameter	FCP11N60	FCPF11N60(T)	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	3.5	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Elerical Characteristics $T_C = 25°C$ unless otherwise noted

<div style="text-align:right">FCP11N60 / FCPF11N60 / FCPF11N60T</div>

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA, $T_J = 25°C$	600	--	--	V
		$V_{GS} = 0$ V, $I_D = 250$ μA, $T_J = 150°C$	--	650	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.6	--	V/°C
BV_{DS}	Drain-Source Avalanche Break-down Voltage	$V_{GS} = 0$ V, $I_D = 11$ A	--	700	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 480$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 5.5$ A	--	0.32	0.38	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40$ V, $I_D = 5.5$ A (Note 4)	--	9.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	1148	1490	pF
C_{oss}	Output Capacitance		--	671	870	pF
C_{rss}	Reverse Transfer Capacitance		--	63	82	pF
C_{oss}	Output Capacitance	$V_{DS} = 480$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	35	--	pF
C_{oss} eff.	Effective Output Capacitance	$V_{DS} = 0$V to 480 V, $V_{GS} = 0$ V	--	95	--	pF
ESR	Equivalent Series Resistance	Drain Open, f=1MHz	--	2.5	--	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300$ V, $I_D = 11$ A, $R_G = 25$ Ω	--	34	80	ns
t_r	Turn-On Rise Time		--	98	205	ns
$t_{d(off)}$	Turn-Off Delay Time		--	119	250	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	56	120	ns
Q_g	Total Gate Charge	$V_{DS} = 480$ V, $I_D = 11$ A, $V_{GS} = 10$ V	--	40	52	nC
Q_{gs}	Gate-Source Charge		--	7.2	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	21	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	33	A
V_{SD}	Drain-Source Diode Forward Volt-age	$V_{GS} = 0$ V, $I_S = 11$ A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 11$ A, $dI_F / dt = 100$ A/μs	--	390	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	--	5.7	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS} = 5.5$A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 11$A, di/dt ≤ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature
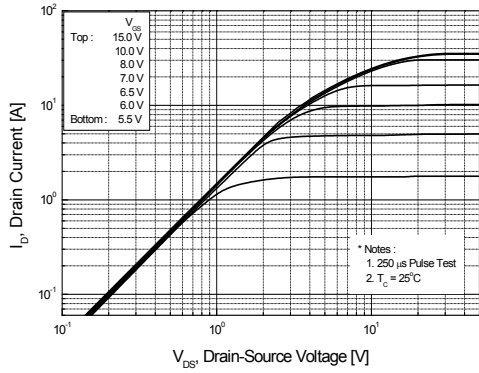
Typical Characteristics
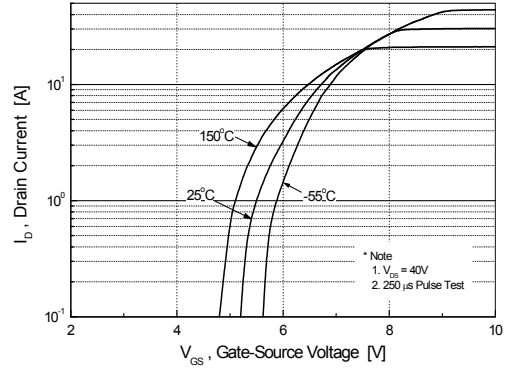
Figure 1. On-Region Characteristics
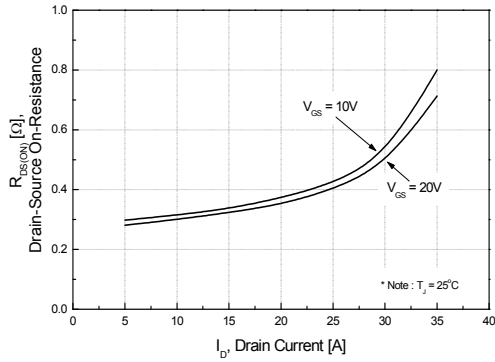

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs.
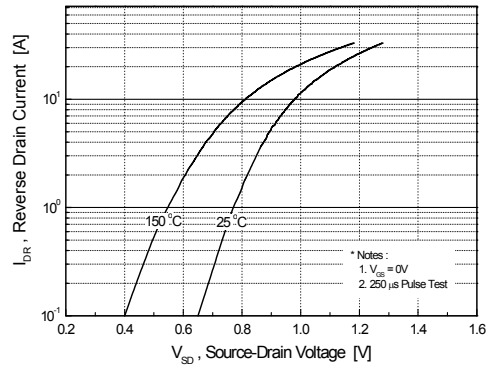Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
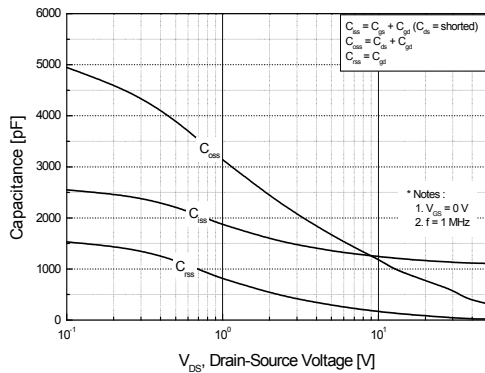Variation vs. Source Current
and Temperature

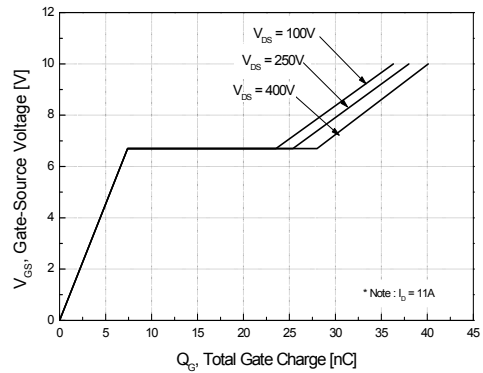Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

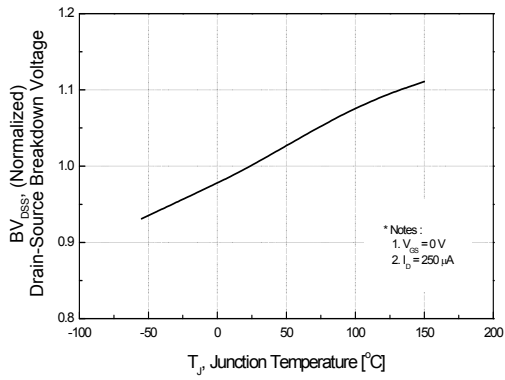## Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation
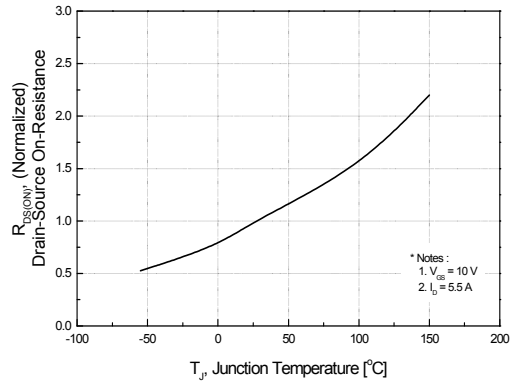vs. Temperature

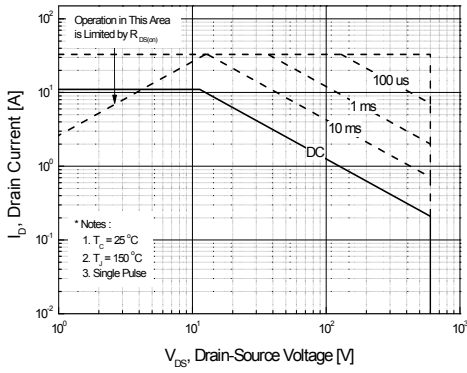Figure 8. On-Resistance Variation
vs. Temperature

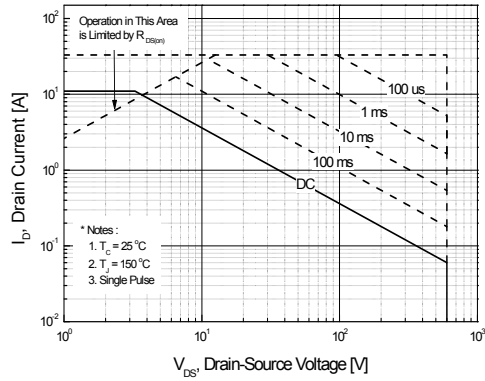Figure 9-1. Maximum Safe Operating Area
for FCP11N60

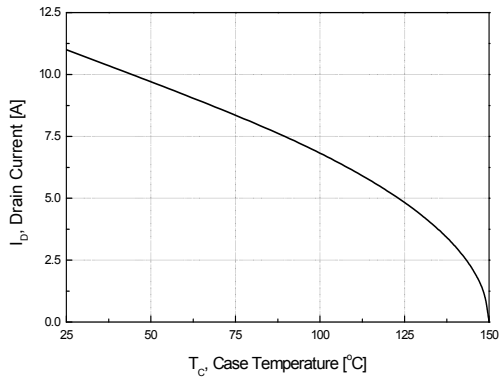Figure 9-2. Maximum Safe Operating Area
for FCPF11N60(T)

Figure 10. Maximum Drain Current
vs. Case Temperature
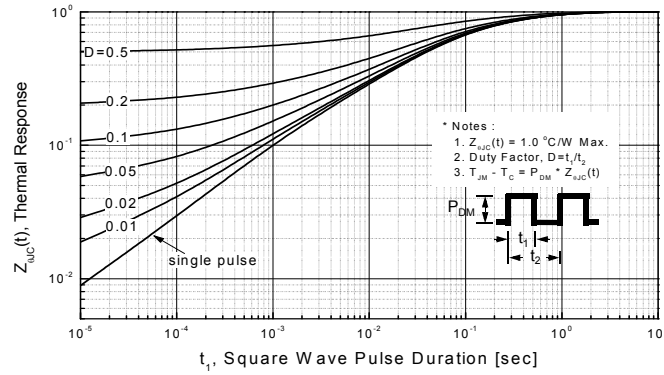
Typical Characteristics (Continued)

* Notes :
1. $Z_{\theta JC}(t)$ = 1.0 °C/W Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 11-1. Transient Thermal Response Curve for FCP11N60

* Notes :
1. $Z_{\theta JC}(t)$ = 3.5 °C/W Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
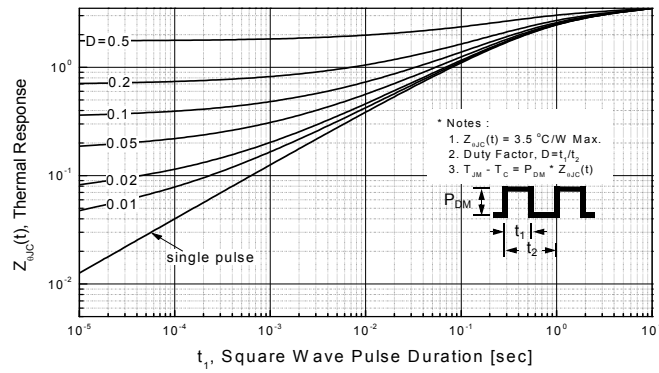
Figure 11-2. Transient Thermal Response Curve for FCPF11N60(T)

Gate Charge Test Circuit & Waveform

12V 200nF 50KΩ 300nF Same Type as DUT

V_{GS}

3mA DUT

V_{DS}

V_{GS} 10V Q_g Q_{gs} Q_{gd} Charge
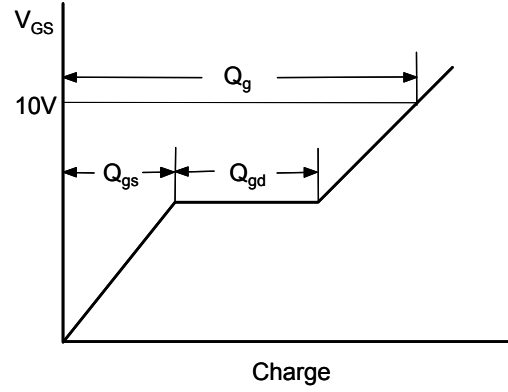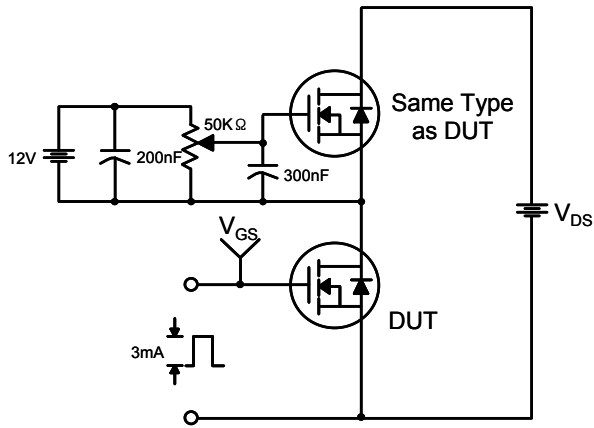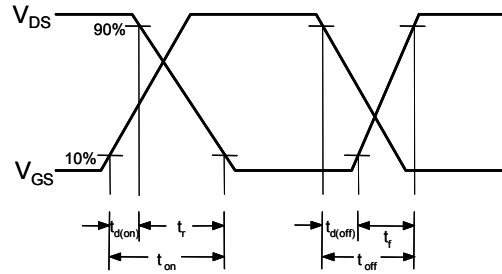
Resistive Switching Test Circuit & Waveforms

R_L V_{DS} V_{GS} V_{DD} R_G 10V DUT

V_{DS} 90% V_{GS} 10% $t_{d(on)}$ t_r t_{on} $t_{d(off)}$ t_f t_{off}
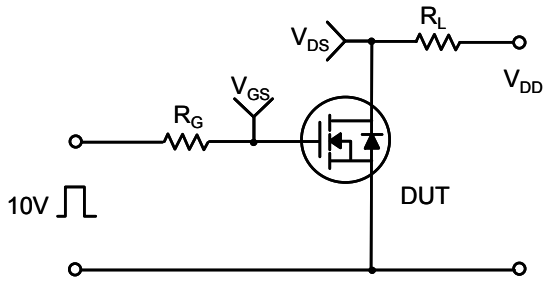
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} L I_D R_G V_{DD} 10V t_p DUT

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS} I_{AS} $I_D(t)$ V_{DD} $V_{DS}(t)$ t_p Time
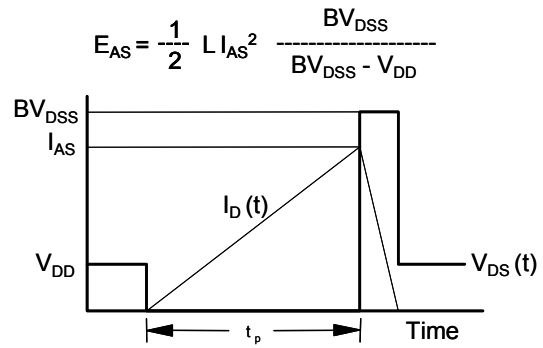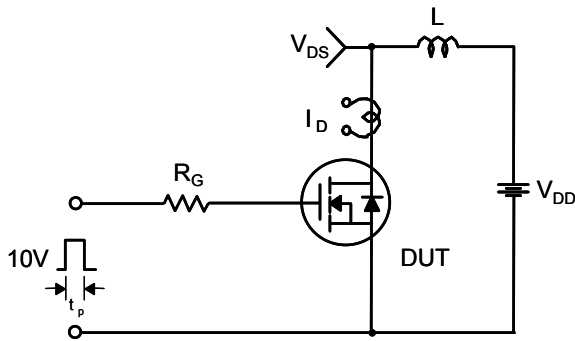
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{GS}

V_{DD}

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Mechanical Dimensions

TO-220AB

Ø4.09
3.50

⊕ 0.36 Ⓜ B AⓂ

A

10,67
9,65

3,43
2,54

16,51
14,22

△9,40
8,38

1 2 3

6,35 MAX

C

14,73
12,70

(1,91)

1,78
1,14

1,02
0,38

2,54

⊕ 0.36 Ⓜ B AⓂ

5,08

4,83
3,56

B

"A1"

7°
3°

6,86
5,84

5°
3°

5°
3°

0,61
△0,33

2,92
2,03

8,89
6,86

△13,40
12,19

3 2 1

5°
3°

5°
3°

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K,
   VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY
   (LOWER LEFT CORNER, LOWER CENTER
   AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
   SINGLE GAUGE = 0,51 - 0,61
   DUAL GAUGE   = 1,14 - 1,40
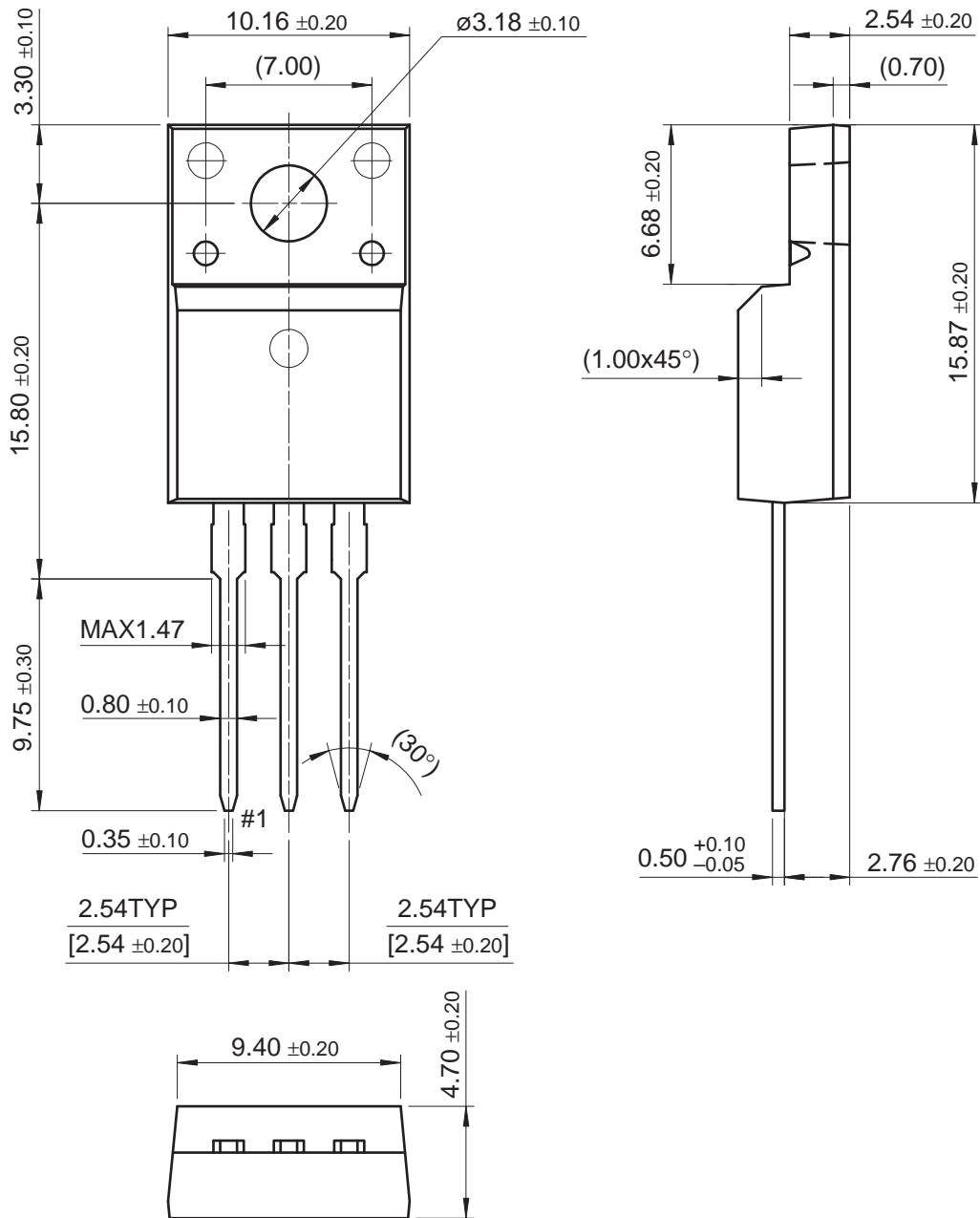G) DRAWING FILE NAME: TO220B03REV6

Dimensions in Millimeters

Mechanical Dimensions

TO-220F

10.16 ±0.20
(7.00)
ø3.18 ±0.10
3.30 ±0.10
15.80 ±0.20
MAX1.47
0.80 ±0.10
(30°)
9.75 ±0.30
0.35 ±0.10
#1
2.54TYP
[2.54 ±0.20]
2.54TYP
[2.54 ±0.20]

2.54 ±0.20
(0.70)
6.68 ±0.20
15.87 ±0.20
(1.00x45°)
0.50 +0.10 −0.05
2.76 ±0.20

9.40 ±0.20
4.70 ±0.20

Dimensions in Millimeters

Rev. B2, October 2003

Package Dimensions

TO-220F Potted

Ø3.18±0.10
10.16±0.20
(7.00)
3.30±0.10
Potting
(5.40)
15.80±0.20
MAX1.47
0.70±0.10
30°
#1
0.35±0.10
2.54TYP
[2.54±0.20]
2.54TYP
[2.54±0.20]
9.75±0.20

2.54±0.20
(0.70)
6.70±0.20
A* (Potting)
(1.00x45°)
15.90±0.20
0.50±0.10/0.05
2.76±0.20

9.40±0.20
4.70±0.20
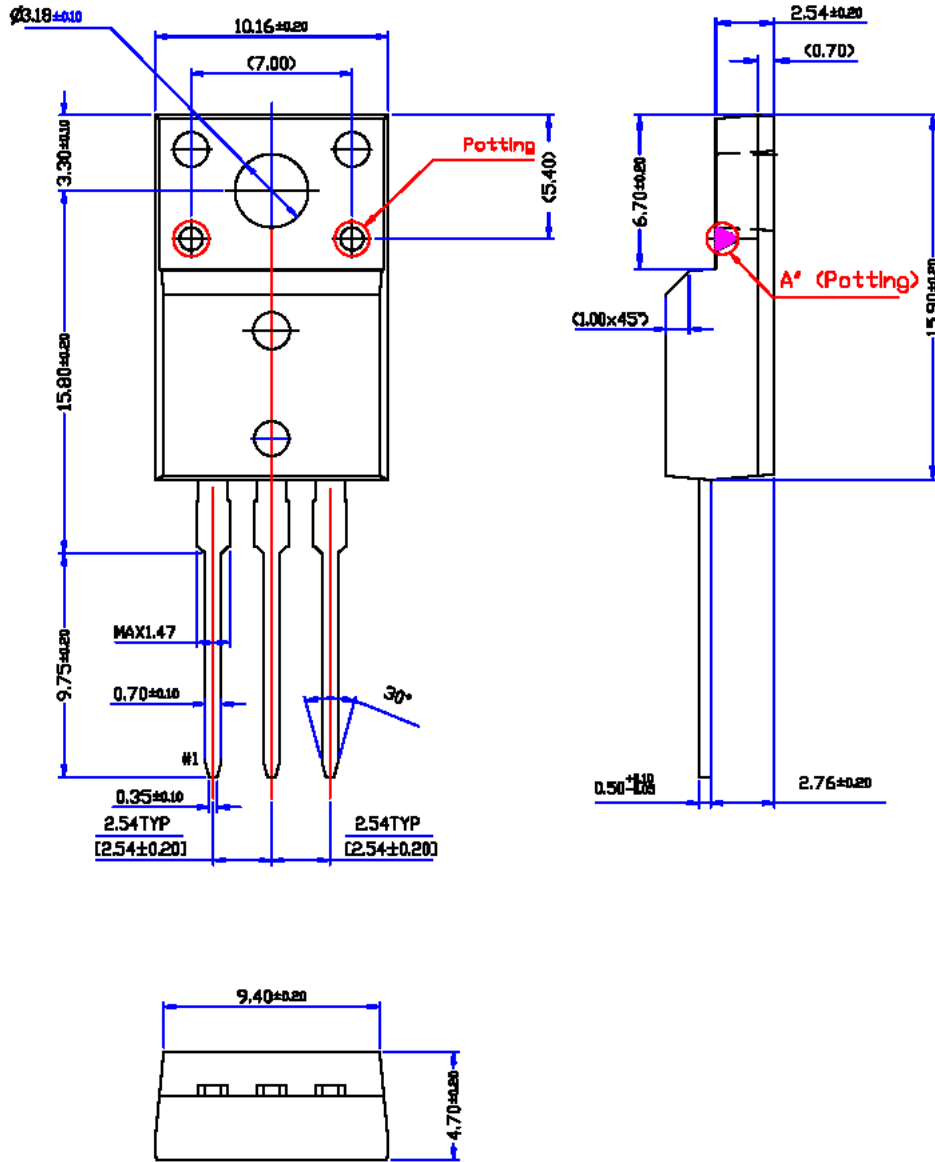
* Front/Back Side Isolation Voltage : AC 2500V

Dimensions in Millimeters

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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