**DATEL**

## FEATURES

- Microprocessor-compatible
- ± ½ LSB total adjustment error
- 100 Microseconds conversion time
- Differential analog inputs
- Ratiometric operation
- Single-supply operation

## GENERAL DESCRIPTION

DATEL's ADC-830 is a low cost, 8-bit, CMOS A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. The ADC-830's digital control inputs, CS, RD, and WR, are active low, and are available in all microprocessor memory systems. Upon completion of a conversion, an Interrupt signal is generated at the converter's output. The ADC-830 will operate as a normal A/D for non-microprocessor based applications.

Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8-bit conversion in 100 microseconds with a maximum total adjusted error of only ± ½ LSB. No zero adjust is required. Also, the differential analog input allows the user to increase the common mode rejection and offset the zero value of the analog input.

Other features include single supply operation and an internal clock generator. The clock generator requires only an external RC network or, it may be driven by an external clock. The clock frequency range is 100 kHz to 1.2 MHz. In addition, the ADC-830 operates ratiometrically or with a 2.5V dc, 5V dc, or, to allow the encoding of smaller analog input voltage ranges, an analog-span-adjusted reference.

The ADC-830 is packaged in 20-pin plastic DIP and operates over the 0°C to +70°C commercial temperature range. Power requirement is +5V dc. With it's combination of low cost, small size, ease of digital interfacing, and versatility of analog interfacing, the ADC-830 is the ideal choice for many process control and instrumentation applications.
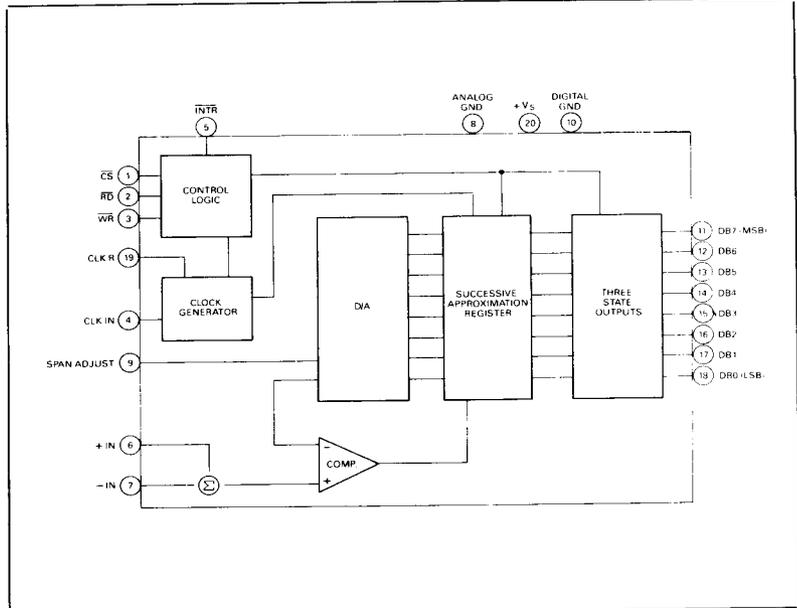


## MECHANICAL DIMENSIONS
## INCHES (MM)



**DATEL**
**ADC-830**
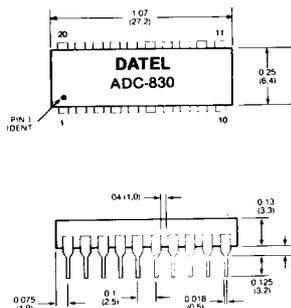
## INPUT/OUTPUT
## CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|----------|-----|----------|
| 1 | CS (CHIP SELECT) | 11 | DB 7 (MSB) |
| 2 | RD (READ STROBE) | 12 | DB 6 |
| 3 | WR (WRITE STROBE) | 13 | DB 5 |
| 4 | CLOCK IN | 14 | DB 4 |
| 5 | INTERRUPT | 15 | DB 3 |
| 6 | + ANALOG IN | 16 | DB 2 |
| 7 | – ANALOG IN | 17 | DB 1 |
| 8 | ANALOG GROUND | 18 | DB 0 (LSB) |
| 9 | SPAN ADJUST | 19 | CLOCK RETURN |
| 10 | DIGITAL GROUND | 20 | + V SUPPLY |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | +6.5V |
| Digital Input Voltage | −0.3V to +18V |
| Analog Input Voltage | −0.3V to (V$_S$ +0.3V) |
| Package Dissipation | 875 mW |

## FUNCTIONAL SPECIFICATIONS
**Typical at +25°C, +5V dc supply voltage, unless otherwise noted.**

### ANALOG INPUTS

| | |
|---|---|
| Analog Input Range[1] | −0.05V to +V$_S$ +0.05V |
| Common Mode Voltage Range | Gnd to +V$_S$ |
| Common Mode Rejection, dc, max. | ±2.44 mV |
| Input Resistance, Span Adjust, min. | 2.5 kΩ |

### DIGITAL INPUTS

| | |
|---|---|
| Input Logic Level, Vin ("1")[2] | +2.0V min. to +15V max. |
| Input Logic Level, Vin("0")[3] | +0.8V max. |
| Clock IN Threshold Voltage[4], Pos. | +2.7V min. to +3.5V max. |
| Neg. | +1.5V min. to +2.1V max. |
| Clock IN Hysteresis[4] | +0.6V min. to +2.0V max. |
| $\overline{CS}$ (Chip Select) | Active low state, enables the ADC-830 for read and write operations. |
| $\overline{WR}$ (Write Strobe) | Start conversion pulse. Input low of 100 nsec. min., in conjunction with a low on $\overline{CS}$, resets S.A.R. and shift register. |
| $\overline{RD}$ (Read Strobe) | Ouput enable pulse. Input low, in conjunction with a low on $\overline{CS}$, enables three-state outputs. Max. enable delay is 200 nsec. |
| Digital Input Capacitance, max. | 7.5 pF |

### DIGITAL OUTPUTS

| | |
|---|---|
| Parallel Output Data | 8 parallel lines of three-state, gateable output data. |
| $\overline{INT}$ (Interrupt) | Device status signal. Low when conversion complete. High when conversion in progress and when output data enabled. |
| Output Logic Level, Vout ("1")[5] | +2.4V min. at −360 µA |
| Vout ("0")[6] | +0.4V max. at 1.6 mA |
| Output Short Circuit Current, Gnd, min. | 4.5 mA |
| Vs., min. | 9.0 mA |
| Off-State Output Current | ±3 µA |
| Digital Output Capacitance, max. | 7.5 pF |

### PERFORMANCE

| | |
|---|---|
| Resolution | 8 binary bits |
| Total Adjusted Error[7], max. | ±½ LSB |
| Conversion Time[8] | 100 µsec. |
| Conversion Rate[9], max. | 8770 CPS |
| Clock Frequency Range[10] | 100 kHz to 1.2 MHz |
| Output Enable Delay[11], max. | 200 nsec. |
| Three-State Control Delay[12], max. | 250 nsec. |
| Interrupt Output Delay, max. | 450 nsec. |
| Power Supply Sensitivity[13] | ±2.44 mV |

### POWER REQUIREMENTS

| | |
|---|---|
| Supply Voltage Range | +4.5V dc to +6.3V dc |
| Supply Current, max. | 1.8 mA |

## PHYSICAL/ENVIRONMENTAL

| | |
|---|---|
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | −65°C to +150°C |
| Package Type | 20 pin plastic DIP |

### FOOTNOTES

1. When − Analog IN (Pin 7) is ≥ + Analog IN (Pin 6), the digital output code will be 0000 0000. Two internal diodes are connected to each analog input which will forward conduct for input voltages one diode drop below ground or above V$_S$.
2. V$_S$ = +5.25V dc, at V$_S$ = +5V dc, high level input current = 1 µA maximum.
3. V$_S$ = +4.75V dc, at V$_S$ = +5V dc, low level input current = 1 µA maximum.
4. Clock IN (Pin 4) is the input of a Schmitt Trigger circuit.
5. V$_S$ = +4.75V. For Vout ("1") = 4.5V high level output current = −10 µA.
6. V$_S$ = +4.75V. Low level output current for the Interrupt Output is 1.0 mA.
7. Specified after full-scale adjustment.
8. With an asynchronous start pulse, up to 8 clock periods may be required before conversion starts.
9. Conversion rate in free-running mode; $\overline{INTR}$ (Pin 5) connected to $\overline{WR}$ (Pin 3), CS (Pin 1) = 0V, and f$_{clk}$ = 740 kHz.
10. V$_S$ = +6V. Clock frequency range at V$_S$ = +5V is 100 kHz to 800 kHz.
11. C$_L$ = 100 pf, use bus driver for large C$_L$.
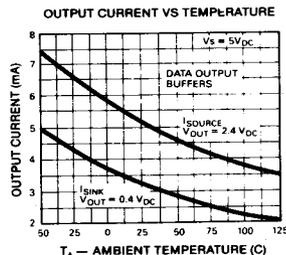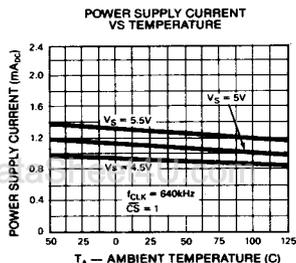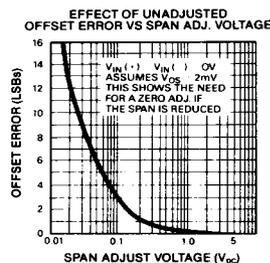12. C$_L$ = 10 pf, R$_L$ = 10 KΩ.
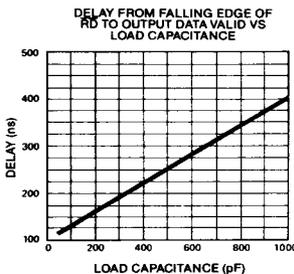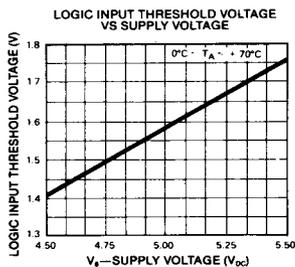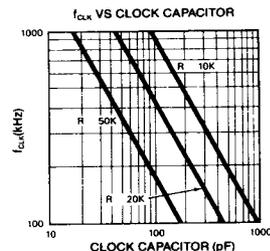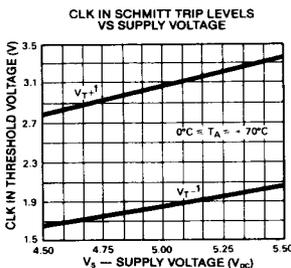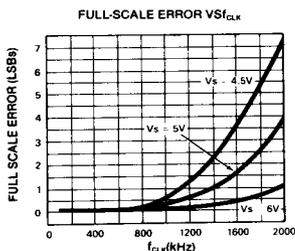13. V$_S$ = +5V ± 10% over full analog input range.

## TECHNICAL NOTES

1. The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) are active low to allow easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (Pin 1) can be grounded and the standard A/D START function is obtained by an active low pulse on the $\overline{WR}$ input (Pin 3) and the Output ENABLE function is obtained by an active low pulse on the $\overline{RD}$ input (Pin 2).

2. The ADC-830 has a differential analog voltage input (Pins 6 & 7). The switching time between the inputs is 4.5 clock periods. The maximum error voltage due to this sampling delay is $\Delta V_e$ (maximum) = $(V_P) (2\pi f_{cm}) (4.5/f_{clk})$ where: $\Delta V_e$ is the error voltage due to sampling delay, $V_P$ is the peak value of the common-mode voltage, and $f_{cm}$ is the common-mode frequency. Because of this internal switching action, displacement currents will flow at the analog inputs. These current transients occur at the leading edge of the internal clock, rapidly decay, and do not cause errors as the comparator is strobed at the end of the clock period. However, if the voltage source applied to Ana. IN + (Pin 6) exceeds V$_S$ by more than 50 mV, a large current may flow through a parasitic diode to V$_S$. If these currents could exceed 1 mA, an external diode should be connected between Ana. IN + (Pin 6) and V$_S$ (Pin 20).

3. The leads to the analog inputs should be kept as short as possible to prevent noise pickup. The source resistance for these inputs should be kept below 5 kΩ. Input bypass capacitors should not be used as they will average the transient input switching currents of the converter causing scale errors.

4. The ADC-830 may be used with a 5V, 2.5V or adjusted voltage reference. The reference is either ½ the value of $V_S$ or equal to a voltage applied to the span adjust pin (Pin 9). This allows for operation in either a ratiometric mode or an absolute mode. The internal gain for the span adjust input is 2.

5. The clock for the ADC-830 may be derived from the CPU or an external RC can be added to provide self clocking. A resistor ($\approx 10$ kΩ) is connected between CLK Return (Pin 19) and CLOCK IN (Pin 4) and a capacitor is connected between CLOCK IN and ground. The resultant clock frequency is $f_{clk}$ = 1/1.1 RC. Heavy capacitive or dc loading of the Clock Return pin should be avoided, a CMOS or low power TTL Buffer should be used to drive loads greater than 50 pF.

6. For continuous conversion operation, the $\overline{CS}$ input (Pin 1) is grounded and the $\overline{WR}$ input (Pin 3) is connected to the $\overline{INTR}$ output (Pin 5). $\overline{WR}$ and $\overline{INTR}$ should be momentarily forced low following a power-up cycle to guarantee operation.

7. The ADC-830 will require a bus driver when the total capacitance of the data bus gets large. For systems with a slow CPU clock frequency, higher capacitive loads may be driven. Low power Schottky or high current bipolar bus drivers with PNP inputs are recommended.

8. The use of good circuit board layout techniques is required for rated performance. Sockets on a PC board should be used, all logic signal leads should be grouped and kept as far as possible from the analog inputs, and the analog inputs should be shielded. A single point analog ground should be used that is separate from the digital ground. $V_S$ should be bypassed, as close to the $V_S$ pin as possible, with a low inductance 1 μF tantalum capacitor. The $V_S$ bypass capacitor and self-clocking capacitor (if used) should be returned to digital ground.
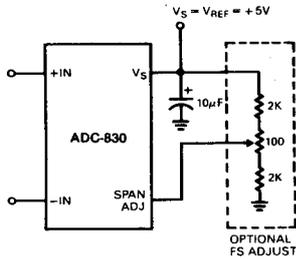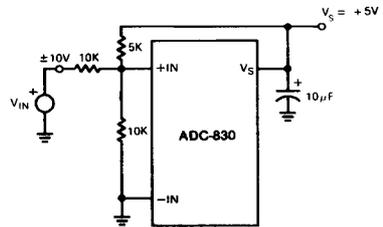
**1**

## TYPICAL PERFORMANCE CHARACTERISTICS



FULL-SCALE ERROR VS $f_{CLK}$



CLK IN SCHMITT TRIP LEVELS VS SUPPLY VOLTAGE

1. $V_T$ = The positive or negative clock IN threshold voltage



$f_{CLK}$ VS CLOCK CAPACITOR



LOGIC INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID VS LOAD CAPACITANCE



EFFECT OF UNADJUSTED OFFSET ERROR VS SPAN ADJ. VOLTAGE



POWER SUPPLY CURRENT VS TEMPERATURE



OUTPUT CURRENT VS TEMPERATURE
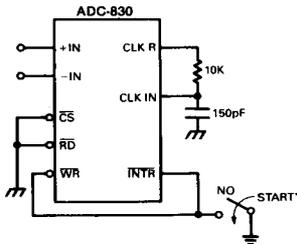
## TYPICAL APPLICATIONS

### ABSOLUTE WITH A +5V REFERENCE
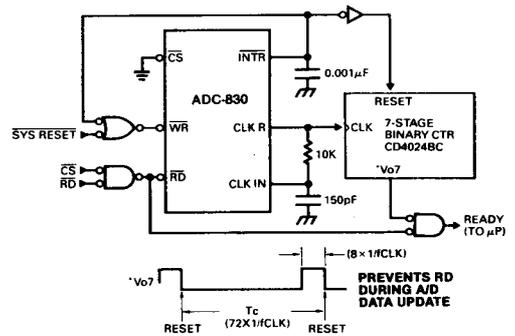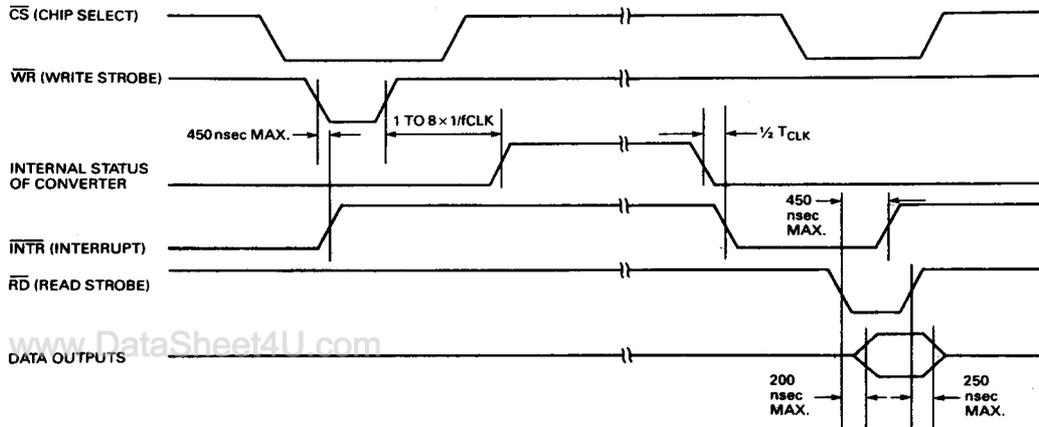
### HANDLING ± 10V ANALOG INPUTS

### SELF—CLOCKING IN FREE-RUNNING MODE

AFTER POWER-UP, A MOMENTARY GROUNDING
OF THE WR INPUT IS NEEDED
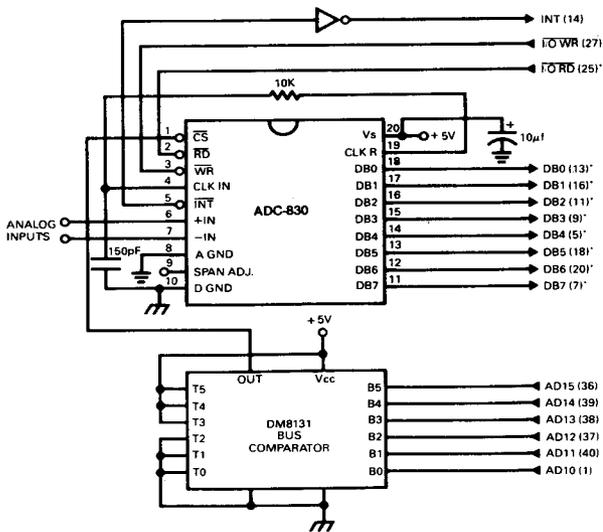TO GUARANTEE OPERATION.

### µP INTERFACE FOR FREE-RUNNING A/D

PREVENTS RD
DURING A/D
DATA UPDATE

## TIMING AND PERFORMANCE

### TIMING DIAGRAM

CS (CHIP SELECT)

WR (WRITE STROBE)

450 nsec MAX.    1 TO 8 × 1/fCLK    ½ TCLK

INTERNAL STATUS
OF CONVERTER

450
nsec
MAX.

INTR (INTERRUPT)

RD (READ STROBE)

DATA OUTPUTS

200
nsec
MAX.

250
nsec
MAX.

## MICROPROCESSOR INTERFACING

### INS 8080A CPU INTERFACE



NOTE 1: *PIN NUMBERS FOR THE INS8228 SYSTEM CONTROLLER, OTHERS ARE INS8080A.

NOTE 2: PIN 23 OF THE INS8228 MUST BE TIED TO +12V THROUGH A 1KΩ RESISTOR TO GENERATE THE RST7 INSTRUCTION WHEN AN INTERRUPT IS ACKNOWLEDGED AS REQUIRED BY THE ACCOMPANYING SAMPLE PROGRAM.

The ADC-830 is designed to interface directly with derivatives of the 8080 µP. The converter can be mapped into memory space using standard memory address decoding, or it can be controlled as an I/O device by using the I/O R and I/O W strobes and decoding address bits A0 → A7 (or A8 → A15) to obtain the CS input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. In systems where the A/D converter is 1 of 8 or less I/O mapped devices, no address decoding circuitry is required. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs, one for each I/O device.

### MC 6800 CPU INTERFACE
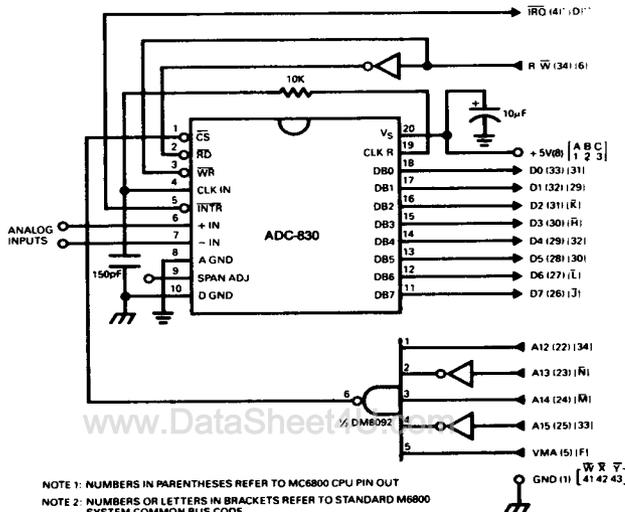


NOTE 1: NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT

NOTE 2: NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE

The control bus for the 6800 µP derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the Ø2 clock. All I/O devices are memory mapped in the 6800 system and a special signal, VMA, indicates that the current address is valid. In many 6800 systems an already decoded 4/5 line is brought out to the common bus at pin 21. This can be tied directly to the ADC-830's CS pin if no other devices are addressed at Hex ADDR: 4XXX or 5XXX.
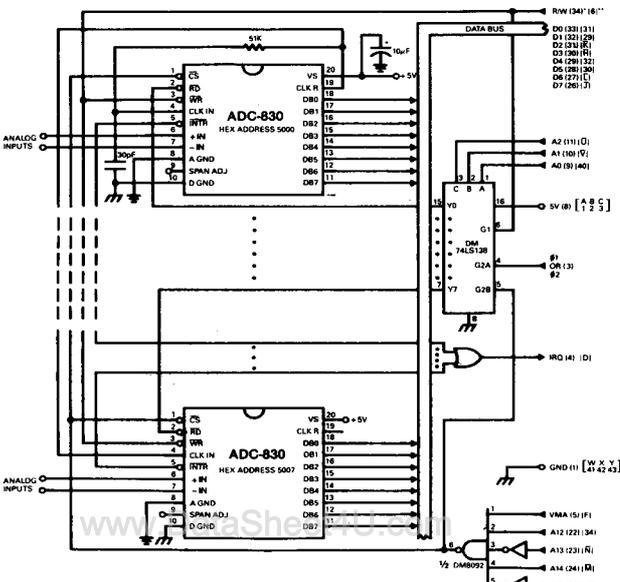
## MICROPROCESSOR INTERFACING

### MULTIPLE ADC-830's IN A MC6800 SYSTEM
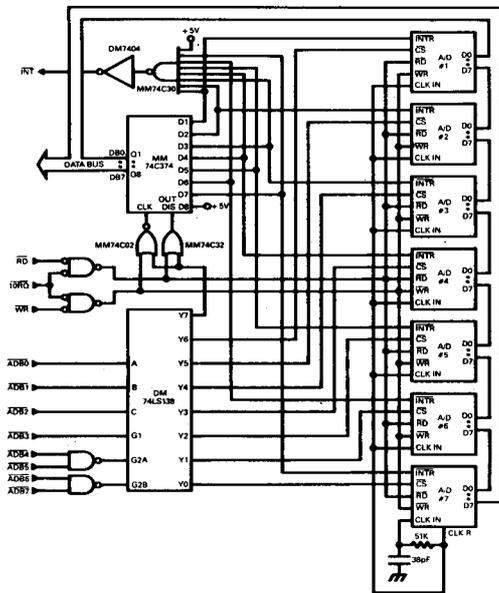


When transferring analog data from several channels to a single μP system, a multiple converter scheme presents several advantages over the conventional multiplexer single converter approach. With the ADC-830, the differential inputs allow individual span adjust for each channel. Also, the channels are sensed simultaneously, reducing the microprocessor's total system servicing time.

In the system shown, the ADC-830's have been arbitrarily located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. The system can easily be extended to allow the interfacing of more converters.

### MULTIPLE ADC-830'S IN A Z-80 INTERRUPT DRIVE MODE



In data acquisition systems where more than one peripheral device will be interrupting program execution of a microprocessor, the CPU must determine which device requires servicing. The circuit shown allows the ADC-830's to be started in any sequence, but will input and store valid data with a priority sequence of A/D #1 through A/D #7. Only the converters whose INT is asserted will be read.

NOTE 1: NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT
NOTE 2: NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE

| ORDERING INFORMATION | |
|---|---|
| **MODEL** | **OPERATING TEMP. RANGE** |
| ADC-830C | 0°C to +70°C |
| **ACCESSORIES** | |
| **Part Number** | **Description** |
| TP100, TP10K | Trimming Potentiometers |