54F/74F157A

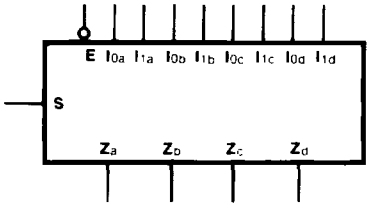
Quad 2-Input Multiplexer

Description

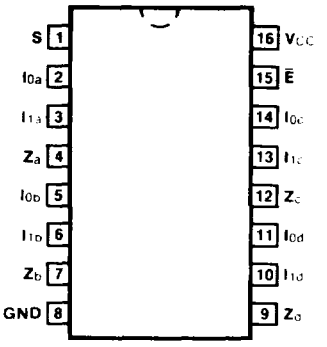
The 'F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157A can also be used to generate any four of the 16 different functions to two variables.

Ordering Code: See Section 5

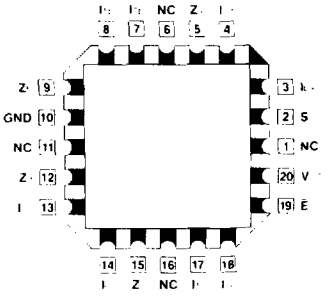
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{0d}	Source 0 Data Inputs	0.5/0.375
I_{1a}-I_{1d}	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
Z_a-Z_d	Outputs	25/12.5

Functional Description

The 'F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input $\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

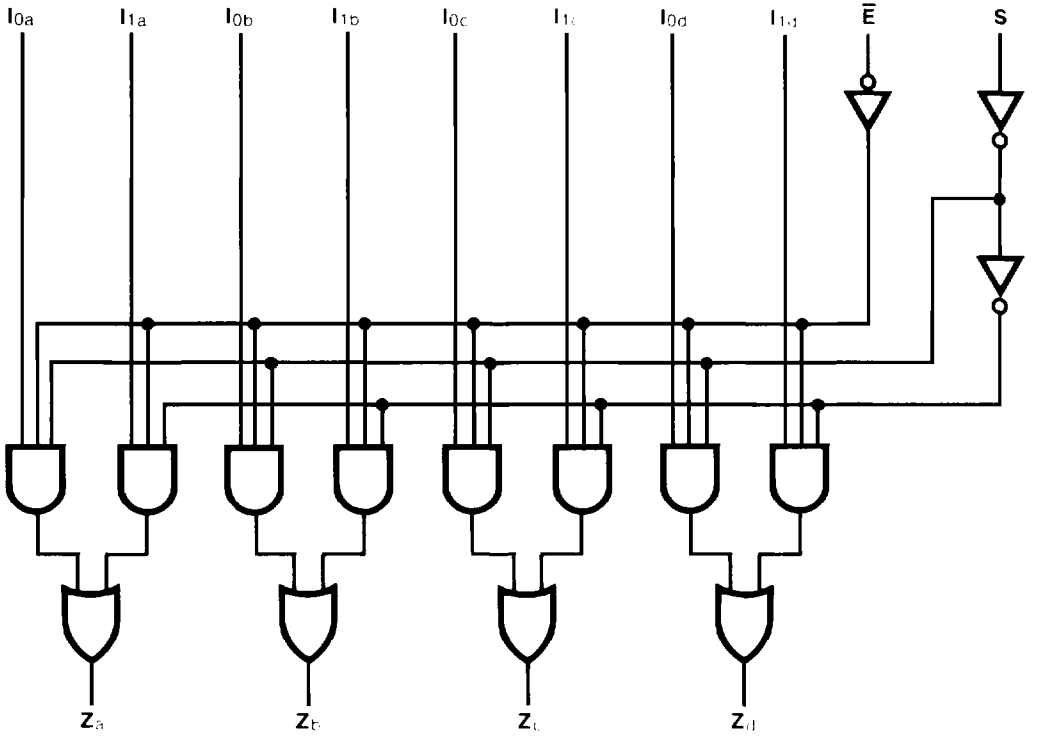
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

A common use of the 'F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

Truth Table

Inputs				Output
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = Max, All Inputs = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	4.0 3.0	7.0 5.0	10.0 7.0	4.0 3.0	12.0 9.0	4.0 3.0	11.0 8.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0 2.5	7.0 4.5	9.5 6.5	5.0 2.5	13.0 7.5	5.0 2.5	11.0 7.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2.5 2.5	4.5 4.0	6.0 5.5	2.5 1.5	7.5 7.5	2.5 2.0	6.5 7.0	ns	3-1 3-4