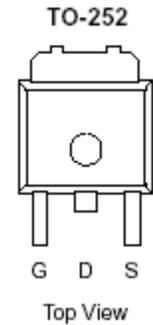
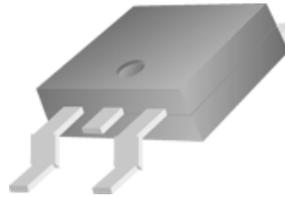


P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (± 25) for battery pack applications



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-26.5	59 @ $V_{GS} = -4.5V$	24
	95 @ $V_{GS} = -2.5V$	19

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-26.5	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ^a	$T_A=25^\circ C$ I_D	24	A
Pulsed Drain Current ^b	I_{DM}	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	-30	A
Power Dissipation ^a	$T_A=25^\circ C$ P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -21 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
		$V_{DS} = -21 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-41			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -24 \text{ A}$			59	m Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -19 \text{ A}$			95	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -24 \text{ A}$		31		S
Diode Forward Voltage	V_{SD}	$I_S = -41 \text{ A}, V_{GS} = 0 \text{ V}$		-0.7		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -24 \text{ A}$		25.0		nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			3.9		
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega, I_D = -24$ $\text{A}, V_{GEN} = -10 \text{ V}, R_G = 6\Omega$		10		nS
Rise Time	t_r			2.8		
Turn-Off Delay Time	$t_{d(off)}$			53.6		
Fall-Time	t_f			46		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics

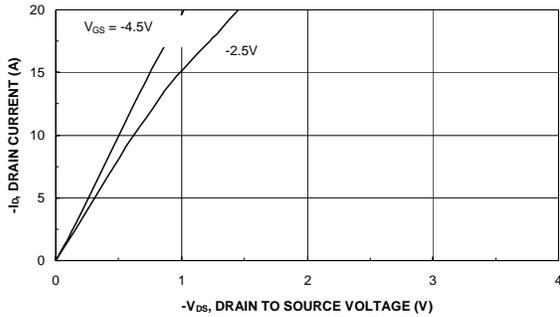


Figure 1. Output Characteristics

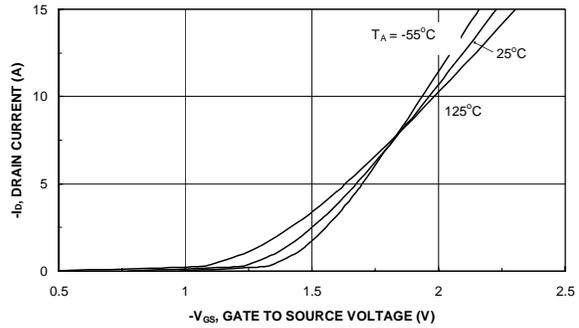


Figure 2. Transfer Characteristics

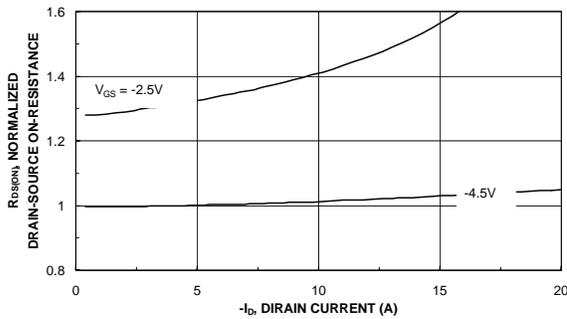


Figure 3. On-Resistance vs. Drain Current

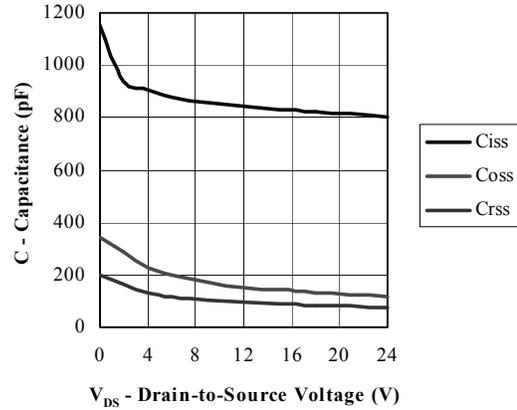


Figure 4. Capacitance

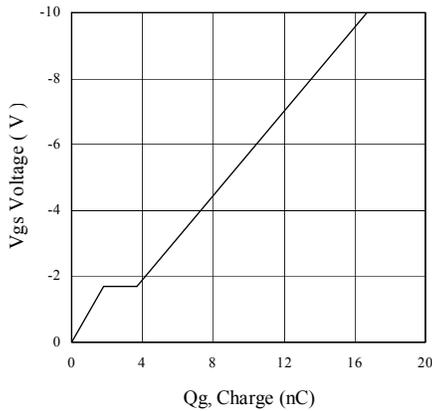


Figure 5. Gate Charge

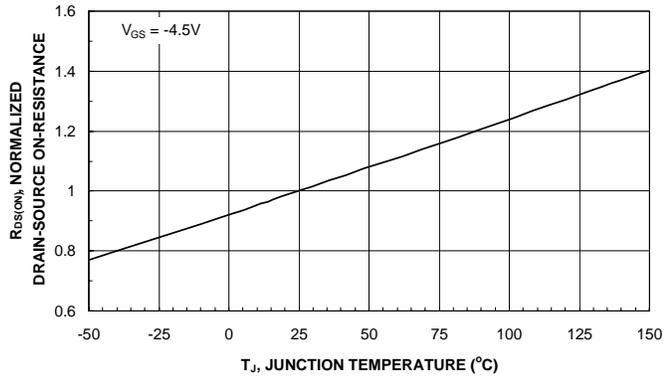


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics

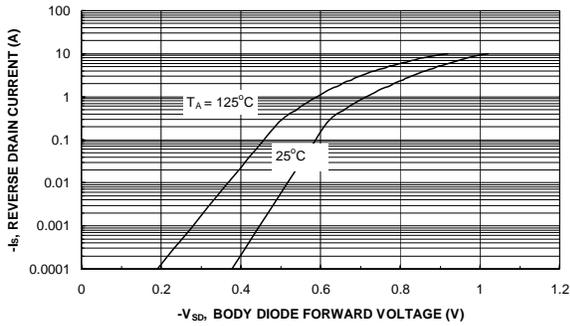


Figure 7. Source-Drain Diode Forward Voltage

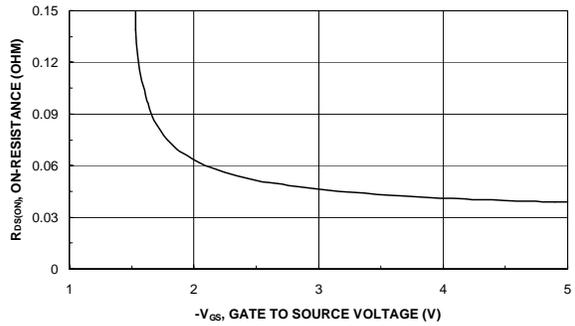


Figure 8. On-Resistance with Gate to Source Voltage

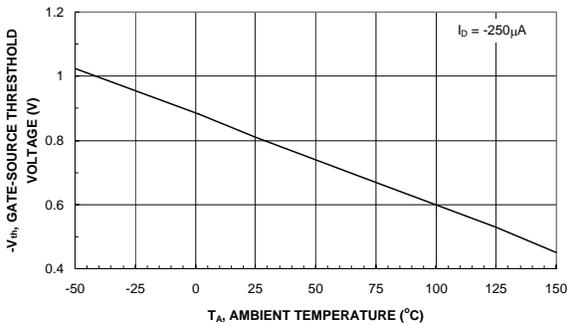


Figure 9. Vth Gate to Source Voltage Vs Temperature

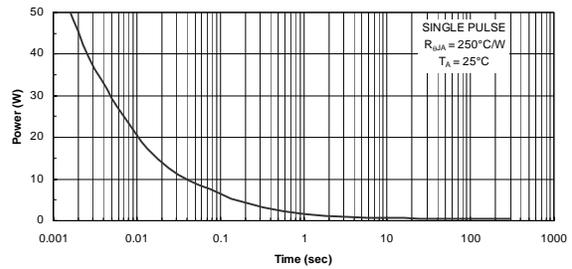


Figure 10. Single Pulse Maximum Power Dissipation

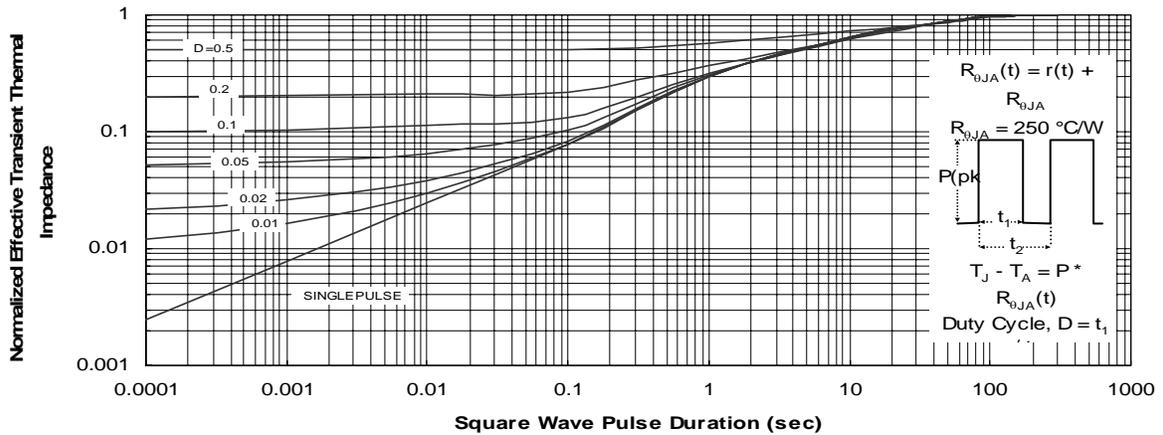
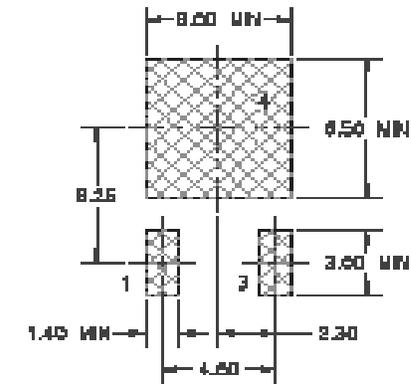
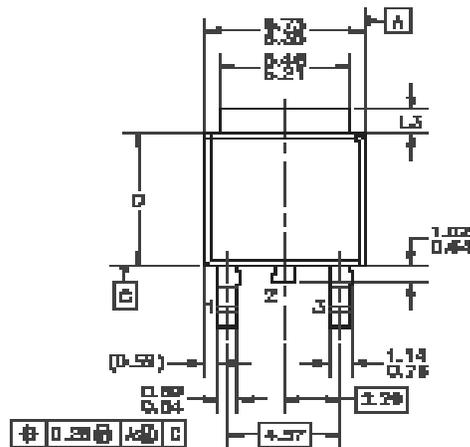
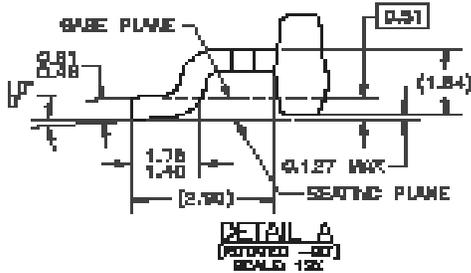
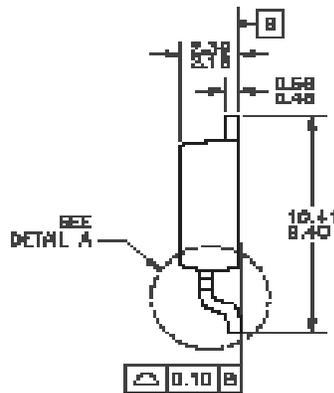
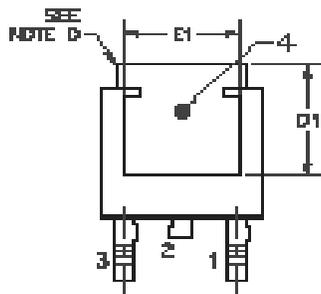


Figure 11. Transient Thermal Response Curve

Package Information



LAND PATTERN RECOMMENDATION



DETAIL A
(NOTED - 90)
SCALE 1:2X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A0	OPTION A1
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.92-0.92
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.57 MIN