REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added device types 03 and 04 and CAGE 65342 as a source for those devices. Added package "Y". Updated Table I, Table IIB, truth table and output load circuits for new device types. - glg	97-11-20	Raymond Monnin

REV																			
SHEET																			
REV	A	A	A																
SHEET	15	16	17																

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary L. Gross

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DRAWING APPROVAL DATE
96-09-06

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, RADIATION-HARDENED, 32K x 8-BIT PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-96891**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

5962-E258-97

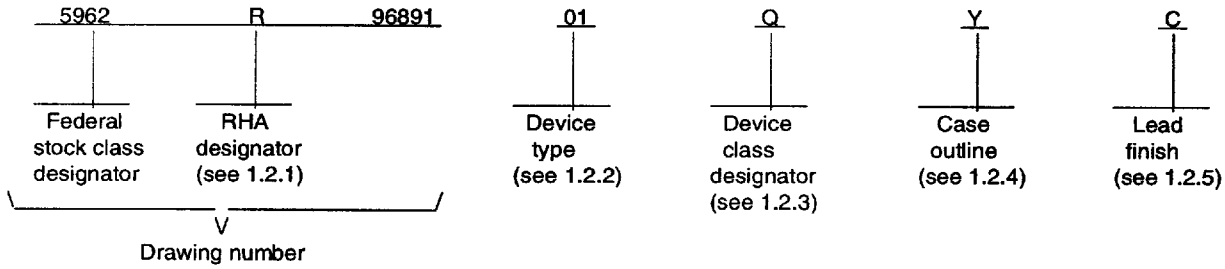
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0032512 317

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 2/	Circuit function	Access time
01 1/	2568C	32K X 8-bit radiation hardened PROM (CMOS inputs)	45 ns
02 1/	2568T	32K X 8-bit radiation hardened PROM (TTL inputs)	45 ns
03	28F256	32K X 8-bit radiation hardened PROM (TTL inputs)	45 ns
04	28F256	32K X 8-bit radiation hardened PROM (TTL inputs)	40 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F28	28	Flat pack
Y	CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device is available in an unprogrammed state only.
2/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein).

1.3 Absolute maximum ratings. 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
Voltage on any pin with respect to ground	-0.5 V dc to V_{DD} +0.5 V dc
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds maximum)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0.0 V dc
Input high voltage (V_{IH}), Device 01	+3.5 V dc minimum to V_{DD}
Device 02	+2.2 V dc minimum to V_{DD}
Device 03 and 04	+2.4 V dc minimum to V_{DD}
Input Low voltage (V_{IL}), Device 01	0.0 V dc to +1.5 V dc maximum
Device 02, 03, and 04	0.0 V dc to +0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C
Radiation features:	
Total dose irradiation, Device 01 and 02	≥ 200 KRads(Si)
Device 03 and 04	≥ 1.0 MRads(Si)
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets, Device 01 and 02	≥ 120 MEV-cm^2/mg
Device 03 and 04	≥ 128 MEV-cm^2/mg
Neutron irradiation	1 x 10^{14} neutrons/cm^2 4/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Guaranteed, but not tested.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.2.4 AC test circuit. The ac test circuit shall be as specified on figure 3.

3.2.5 Read cycle waveforms. The read cycle waveforms shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage	V_{OL1}	V_{DD} = 4.5 V, I_{OL} = 4.0 mA	1, 2, 3	All		0.4	V
		M,D,L,R,F,G,H	1 1/			2/	
Output low voltage	V_{OL2}	V_{DD} = 4.5 V, I_{OL} = 200µA	1, 2, 3	All		0.1	V
		M,D,L,R,F,G,H	1 1/			2/	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -200µA	1, 2, 3	All	V_{DD} - 0.1		V
	V_{OH2}	I_{OH} = -2.0mA		01,02	4.2		
				03,04	2.4		
		M,D,L,R,F,G,H	1 1/		2/		
Input low voltage CMOS inputs	V_{IL1}		1, 2, 3	01		1.5	V
		M,D,L,R,F,G,H	1 1/			2/	
Input low voltage TTL inputs	V_{IL2}		1, 2, 3	02,03,04		0.8	V
		M,D,L,R,F,G,H	1 1/			2/	
High-level input voltage CMOS inputs	V_{IH1}		1, 2, 3	01	3.5		V
		M,D,L,R,F,G,H	1 1/		2/		
High-level input voltage TTL inputs	V_{IH2}		1, 2, 3	02	2.2		V
				03, 04	2.4		
		M,D,L,R,F,G,H	1 1/		2/		
Input leakage current	I_{ILK}	0 V ≤ V_{IN} ≤ 5.5 V	1, 2, 3	All	-5	5	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Three-state output leakage current	I_{OLK}	0 V ≤ V_{OUT} ≤ 5.5 V	1, 2, 3	All	-10	10	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Input capacitance	C_{IN}	f = 1 Mhz @ 0V, V_{DD} = 4.5V 2/ 3/	4	01,02		7	pF
		See 4.4.1c		03,04		15	pF
I/O capacitance	$C_{I/O}$			01,02		10	pF
				03,04		15	pF
Functional tests		See 4.4.1d	7,8A,8B	All			
		M,D,L,R,F,G,H	1 1/				

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Operating supply current	I_{DD1}	$f = 1/t_{AVAV}$ (min) No output load	CMOS input	1, 2, 3	01,02		200	mA
			TTL input		03,04		125	
			M,D,L,R,F,G,H	1 1/			2/	
Standby supply current	I_{DD2}	$\overline{CE} = V_{PP} = V_{IH} = V_{DD}$, CMOS input		1, 2, 3	01,02		2.0	mA
		$\overline{CE} = V_{DD} - 0.5$, $V_{DD} = 5.5$ V CMOS input			03,04		2.0	
			M,D,L,R,F,G,H	1 1/			2/	
Read cycle time	t_{AVAV}	See figure 3 and 4 4/		9, 10, 11	01,02,03	45		ns
					04	40		
			M,D,L,R,F,G,H	9 1/		2/		
Address access time	t_{AVQV}			9, 10, 11	01,02,03		45	ns
					04		40	
			M,D,L,R,F,G,H	9 1/			2/	
$\overline{CE}$ access time	t_{ELQV}			9, 10, 11	01,02,03		45	ns
					04		40	
			M,D,L,R,F,G,H	9 1/			2/	
$\overline{OE}$ access time	t_{GLQV}			9, 10, 11	01,02		45	ns
					03,04		15	
			M,D,L,R,F,G,H	9 1/			2/	
$\overline{CE}$ to output active	t_{ELQX}			9, 10, 11	All	0		ns
			M,D,L,R,F,G,H	9 1/		2/		
$\overline{OE}$ to output active	t_{GLQX}			9, 10, 11	All	0		ns
			M,D,L,R,F,G,H	9 1/		2/		
Output hold time	t_{AXQX}			9, 10, 11	All	0		ns
			M,D,L,R,F,G,H	9 1/		2/		
$\overline{CE}$ to output disable	t_{EHQZ}			9, 10, 11	All		15	ns
			M,D,L,R,F,G,H	9 1/			2/	
$\overline{OE}$ controlled output tri-state time	t_{GHQZ}			9, 10, 11	All		15	ns
			M,D,L,R,F,G,H	9 1/			2/	ns

1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C$. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
3/ Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
4/ Test conditions assume input pulse levels of 0 V to V_{DD}, input rise and fall times of $\le$ 2.0 ns/volt, input and output timing reference levels (except for tri-state parameters) of 2.5 V, and input and output timing reference levels for tri-state parameters of $V_{OL} = 0.5$ V and $V_{OH} = V_{DD}-0.5$ V.

Device types	ALL
Case outlines	X,Y
Terminal number	Terminal symbol
1	A14
2	A12
3	A7
4	A6
5	A5
6	A4
7	A3
8	A2
9	A1
10	A0
11	DQ0
12	DQ1
13	DQ2
14	GND
15	DQ3
16	DQ4
17	DQ5
18	DQ6
19	DQ7
20	$\overline{CE}$
21	A10
22	$\overline{OE}$
23	A11
24	A9
25	A8
26	A13
27	V_{PP} 1/
28	V_{DD}

1/ For device types 03 and 04, V_{PP} is replaced by $\overline{PE}$.

FIGURE 1. Terminal connections.

Read modes for device types 01 and 02

Mode	$\overline{CE}$ 1/	$\overline{OE}$ 1/	V_{PP} 1/	I/O	Power 2/
Read	Low	Low	V_{DD}	Data-out	Active
Tristate	Low	High	V_{DD}	High-Z	Active
Standby	V_{DD}	X 3/	V_{DD}	High-Z	Standby1
Standby	High	X 3/	V_{DD}	High-Z	Standby2
Program	Low	High	17V ± 0.5V	Data-in	Programming

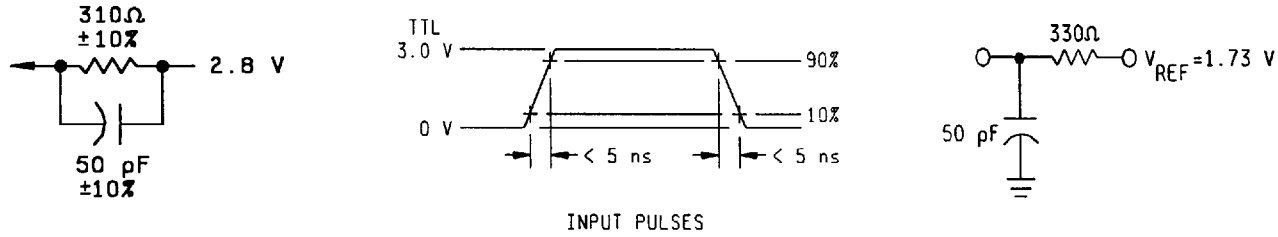
1/ High: $V_{IN} \geq 2.2$ V for TTL inputs; $V_{IN} \geq 3.5$ V for CMOS inputs.
Low: $V_{IN} \leq 0.8$ V for TTL inputs; $V_{IN} \leq 1.5$ V for CMOS inputs.
2/ Minimum I_{DD} is drawn when Standby mode is implemented with $\overline{CE} = V_{DD}$ (standby1 power).
3/ V_{IN} for don't care (X) inputs = V_{IL} or V_{IH}.

Read modes for device types 03 and 04

Mode	$\overline{CE}$ 1/	$\overline{OE}$ 1/	$\overline{PE}$ 1/	I/O
Standby	High	X 2/	High	High-Z
Read	Low	Low	High	Data-out
Program	Low	High	Low	Data-in
Read 3/	Low	High	High	High-Z

1/ High: $V_{IN} \geq 2.2$ V for TTL inputs.
Low: $V_{IN} \leq 0.8$ V for TTL inputs.
2/ V_{IN} for don't care (X) inputs = V_{IL} or V_{IH}.
3/ Device active; outputs disabled.

FIGURE 2. Truth tables.



Device 01 and 02 NOTE: Measurement of data output occurs at midpoint Device 03 and 04

FIGURE 3. Output load circuits or equivalent and switching waveform.

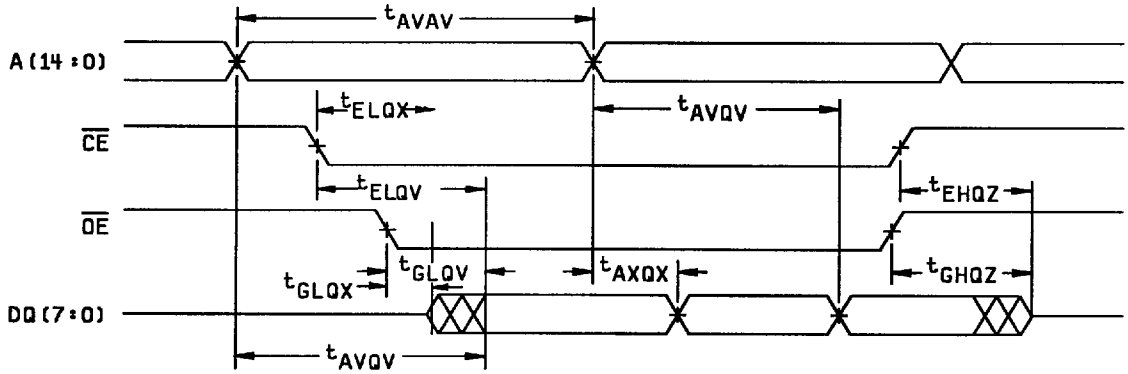


FIGURE 4. Read cycle waveform.

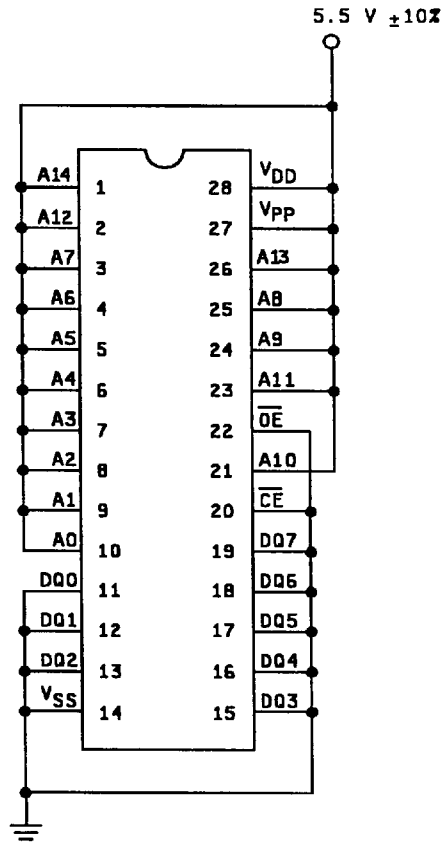


FIGURE 5. Irradiation circuit.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table I. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (prebum-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

f. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.4.4.3 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEP).
d. Number of transients (SEP).
e. Occurence of latchup (SEP).

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

Table IIA. Elecrtical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table IA)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	1,7,9	1,7,9	1,7,9
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the zero hour electrical parameters (see table IIA).
7/ See 4.4.1f.

Table IIB. Delta limits at +25°C.

Test 1/	Device types	Delta limits
I_{DD1}	01, 02	±10% of specified value in table I
I_{DD2} 2/	03, 04	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ If devices are tested at or below 10µA, no deltas are required.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

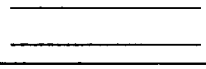
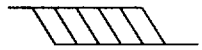
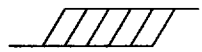
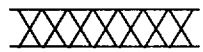
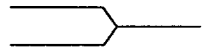
6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Symbols, definitions, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{DD} ..... Supply current.
I_I ..... Input current.
I_O ..... Output current.
T_C ..... Case temperature.
V_{DD} ..... Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-11-20

Approved sources of supply for SMD 5962-96891 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9689101QXC	52088	LMP2568C-Q45X
5962R9689101VXC	52088	LMP2568C-V45X
5962R9689102QXC	52088	LMP2568T-Q45X
5962R9689102VXC	52088	LMP2568T-V45X
5962H9689103QXA	65342	UT28F256T-45UCAH
5962H9689103VXA	65342	UT28F256T-45UCAH
5962H9689103QXC	65342	UT28F256T-45UCCH
5962H9689103VXC	65342	UT28F256T-45UCCH
5962H9689103QYA	65342	UT28F256T-45PCAH
5962H9689103VYA	65342	UT28F256T-45PCAH
5962H9689103QYC	65342	UT28F256T-45PCCH
5962H9689103VYC	65342	UT28F256T-45PCCH
5962H9689104QXA	65342	UT28F256T-40UCAH
5962H9689104VXA	65342	UT28F256T-40UCAH
5962H9689104QXC	65342	UT28F256T-40UCCH
5962H9689104VXC	65342	UT28F256T-40UCCH
5962H9689104QYA	65342	UT28F256T-40PCAH
5962H9689104VYA	65342	UT28F256T-40PCAH
5962H9689104QYC	65342	UT28F256T-40PCCH
5962H9689104VYC	65342	UT28F256T-40PCCH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
52088	Lockheed Martin Federal Systems, Incorporated 9500 Godwin Drive Manassas, VA 22110-4104
65342	UTMC Microelectronics Systems Incorporated 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.