Integrated Device Technology, Inc.

FAST CMOS PARITY BUS TRANSCEIVER

IDT 54/74FCT833A/B
IDT 54/74FCT834A/B*
IDT 54/74FCT853A/B
IDT 54/74FCT854A/B*

FEATURES:

- Equivalent to AMD's Am29833-34 and Am29853-54 bipolar parity bus transceivers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High speed bidirectional bus transceiver for processor-organized devices
  - Non-inverting propagation delay = 7.0ns max.
  - Inverting propagation delay = 7.0ns max.
- Buffered direction three state control
- Error Flag with open-drain output
- I_{OL} = 48mA (commercial) and 32mA (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Available in Plastic DIP, CERDIP, LCC, PLCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

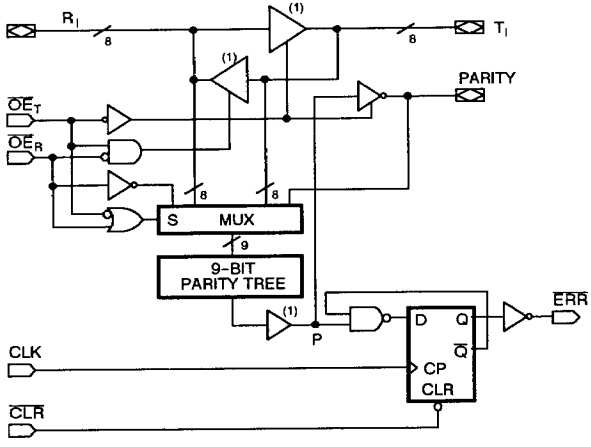
DESCRIPTION:

The IDT54/74FCT833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available: the IDT54/74FCT833/34 register option and the IDT54/74FCT853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

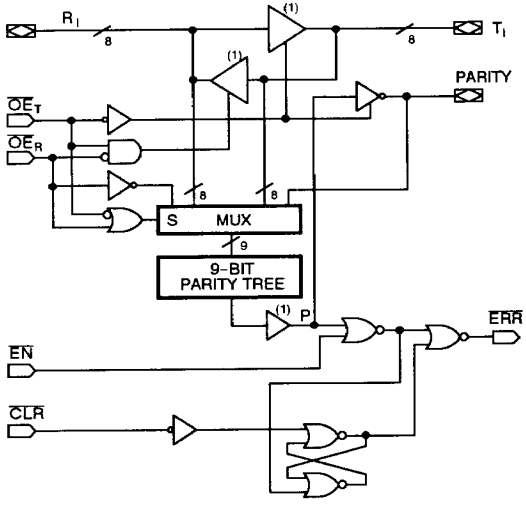
The output enables $\overline{OE_T}$ and $\overline{OE_R}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{OE_R}$ and $\overline{OE_T}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The IDT54/74FCT833 and IDT54/74FCT853 are non-inverting, while the IDT54/74FCT834 and IDT54/74FCT854 present inverting data at the outputs. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT833
(Device Shown Non-inverting)



IDT54/74FCT853
(Device Shown Non-inverting)



NOTE:

1. Non-inverting buffer for IDT54/74FCT833/53, inverting buffer for IDT54/74FCT834/54, note that the inverting device converts the positive logic "R" bus levels to negative levels on "T" bus.

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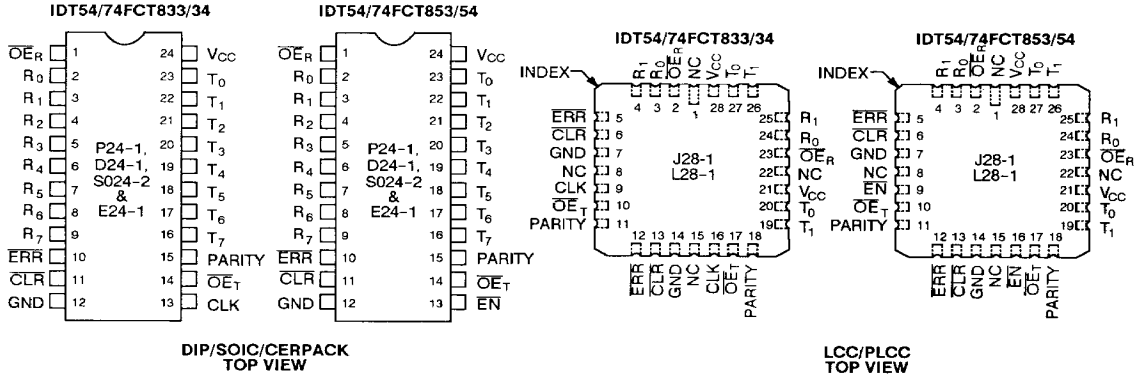
*Advance information only for IDT54/74FCT834 and IDT54/74FCT854.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
IDT54/74FCT833/34			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
IDT54/74FCT853/54			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault latch output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Enable latch input for fault flag.

ERROR FLAG OUTPUT TRUTH TABLE

IDT54/74FCT833/IDT54/74FCT834 (REGISTER OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
CLR	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	Sample (1's Capture)
H	↑	–	L	L	
H	↑	L	–	L	
L	–	–	–	H	Clear

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

IDT54/74FCT853/IDT54/74FCT854 (LATCH OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
$\overline{EN}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample (1's Capture)
L	H	–	L	L	
L	H	H	H	H	
H	L	–	–	H	Clear
H	H	–	L	L	Store
H	H	–	H	H	

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

FUNCTION TABLES

IDT54/74FCT833 NON-INVERTING REGISTER OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_I (Σ OF H'S)	T_I INCL PARITY (Σ OF H'S)	R_I	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	H	
H	H	H	↑	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT834 INVERTING REGISTER OPTION(2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_I (Σ OF L'S)	T_I INCL PARITY (Σ OF H'S)	R_I	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	L	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	L	NA	NA	H	
H	L	H	↑	NA	L (Odd)	H	NA	NA	L	
H	L	H	↑	NA	L (Even)	H	NA	NA	H	
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	L	
H	H	H	↑	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
*Store the Error State of the Last Receive Cycle

Z = High Impedance
NA = Not Applicable
– = Don't Care or Irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:

1. Output state assumes HIGH output pre-state.
2. Note that for the negative levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

FUNCTION TABLES (CONTINUED)

IDT54/74FCT853 NON-INVERTING LATCH OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_I (Σ OF H'S)	T_I INCL PARITY (Σ OF H'S)	R_I	T_I	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT854 INVERTING LATCH OPTION (2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_I (Σ OF H'S)	T_I INCL PARITY (Σ OF H'S)	R_I	T_I	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance
NC = No Change
NA = Not Applicable
*Store the Error State of the Last Receive Cycle
– = Don't Care or Irrelevant
Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:

1. Output state assumes HIGH output pre-state.
2. Note that for negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Ouput and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min.	All other outputs V_{IN} = V_{IH} or V_{IL}; I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
			$\overline{ERR}$; I_{OL} = 48mA	–	0.3	0.5	
V_H	Input Hysteresis on T_I and R_I	–		–	200	–	mV

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_T$ = $\overline{OE}_R$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND $\overline{OE}_R$ = V_{CC} f_i = 2.5MHz One Input Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	1.2	3.4	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.6	5.4	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND f_i = 2.5MHz $\overline{OE}_R$ = V_{CC} Eight Inputs Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	3.8	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER TEMPERATURE RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[4]	IDT54/74FCT8XXA[3]				IDT54/74FCT8XXB[3]				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH}	Propagation Delay R_i to $\overline{T}_i$, T_i to R_i		C_L = 50pF	–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PHL}				–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PLH}			C_L = 300pF[6]	–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PHL}				–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PLH}	Propagation Delay R_i to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF[6]	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PZH}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZL}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZH}			C_L = 300pF[6]	–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PZL}				–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PHZ}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i		C_L = 5pF[6]	–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PLZ}				–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PHZ}			C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLZ}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{SU}	T_i, PARITY to CLK Set-up Time [1]		C_L = 50pF	12.0	–	16.0	–	8.5	–	11.0	–	ns
t_H	T_i, PARITY to CLK Hold Time [1]			0	–	0	–	0	–	0	–	ns
t_{SU}	Clear Recovery Time $\overline{CLR}$ to CLK [2]			15.0	–	20.0	–	10.5	–	14.0	–	ns
t_W	Clock Pulse Width [1]	HIGH		7.0	–	9.5	–	5.5	–	7.0	–	ns
		LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_W	Clear Pulse Width	LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ [1]		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		C_L = 50pF	–	16.0	–	20.0	–	15.0	–	18.0	ns
t_{PLH}	Propagation-Delay T_i, PARITY TO $\overline{ERR}$ (PASS Mode Only) IDT54/74FCT853 and IDT54/74FCT854		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}	Propagation Delay $\overline{OE}_R$ to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF[6]	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns

NOTES:
1. For IDT54/74FCT853/54, replace CLK with $\overline{EN}$.
2. Not applicable to IDT54/74FCT853/54.
3. XX represents 33, 34, 53 and 54.
4. See test circuit and waveforms.
5. Minimum limits are guaranteed but not tested on Propagation Delays.
6. These parameters are guaranteed but not tested.

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ORDERING INFORMATION