

DCR750F85

Phase Control Thyristor

Preliminary Information



DS5934-1.0 August 2008 (LN26349)

FEATURES

- **Double Side Cooling**
- High Surge Capability

APPLICATIONS

KEY PARAMETERS

V _{DRM} I _{T(AV)} I _{TSM} dV/dt*	8500V 733A 9800A 1500V/µs 200A/µs
dl/dt	200A/µs

* Higher dV/dt selections available

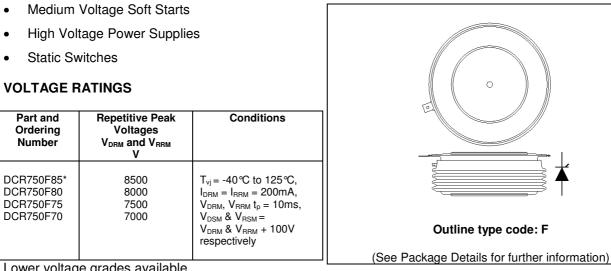


Fig. 1 Package outline

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR750F85* DCR750F80 DCR750F75 DCR750F70	8500 8000 7500 7000	$\begin{array}{l} T_{vj} = -40 \ ^{\circ} C \ to \ 125 \ ^{\circ} C, \\ I_{DRM} = I_{RRM} = 200 \ ^{\circ} A, \\ V_{DRM}, V_{RRM} \ t_p = 10 \ ^{\circ} ms, \\ V_{DSM} \& V_{RSM} = \\ V_{DRM} \& V_{RRM} + 100 V \\ respectively \end{array}$

Lower voltage grades available. *8200V @ -40° C, 8500V @ 0° C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR750F85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.



CURRENT RATINGS

 T_{case} = 60 °C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load	733	А
I _{T(RMS)}	RMS value	-	1151	А
Ι _Τ	Continuous (direct) on-state current	-	1139	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125 °C	9.8	kA
l ² t	I ² t for fusing	V _R = 0	0.48	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Condition	Min.	Max.	Units	
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.0184	°C/W
		Single side cooled	Anode DC	-	0.0333	℃/W
			Cathode DC	-	0.0418	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 23 kN	Double side	-	0.004	°C/W
		(with mounting compound)	Single side	-	0.008	℃/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T _{stg}	Storage temperature range			-55	125	°C
Fm	Clamping force			20.0	25.0	kN



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DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditio	Min.	Max.	Units	
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125 °C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125 °C, ga	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{\text{T}(\text{AV})}$	Repetitive 50Hz	-	100	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	200	A/µs
		t _r < 0.5μs, T _j = 125 ℃				
V _{T(TO)}	Threshold voltage – Low level	100A to 500A at T _{case} = 125	°C	-	1.030	V
	Threshold voltage – High level	500A to 2500A at T _{case} = 125	5°C	-	1.30	V
r _T	On-state slope resistance – Low level	100A to 500A at T _{case} = 125	-	2.06	mΩ	
	On-state slope resistance – High level	500A to 2500A at T _{case} = 125	-	1.542	mΩ	
t _{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source	30V, 10Ω	-	3	μs
		tr = 0.5µs, Tj = 25 ℃				
tq	Turn-off time	T _j = 125 ℃, I _{peak} = 1000A, t _p V _R = 100V, dI/dt = 5A/μs,	= 1000us,	-	1200	μs
		$dV_{DR}/dt = 20V/\mu s$ linear to 2500V				
I _{RR}	Reverse Recovery current	I _T = 1000A, tp = 1000us,T _i = 125 ℃,		95	118	А
Qs	Stored charge	$dI/dt = -5A/\mu s$, $V_{Rpeak} = 100V$		3000	4000	μC
ΙL	Latching current	$T_j = 25 ^{\circ}\text{C}, V_D = 5V$		-	3	Α
Ι _Η	Holding current	$T_j = 25 ^{\circ}C, R_{G-K} = \infty, I_{TM} = 50$	0A, I _T = 5A	-	300	mA



GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	$V_{\text{DRM}} = 5V, T_{\text{case}} = 25 ^{\circ}\text{C}$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V _{DRM,} T _{case} = 125 ℃	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25 ℃	250	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM,} T _{case} = 125 ℃	15	mA

CURVES

BYNEX SEMICONDUCTOR

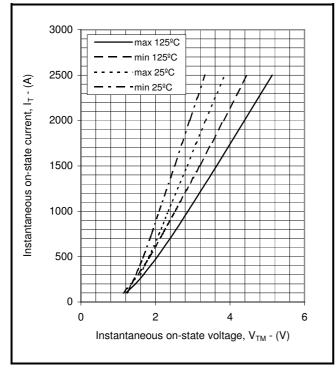


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

Where A = 0.454245B = 0.106933 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$ C = 0.001271D = 0.013218these values are valid for T_j = 125 $^{\circ}\!\!\!\mathrm{C}$ for I_T 100A to 3000A

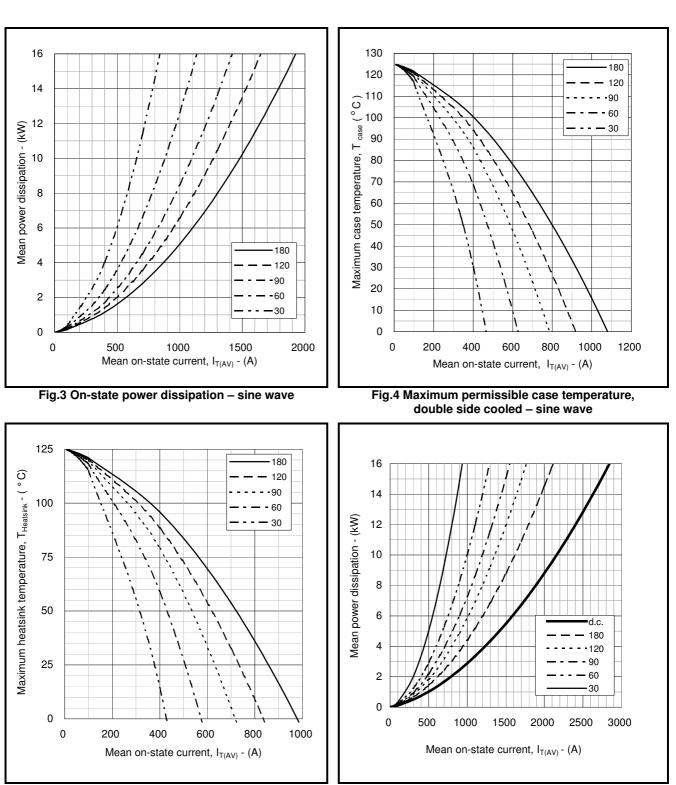


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

Fig.6 On-state power dissipation - rectangular wave

SEMICONDUCTOR

DCR750F85



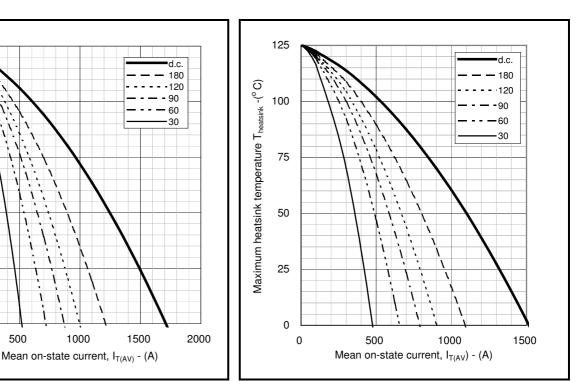
125

Maximum permissible case temperature , T_{case} -(°C) 52 05 54 00

0

0

500





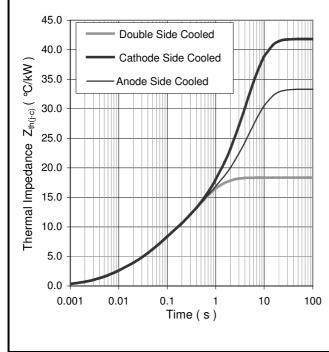


Fig.8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

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		1	2	3	4
Double side cooled	R _i (°C/kW)	7.5608	4.0772	3.8420	2.8671
	T _i (s)	0.6877	0.2537	0.0614	0.0101
Anode side cooled	R _i (°C/kW)	6.7211	4.6219	15.5387	14.8631
	T _i (s)	0.1910	0.0158	5.0011	3.3169
Cathode side cooled	R _i (°C/kW)	11.5564	8.5810	4.7942	8.3643
	T _i (s)	4.2216	6.0269	0.0166	0.2255

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

$\Delta \textbf{R}_{\text{th(j-c)}} \text{ Conduction}$

Tables show the increments of thermal resistance $R_{\text{th}(j\text{-}c)}$ when the device operates at conduction angles other than d.c.

D	ouble side co	A	Anode Side Cooling			Cathode Sided Cooling		
	ΔZ_{th}	(z)		ΔZ	_{th} (z)		$\Delta Z_{th}(z)$	
θ°	sine.	rect.	θ°	sine.	rect.	θ°	sine.	rect.
180	3.19	2.14	180	2.97	2.03	180	2.95	2.02
120	3.72	3.10	120	3.43	2.89	120	3.40	2.87
90	4.29	3.64	90	3.92	3.36	90	3.88	3.34
60	4.81	4.23	60	4.36	3.87	60	4.31	3.84
30	5.22	4.88	30	4.69	4.41	30	4.64	4.37
15	5.40	5.22	15	4.84	4.70	15	4.79	4.65

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)



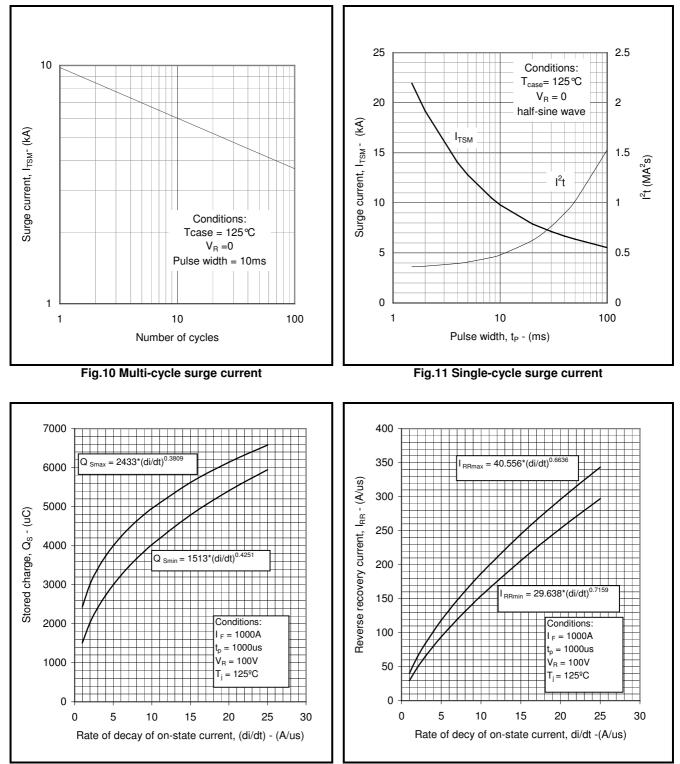


Fig.12 Stored charge

Fig.13 Reverse recovery current

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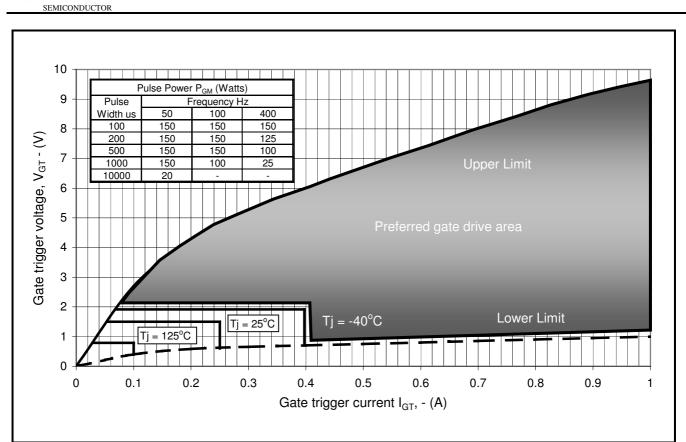


Fig14 Gate Characteristics

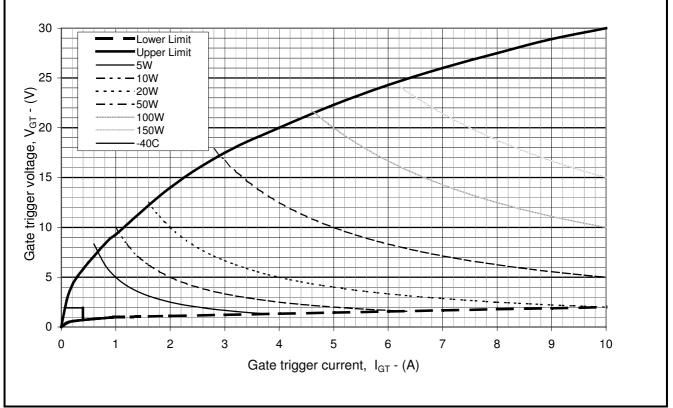


Fig. 15 Gate characteristics

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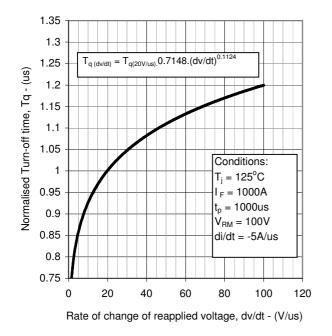


Fig.16 Turn-off time



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PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

3rd ANGLE PROJECTION Image: Constant of the second sec	Device DCR1003SF18 DCR1006SF28 DCR1008SF36 DCR1020F65 DCR1050SF42 DCR1180F52 DCR1274SF18 DCR1275SF28 DCR1277SF36 DCR1279SF48 DCR1350F42 DCR1610F28 DCR1640F28 DCR1830F22	Maximum Thickness (mm) 26.415 26.49 26.72 27.1 26.72 26.84 26.415 26.49 26.72 26.84 26.72 26.84 26.72 26.84 26.72 26.49 26.49 26.49 26.49	Minimum Thickness (mm) 25.865 25.94 26.17 26.55 26.17 26.29 25.865 25.94 26.17 26.29 26.17 26.29 26.17 25.94 25.94 25.94 25.94
Ø73.0 MAX			
	DCR1610F28	26.49	25.94
	DCR810F85 DCR840F48	27.46 26.84	26.91 26.29
Ø47.0 NOM	DCR890F65 DCR950F65	27.1 27.1	26.5 26.5
FOR PACKAGE HEIGHT SEE TABLE			
Lead length: 42 Lead terminal connec			

Fig.17 Package outline



POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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