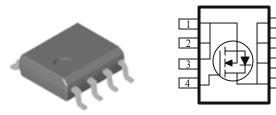
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N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V _{DS} (V)	$r_{\mathrm{DS(on)}} m(\Omega)$	I _D (A)		
30	$22 @ V_{GS} = 10V$	9.4		
	$30 @ V_{GS} = 4.5V$	7.0		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage			±20	v	
Continuous Drain Current ^a	$T_A=25^{\circ}C$	I.	9.4		
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	7.4	А	
Pulsed Drain Current ^b		I _{DM}	±30		
Continuous Source Current (Diode Conduction) ^a			1.6	Α	
	$T_A=25^{\circ}C$	D_	3.1	W	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	тD	2		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 10 sec	D	50	°C/W	
	Steady State	$R_{\theta JA}$	92	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

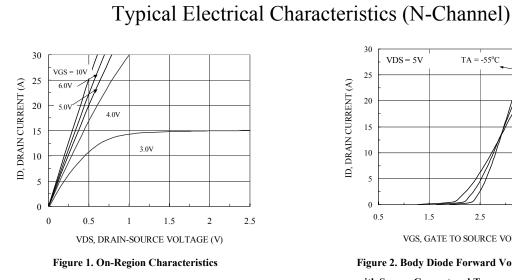
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SPECIFICATIONS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Tost Conditions	Limits			Unit	
r ar ameter	Symbol	Test Conditions		Тур	Max	Umt	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$			1	uA	
	-033	$V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			25		
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	20			Α	
Drain-Source On-Resistance ^A	r.	$V_{GS} = 10 \text{ V}, I_D = 9.2 \text{ A}$			22	mΩ	
Dram-Source On-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$			30	1115.2	
Forward Tranconductance ^A	$g_{\rm fs}$	$V_{DS} = 15 \text{ V}, I_D = 9.2 \text{ A}$		40		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 2.3$ A, $V_{\rm GS} = 0$ V		0.7		V	
Dynamic ^b							
Total Gate Charge	Qg	$N_{\rm e} = 10 N_{\rm e} N_{\rm e} = 4.5 N_{\rm e}$		4.0			
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$		1.1		nC	
Gate-Drain Charge	Q _{gd}	$I_D = 7 A$		1.4			
Input Capacitance	C _{iss}	V = 15 V V = 0 V		720			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$		165		pF	
Reverse Transfer Capacitance	C _{rss}	I = IMHZ		60			
Turn-On Delay Time	t _{d(on)}			16			
Rise Time	t _r	V_{DD} = 10 V, R_L = 6 Ω , I_D = 1 A,		5			
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 V$		23		nS	
Fall-Time	t _f			3			

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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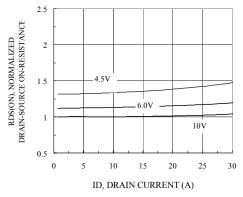


Figure 3. On Resistance Vs Vgs Voltage

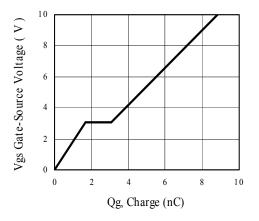


Figure 5. Gate Charge Characteristics

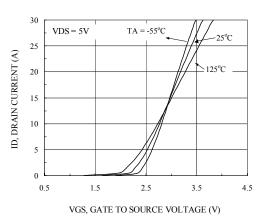
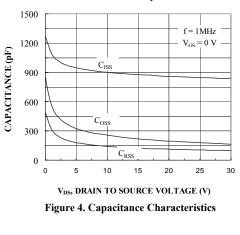


Figure 2. Body Diode Forward Voltage Variation

with Source Current and Temperature



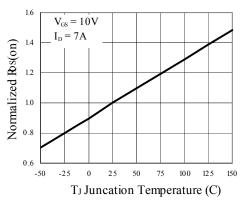
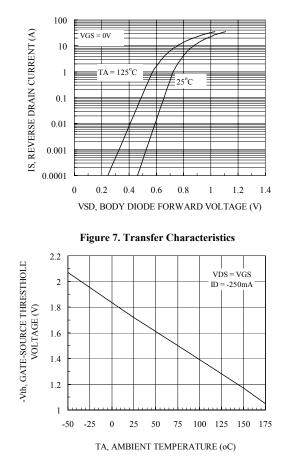


Figure 6. On-Resistance Variation with Temperature



Typical Electrical Characteristics (N-Channel)

Figure 9. Vth Gate to Source Voltage Vs Temperature

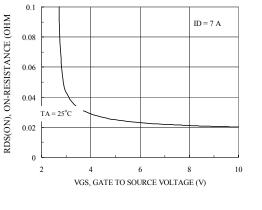


Figure 8. On-Resistance with Gate to Source Voltage

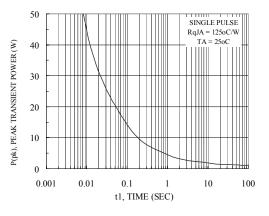
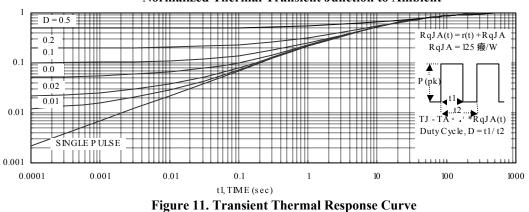


Figure 10. Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Junction to Ambient

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