HT93LC86

CMOS 16K 3-Wire Serial EEPROM

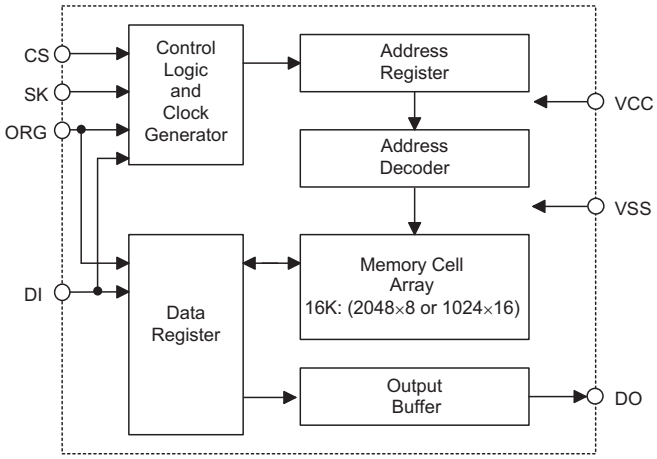
Features

- Operating voltage: 2.2V~5.5V
- Low power consumption
  - Operating: 5mA max.
  - Standby: 10μA max.
- User selectable internal organization
  - 16K: 2048×8 or 1024×16
- 3-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Write operation with built-in timer
- Software controlled write protection
- 40-year data retention
- 10^6 rewrite cycles per word
- Commercial temperature range (0°C to +70°C)
- 8-pin DIP/SOP/TSSOP package

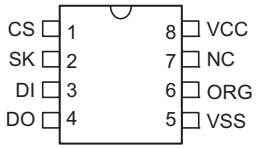
General Description

The HT93LC86 is a 16K-bit low voltage nonvolatile, serial electrically erasable programmable read only memory device using a CMOS floating gate process. Its 16384 bits of memory are organised into 1024 words of 16 bits each when the ORG pin is connected to VCC or organised into 2048 words of 8 bits each when it is tied to VSS. The device is especially suitable for use in many industrial and commercial applications where low power and low voltage operation are essential. The device can easily interface to microcontrollers using the versatile serial interface compose of (CS), serial clock (SK), data input (DI) and data output (DO).

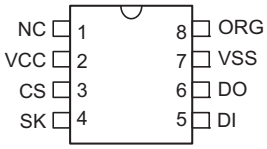
Block Diagram



Pin Assignment



HT93LC86
8 DIP-A/SOP-A/TSSOP-A



HT93LC86
8 SOP-B

Pin Description

Pin Name	I/O	Description
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Serial data input
DO	O	Serial data output
VSS	—	Negative power supply, ground
ORG	I	Internal Organization When ORG is connected to VDD or left floating, the (×16) memory organization is selected. When ORG is connected to VSS, the (×8) memory organization is selected. The ORG pin is connected to an internal pull-high resistor.
NC	—	No connection
VCC	—	Positive power supply

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... 0°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.2	—	5.5	V
I_{CC1}	Operating Current (TTL)	5V	DO no load, SK=1MHz	—	—	5	mA
I_{CC2}	Operating Current (CMOS)	5V	DO no load, SK=1MHz	—	—	5	mA
		2.2V~5.5V	DO no load, SK=250kHz	—	—	5	mA
I_{STB}	Standby Current (CMOS)	5V	CS=SK=DI=0V	—	—	10	μA
I_{LI}	Input Leakage Current	5V	V_{IN}=V_{SS}~V_{CC}	0	—	1	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=V_{SS}~V_{CC}, CS=0V	0	—	1	μA
V_{IL}	Input Low Voltage	5V	—	0	—	0.8	V
		2.2V~5.5V	—	0	—	0.1V_{CC}	V
V_{IH}	Input High Voltage	5V	—	2	—	V_{CC}	V
		2.2V~5.5V	—	0.9V_{CC}	—	V_{CC}	V
V_{OL}	Output Low Voltage	5V	I_{OL}=2.1mA	—	—	0.4	V
		2.2V~5.5V	I_{OL}=10μA	—	—	0.2	V
V_{OH}	Output High Voltage	5V	I_{OH}=–400μA	2.4	—	—	V
		2.2V~5.5V	I_{OH}=–10μA	V_{CC}–0.2	—	—	V
C_{IN}	Input Capacitance	—	V_{IN}=0V, f=250kHz	—	—	5	pF
C_{OUT}	Output Capacitance	—	V_{OUT}=0V, f=250kHz	—	—	5	pF

A.C. Characteristics

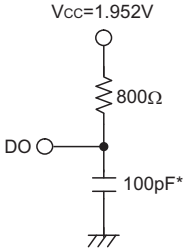
Symbol	Parameter	V_{CC}=5V±10%		V_{CC}=3V±10%		V_{CC}=2.2V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	0	2000	0	500	0	250	kHz
t_{SKH}	SK High Time	250	—	1000	—	2000	—	ns
t_{SKL}	SK Low Time	250	—	1000	—	2000	—	ns
t_{CSS}	CS Setup Time	50	—	200	—	200	—	ns
t_{CSH}	CS Hold Time	0	—	0	—	0	—	ns
t_{CDS}	CS Deselect Time	250	—	250	—	1000	—	ns
t_{DIS}	DI Setup Time	100	—	200	—	400	—	ns
t_{DIH}	DI Hold Time	100	—	200	—	400	—	ns
t_{PD1}	DO Delay to ″1″	—	250	—	1000	—	2000	ns
t_{PD0}	DO Delay to ″0″	—	250	—	1000	—	2000	ns
t_{SV}	Status Valid Time	—	250	—	250	—	250	ns
t_{HZ}	DO Disable Time	—	100	—	200	—	400	ns
t_{PR}	Write Cycle Time	—	5	—	5	—	5	ms

A.C. Test Conditions

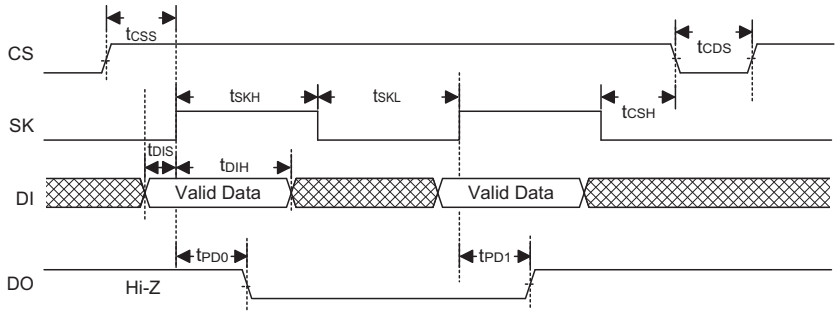
Input rise and fall time: 5ns (1V to 2V)

Input and output timing reference levels: 1.5V

Output load circuit: See Figure right



Note: * Including scope and jig



Functional Description

The HT93LC86 is accessed via a three-wire serial communication interface. The device is arranged into 1024 words by 16 bits or 2048 words by 8 bits depending whether the ORG pin is connected to VCC or VSS. The HT93LC86 contains seven instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. When the user selectable internal organization is arranged into 1024×16 (2048×8), these instructions are all made up of 13(14) bits data: 1 start bit, 2 op code bits and 10(11) address bits.

By using the control signal CS, SK and data input signal DI, these instructions can be transmitted to the HT93LC86. These serial instruction data presented at the DI input will be written into the device on the rising edge of SK. During the READ cycle, the DO pin acts as the data output and during the WRITE or ERASE cycle, the DO pin indicates the BUSY/READY status. When the DO pin is active for reading data or as a BUSY/READY indicator the CS pin must be high; otherwise the DO pin will be in a high-impedance state. For successful instruction execution, CS must be pulled low once after the instruction is sent. After power on, the device is by default in the EWDS state. An EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. The following are the functional descriptions and timing diagrams of all seven instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. The 8 bit or 16 bit data stream is preceded by a logical ″0″ dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power on and power off state the device automatically enters the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise any ERASE/WRITE instructions will be invalid. After the EWEN instruction is issued, the programming enable condition remains until the power is removed off until an EWDS instruction is issued. No data can be written into the device in the programming disable state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erase is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the internal erase, the SK clock is not required. During the internal erase, the busy/ready status can be verified by keeping CS high. If busy, the DO pin will remain low but when the operation is over, the DO pin will return to a high level permitting further instructions to be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the internal writing, the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. It is therefore not necessary to erase data before the WRITE instruction is issued. During the internal writing, the busy/ready status can be verified by keeping CS high. If busy, the DO pin will remain low but when the operation is over, the DO pin will return to a high level permitting further instructions to be executed.

ERAL

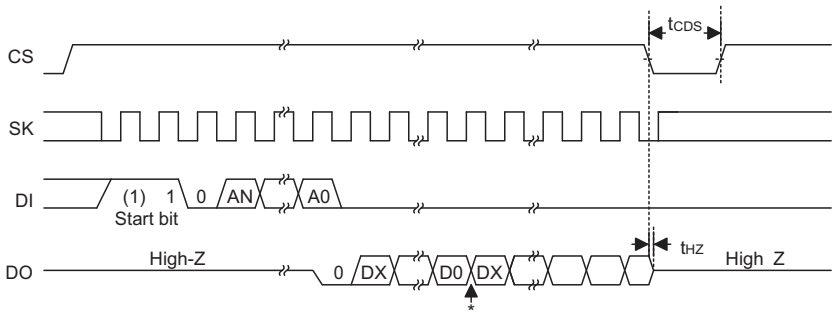
The ERAL instruction erases the entire 1024×16 or 2048×8 memory cells to a logical ″1″ state in the programming enable mode. After the erase-all instruction has been issued, the data erase feature is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, the SK clock is not required. During the internal erase-all operation, the busy/ready status can be verified by keeping CS high. If busy, the DO pin will remain low but when the operation is over, the DO pin will return to a high level permitting further instructions to be executed.

WRAL

The WRAL instruction writes data into the entire 1024×16 or 2048×8 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, the SK clock is not required. During the internal write-all operation, the busy/ready status can be verified by keeping CS high. If busy, the DO pin will remain low but when the operation is over, the DO pin will return to a high level permitting further instructions to be executed.

Timing Diagrams

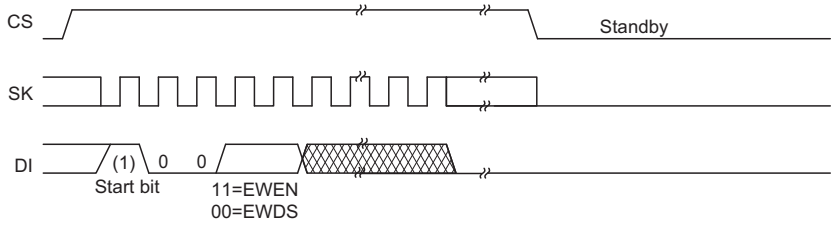
READ



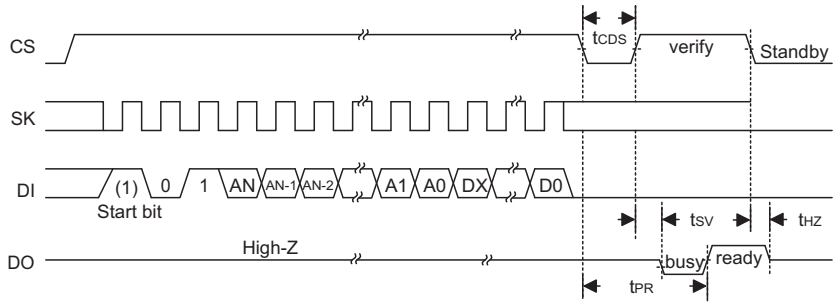
* Address pointer automatically cycles to the next word

Mode	(X16)	(X8)
AN	A9	A10
DX	D15	D7

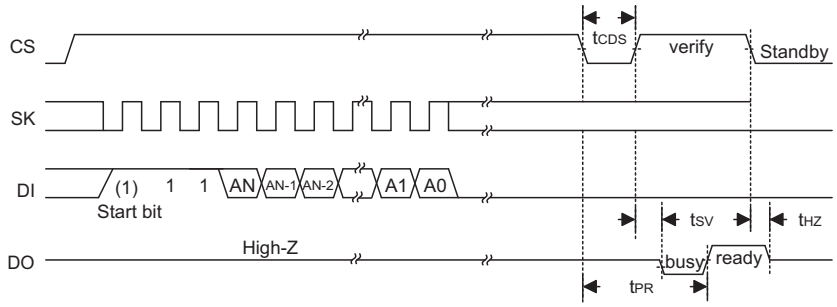
EWEN/EWDS



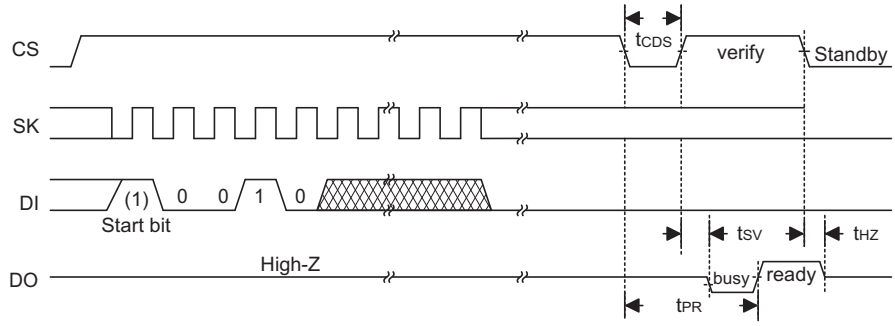
WRITE



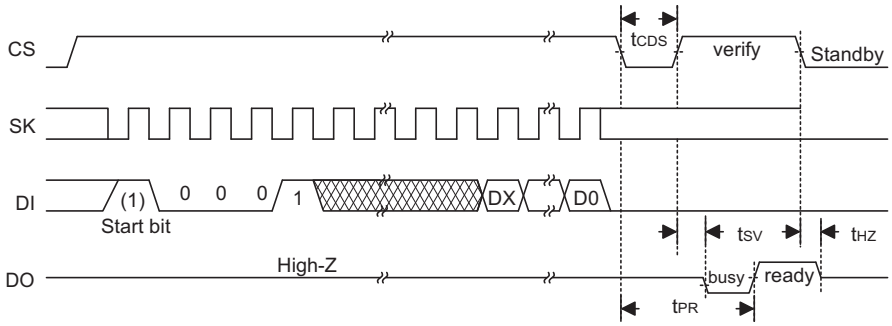
ERASE



ERAL



WRAL



Instruction Set Summary

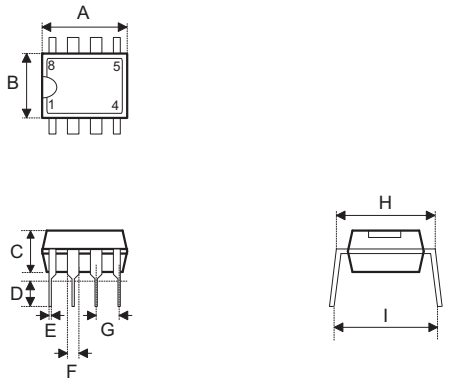
Instruction	Comments	Start Bit	Op Code	Address ORG=0 X8	Address ORG=1 X16	Data ORG=0 X8	Data ORG=1 X16
READ	Read data	1	10	A10~A0	A9~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A10~A0	A9~A0	—	
WRITE	Write data	1	01	A10~A0	A9~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXXXX	11XXXXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXXXX	00XXXXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXXXX	10XXXXXXXX	—	
WRAL	Write All	1	00	01XXXXXXXXX	01XXXXXXXX	D7~D0	D15~D0

Note: ″X″ stands for don′t care

Data should be written to the EEPROM in the format (8-bit or 16-bit mode) in which it is to be read.

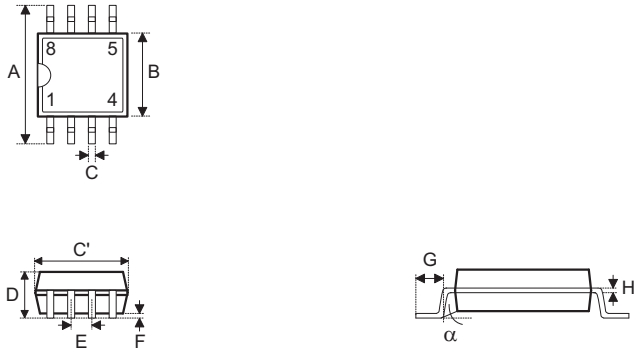
Package Information

8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	—	—	375

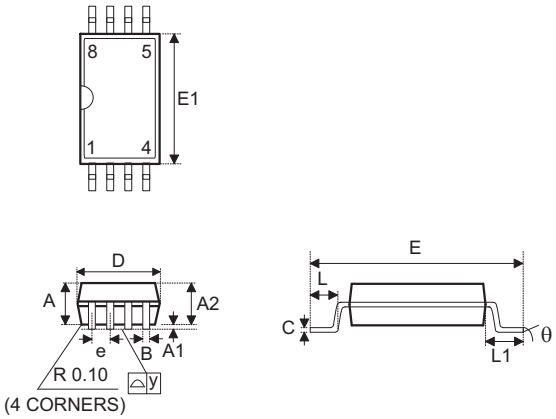
8-pin SOP (150mil) Outline Dimensions



• MS-012

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	150	—	157
C	12	—	20
C′	188	—	197
D	—	—	69
E	—	50	—
F	4	—	10
G	16	—	50
H	7	—	10
α	0°	—	8°

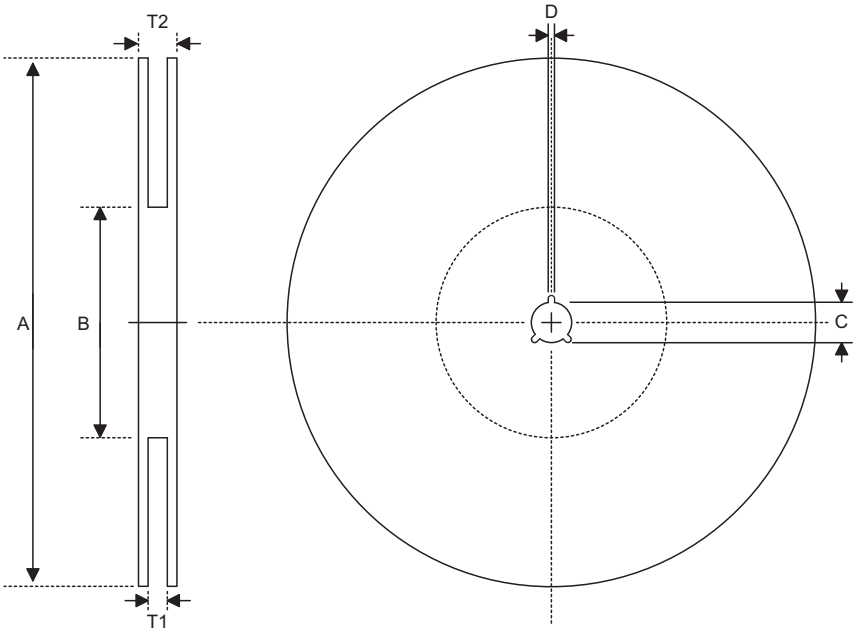
8-pin TSSOP Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.20
A1	0.05	—	0.15
A2	0.95	—	1.05
B	—	0.25	—
C	0.11	—	0.15
D	2.90	—	3.10
E	6.20	—	6.60
E1	4.30	—	4.50
e	—	0.65	—
L	0.50	—	0.70
L1	0.90	—	1.10
y	—	—	0.10
θ	0°	—	8°

Product Tape and Reel Specifications

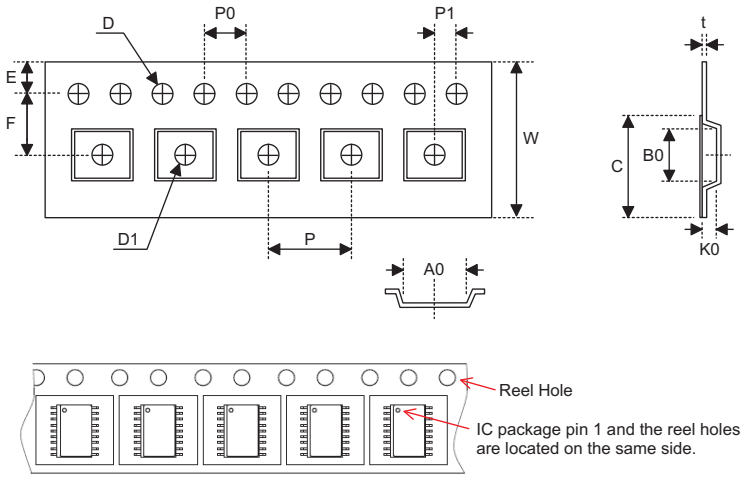
Reel Dimensions



SOP 8N, TSSOP 8L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.10
D1	Cavity Hole Diameter	1.50+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

TSSOP 8L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	5.5±0.5
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.5^{+0.1/-0.0}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	7.0±0.1
B0	Cavity Width	3.6±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.300±0.013
C	Cover Tape Width	9.3±0.1

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