EF7910

ADVANCE INFORMATION

FSK MODEM

The EF7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. It is pin selectable for baud rates of 300, 600 or 1200 bits per second and is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

Digital signal processing techniques are employed in the EF7910 to perform all major functions such as modulation, demodulation and filtering. The EF7910 contains on-chip analog-to-digital and-digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

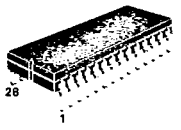
The EF7910 is fabricated using HMOS technology in a 28-pin package. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ± 5 volts.

- Complete FSK MODEM in a 28-pin package - just add line interface
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications
- No external filtering required
- All digital signal processing, digital filters and ADC/DAC included on-chip
- Includes essential RS-232/CCITT V.24 handshake signals
- Auto-answer capability
- Local copy/test modes
- 1200 bps full duplex on 4-wire line
- Pin-programmable mode section.

HMOS

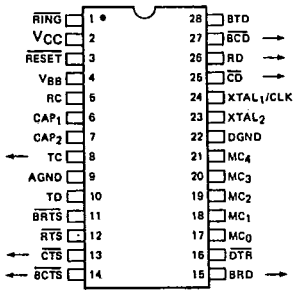
FSK MODEM

CASE CB-132



J SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT



Ref.01930

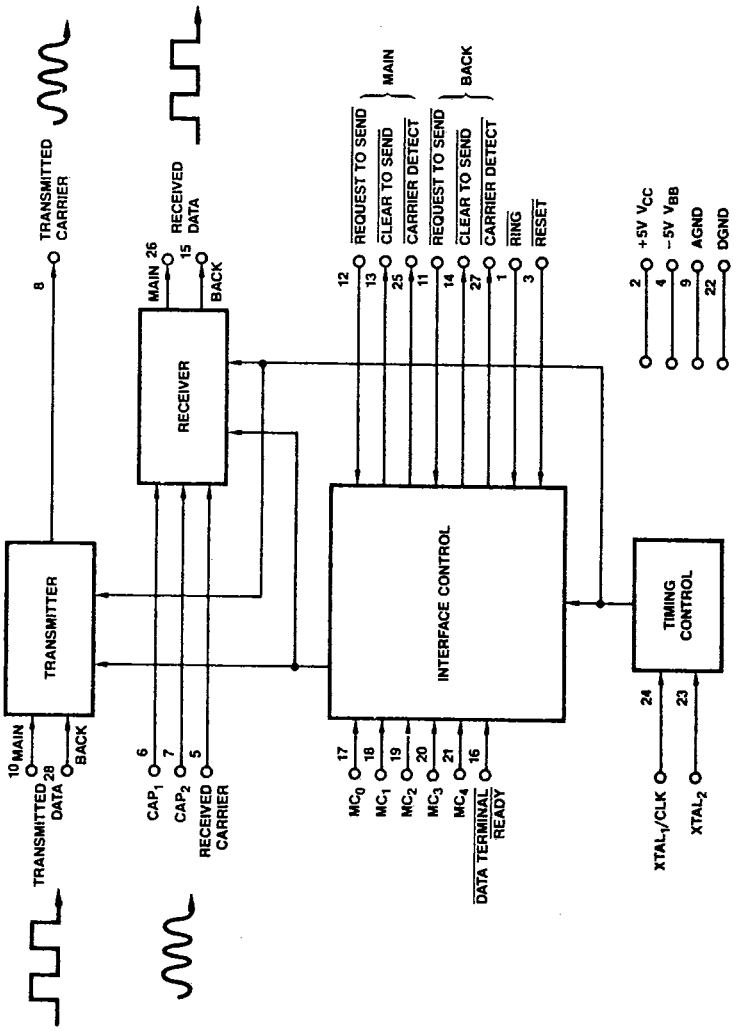


Figure 1. EF7910 Block Diagram

INTERFACE SIGNAL DESCRIPTION

MC_0-MC_4 (CONTROL INPUTS)

These five inputs select one of thirty-two modem configurations according to the Bell or CCITT specifications listed in Table 1. Only 19 of these 32 modes are actually available to the user.

Modes 0-8 are the normal operation modes. The 1200 Baud modes can be selected with or without a compromise equalizer.

Modes 16-25 permit loop back of the EF7910 transmitter and receiver. No internal connection is made. The user must externally connect the TRANSMITTED CARRIER pin (Figure 2) to the RECEIVED CARRIER pin if analog loopback is required. For digital loopback, external connection of RECEIVED DATA and TRANSMITTED DATA is required. Whenever a mode in this group is selected, the effect is to set all transmit and receive filters to the same channel frequency band so that loopback can be performed.

Modes 9-15 and 26-31 are reserved and should not be used.

DATA TERMINAL READY ($\overline{DTR}$)

A LOW level on this input indicates the data terminal desires to send and/or receive data via the modem. This signal is gated with all other TTL inputs and outputs so that a low level enables all these signals as well as the internal control logic to function. A HIGH level disables all TTL I/O pins and the internal logic.

REQUEST TO SEND ($\overline{RTS}$)

A LOW level on this input instructs the modem to enter transmit mode. This input must remain LOW for the duration of data transmission. The signal has no effect if $\overline{DATA\ TERMINAL\ READY}$ is HIGH (disabled). A HIGH level on this input turns off the transmitter.

CLEAR TO SEND ($\overline{CTS}$)

This output goes LOW at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes LOW. Actual data to be transmitted should not be presented to the TRANSMITTED DATA input until a LOW is indicated on the $\overline{CLEAR\ TO\ SEND}$ output. Normally the user should force the TD input HIGH whenever $\overline{CTS}$ is off (HIGH). This signal never goes LOW as long as $\overline{DTR}$ is HIGH (disabled). $\overline{CLEAR\ TO\ SEND}$ goes HIGH at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes HIGH.

CARRIER DETECT ($\overline{CD}$)

A LOW on this output indicates that a valid carrier signal is present at the receiver and has been present for at least a time, t_{CDON}, where t_{CDON} depends upon the selected modem configuration (Table 3b). A HIGH on this output signifies that no valid carrier is being received and has not been received for a time, t_{CDOFF}. $\overline{CARRIER\ DECTECT}$ remains HIGH when $\overline{DTR}$ is HIGH. Values for t_{CDON} and t_{CDOFF} are configuration dependent and are listed in Table 3b.

TRANSMITTED DATA (TD)

Data bits to be transmitted are presented on this input serially; HIGH (mark) corresponds to logic 1 and LOW (space) corresponds to logic 0. This data determines which frequency appears at any instant at the TRANSMITTED CARRIER output pin (Table 3a). No signal appears at the TRANSMITTED CARRIER output unless $\overline{DTR}$ is LOW and $\overline{RTS}$ is LOW.

RECEIVED DATA (RD)

Data bits demodulated from the RECEIVED CARRIER input are available serially at this output; HIGH (mark) indicates logic 1 and LOW (space) indicates logic 0. Under the following conditions this output is forced to logic 1 because the data may be invalid:

1. When $\overline{CARRIER\ DETECT}$ is HIGH
2. During the internal squelch delay at half-duplex line turn around (202/V.23 modes only)
3. During soft carrier turnoff at half-duplex line turn around (202 mode only)
4. When $\overline{DTR}$ is HIGH
5. When $\overline{RTS}$ ON and $\overline{BRTS}$ OFF in V.23/202 modes only
6. During auto-answer sequence

BACK REQUEST TO SEND ($\overline{BRTS}$)

Since the 1200 bps modem configurations, Bell 202 and CCITT V.23, permit only half duplex operation over two-wire lines, a low baud rate "backward" channel is provided for transmission from the main channel receiver to the main channel transmitter. This input signal ($\overline{BRTS}$) is equivalent to $\overline{REQUEST\ TO\ SEND}$ for the main channel, except it belongs to the backward channel. Note that since the EF7910 contains a single transmitter, $\overline{RTS}$ and $\overline{BRTS}$ should not be asserted simultaneously. $\overline{BRTS}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. In all other modes it is ignored.

For V.23 mode the frequency appearing at the transmitted carrier (TC) output pin is determined by a MARK or SPACE at the back transmitted data ($\overline{BTD}$) input (Table 3a).

For 202 mode a frequency of 387Hz appears at TC when $\overline{BRTS}$ is LOW and BTD is HIGH. No energy (0.0 volt) appears at TC when $\overline{BRTS}$ is HIGH. BTD should be fixed HIGH for 202 back channel transmission. The signal, $\overline{BRTS}$, then is equivalent to the signal, Secondary Request-to-Send, for 202 S/T modems, or Supervisory Transmitted Data for 202 C/D modems.

BACK CLEAR TO SEND ($\overline{BCTS}$)

This line is equivalent to $\overline{CLEAR\ TO\ SEND}$ for the main channel, except it belongs to the back channel. $\overline{BCTS}$ is meaningful only when a V.23 mode is selected by MC_0-MC_4. This signal is not used in Bell 202 back mode.

BACK CARRIER DETECT ($\overline{BCD}$)

This line is equivalent to $\overline{CARRIER\ DETECT}$ for the main channel, except it belongs to the backward channel. $\overline{BCD}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For V.23 back channel mode, $\overline{BCD}$ turns on when either the MARK or SPACE frequency appears with sufficient level at the received carrier (RC) input.

For 202 back channel mode, $\overline{BCD}$ turns on in response to a 387Hz tone of sufficient level at the RC input. In this case $\overline{BCD}$ is equivalent to the signal, Secondary Received Line Signal Detector, for 202 S/T modems, or Supervisory Received Data for 202 C/D modems.

BACK TRANSMITTED DATA (BTD)

This line is equivalent to TRANSMITTED DATA for the main channel, except it belongs to the back channel. BTD is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For 202 back transmission of on/off keying, BTD should be fixed at a HIGH level.

BACK RECEIVED DATA (BRD)

This line is equivalent to RECEIVED DATA (except clamping) for the main channel, except it belongs to the back channel. BRD is meaningful only when a V.23 mode is selected by MC_0-MC_4. Under the following conditions this output is forced HIGH:

1. $\overline{BRD}$ HIGH
2. $\overline{DTR}$ HIGH
3. V.21/103 mode
4. During auto-answer
5. When $\overline{BRTS}$ ON and $\overline{RTS}$ OFF in V.23 modes only

87D 08626 D T-75-33-05

TRANSMITTED CARRIER (TC)

This analog output is the modulated carrier to be conditioned and sent over the phone line.

RECEIVED CARRIER (RC)

This input is the analog signal received from the phone line. The modem extracts the information contained in this modulated carrier and converts it into a serial data stream for presentation at the RECEIVED DATA (BACK RECEIVED DATA) output.

$\overline{RING}$

This input signal permits auto-answer capability by responding to a ringing signal from a data access arrangement. If a ringing signal is detected (RING LOW) and DTR is LOW, the modem begins a sequence to generate an answer tone at the TC output.

$XTAL_1$, $XTAL_2$

Master timing of the modem is provided by either a crystal connected to these two inputs or an external clock inserted into $XTAL_1$. The value of the crystal or the external clock frequency must be 2.4576MHz ±.01%.

V_{CC}

+5 volt power supply. (±5%)

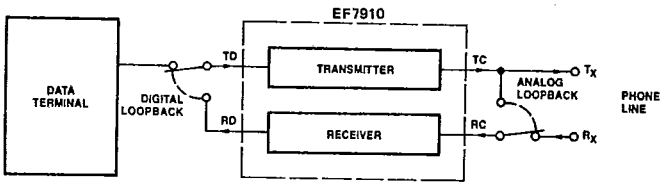
V_{BB}

−5 volt power supply. (±5%)

TABLE 1.

MC_4	MC_3	MC_2	MC_1	MC_0	
0	0	0	0	0	Bell 103 Originate 300bps full duplex
0	0	0	0	1	Bell 103 Answer 300bps full duplex
0	0	0	1	0	Bell 202 1200bps half duplex
0	0	0	1	1	Bell 202 with equalizer 1200bps half duplex
0	0	1	0	0	CCITT V.21 Orig 300bps full duplex
0	0	1	0	1	CCITT V.21 Ans 300bps full duplex
0	0	1	1	0	CCITT V.23 Mode 2 1200bps half duplex
0	0	1	1	1	CCITT V.23 Mode 2 with equalizer 1200bps half duplex
0	1	0	0	0	CCITT V.23 Mode 1 600bps half duplex
0	1	0	0	1	Reserved
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	Bell 103 Orig loopback
1	0	0	0	1	Bell 103 Ans loopback
1	0	0	1	0	Bell 202 Main loopback
1	0	0	1	1	Bell 202 with equalizer loopback
1	0	1	0	0	CCITT V.21 Orig loopback
1	0	1	0	1	CCITT V.21 Ans loopack
1	0	1	1	0	CCITT V.23 Mode 2 main loopback
1	0	1	1	1	CCITT V.23 Mode 2 with equalizer loopback
1	1	0	0	0	CCITT V.23 Mode 1 main loopback
1	1	0	0	1	CCITT V.23 Back loopback
1	1	0	1	0	Reserved
1	1	0	1	1	
1	1	1	0	0	
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

Figure 2. Loopback Configurations



87D 08627 T-75-33-05

DGND

Digital signal ground pin.

AGND

Analog signal ground pin (for TRANSMITTED CARRIER and RECEIVED CARRIER).

CAP_1, CAP_2

Connection points of external capacitor/resistor required for proper operation of on-chip analog-to-digital converter.

Recommended values are: C = 2000pF ±10%,
R = 100Ω ±10%.

$\overline{RESET}$

This input signal is for a reset circuit which operates in either of two modes. It automatically resets when power is applied to the device, or it can be activated by application of an external active low TTL pulse.

THEORY OF OPERATION

The EF7910 MODEM consists of three main sections, shown in the block diagram of Figure 1 – Transmitter, Receiver, and Interface Control.

TRANSMITTER (Modulator)

The transmitter, shown in Figure 3, receives binary digital data from a source such as a UART and converts the data to an analog signal using frequency shift keying (FSK) modulation. This analog signal is applied to the phone line through a DAA or acoustic coupler. FSK is a modulation technique which encodes one bit per baud. A logic one applied to the TRANSMITTED DATA (TD) input causes a sine wave at a given frequency to appear at the analog TRANSMITTED CARRIER (TC) output. A logic zero applied to input TD causes a sine wave of a different frequency to appear at the TC ouput. As the data at the TD input switches between logical one and zero, the TC output switches between the two frequencies. In the EF7910 this switching between frequencies is phase continuous. The frequencies themselves are digitally synthesized sine functions.

The frequencies for each modem configuration available in the EF7910 are listed in Table 3a.

The process of switching between two frequencies as in FSK generates energy at many more frequencies than the two used in the modulation. All the transmitted information can be recovered from a frequency band B Hz wide, where B is the bit rate or maximum rate of change of the digital data at the TD input. This band is centered about a frequency, f_C,
where $f_C = f_1 + (f_2 - f_1)/2$
(f_1 = lower of two FSK frequencies)
(f_2 = higher of two FSK frequencies)

In addition to this primary information band, there exist side bands containing redundant information. It is desirable to attenuate these bands for two reasons:

1. The phone companies have specifications on the amount of energy allowed in certain frequency bands on the line.
2. If two independent information channels are present simultaneously on the line (e.g. 300 bps full duplex or 1200 bps half duplex with back), the redundant transmitter components may fall in the frequency band of the local receiver channel and interfere with detection. In the EF7910 these redundant and undesirable components are attenuated by digital bandpass filters.

Following the digital bandpass filters, the filtered FSK signal is converted to an analog signal by an on-chip DAC operating at a high sample rate. This analog FSK signal is finally smoothed by a simple on-chip analog low pass filter.

RECEIVER (Demodulator)

A simplified block diagram of the EF7910 FSK receiver is shown in Figure 4. Data transmitted from a remote site modem over the phone line is an FSK-modulated analog carrier. This carrier is applied to the RECEIVED CARRIER (RC) pin via a DAA or acoustic coupler. The first stage of the demodulator is a simple on-chip analog low pass anti-alias filter. The output of this is converted into digital form and filtered by digital bandpass filters to improve the signal to noise ratio and reject other independent channel frequencies associated with the phone line in the case of full duplex configuration. The bandpass filtered output is digitally demodulated to recover the binary data. A carrier detect signal is also digitally extracted from the received line carrier to indicate valid data.

Figure 3. Transmitter Block Diagram

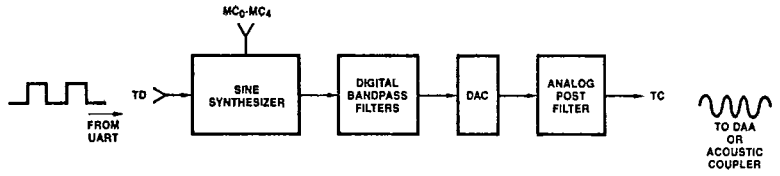
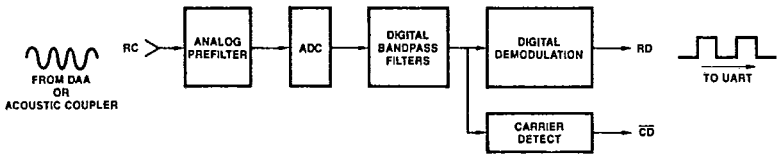


Figure 4. Receiver Block Diagram



INTERFACE CONTROL

This section controls the handshaking between the modem and the local terminal. It consists primarily of delay generation counters, two state machines for controlling transmission and reception, and mode control decode logic for selecting proper transmit frequencies and transmit and receive filters according to the selected modem type. Inputs and outputs from this section are as follows:

$\overline{\text{REQUEST TO SEND}}$ (Main and Back)
$\overline{\text{CLEAR TO SEND}}$ (Main and Back)
$\overline{\text{CARRIER DETECT}}$ (Main and Back)
$\overline{\text{RING}}$
MC0-MC4
$\overline{\text{DATA TERMINAL READY}}$

Internal logic clamps protocol signals to different levels under certain conditions (e.g., initial conditions).

When Bell 103/113 and V.21 modem configurations are selected, the back channel signals are non-functional.

Figures 7 and 8 depict the sequencing of the two state machines. State machine 1 implements main or back channel transmission and the auto-answer sequence. State machine 2 implements reception on main or back channel.

The state machine powers on to the state labelled INITIAL CONDITIONS. Handshake signals are set to or assumed to be the levels listed in Table 2. The machine then waits for $\overline{\text{DATA TERMINAL READY}}$ ($\overline{\text{DTR}}$) to be turned on. Whenever $\overline{\text{DTR}}$ is turned to the OFF state from an ON condition, each state machine and external signals return to the initial conditions within 25 microseconds. After $\overline{\text{DTR}}$ is turned ON the EF7910 becomes operational as a modem and the state machines proceed as depicted in the flowcharts.

The definitions of the terms Full Duplex and Half Duplex used in these flowcharts are depicted below (Figs. 5 and 6). "Full Duplex" applies to all 103/113, V.21 modes. "Half Duplex" applies to 202 and V.23, both forward and backward channel.

Full Duplex: Data can be transmitted and received simultaneously at a rate of 300 baud. Two independent 300Hz channels are frequency multiplexed into the 3000Hz bandwidth of the phone line. The EF7910 configurations for the Bell 103/113 and CCITT V.21 can be operated full duplex.

Half Duplex: In half duplex with back channel, the modem may transmit at 1200/600 baud and receive at 5/75 baud. Alternatively it may transmit at 5/75 baud and receive at 1200/600 baud. Examples are Bell 202 and CCITT V.23.

TABLE 2.
INITIAL CONDITIONS

Data Terminal Ready ($\overline{\text{DTR}}$)	OFF
Request to Send ($\overline{\text{RTS}}$)	OFF
Clear to Send ($\overline{\text{CTS}}$)	OFF
Transmitted Data (TD)	Ignored
Back Channel Request to Send ($\overline{\text{BRTS}}$)	OFF
Back Channel Clear to Send ($\overline{\text{BCTS}}$)	OFF
Back Channel Transmitted Data (BTD)	Ignored
Ring ($\overline{\text{RING}}$)	OFF
Carrier Detect ($\overline{\text{CD}}$)	OFF
Received Data (RD)	MARK
Back Channel Carrier Detect ($\overline{\text{BCD}}$)	OFF
Back Channel Received Data (BRD)	MARK

Figure 5. Full Duplex

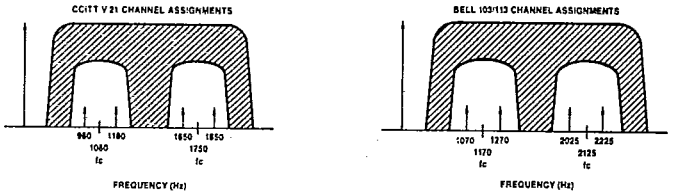


Figure 6. Half Duplex

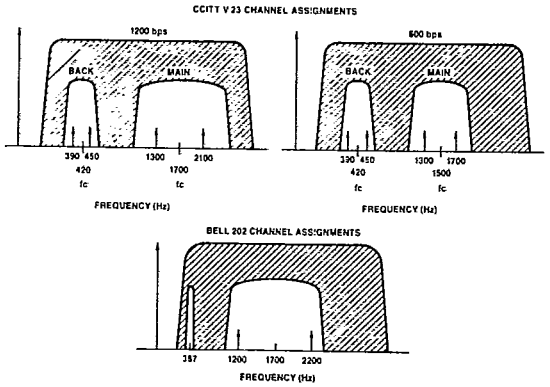


TABLE 3(a). FREQUENCY PARAMETERS

Modem	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		Answer Tone Freq Hz
			Space Hz	Mark Hz	Space Hz	Mark Hz	
Bell 103 Orig	300	Full	1070	1270	2025	2225	–
Bell 103 Ans	300	Full	2025	2225	1070	1270	2225
CCITT V.21 Orig	300	Full	1180	980	1850	1650	–
CCITT V.21 Ans	300	Full	1850	1650	1180	980	2100
CCITT V.23 Mode 1	600	Half	1700	1300	1700	1300	2100
CCITT V.23 Mode 2	1200	Half	2100	1300	2100	1300	2100
CCITT V.23 Mode 2 Equalized	1200	Half	2100	1300	2100	1300	2100
Bell 202	1200	Half	2200	1200	2200	1200	2025
Bell 202 Equalized	1200	Half	2200	1200	2200	1200	2025
CCITT V.23 Back	75	–	450	390	450	390	–
Bell 202 Back	5	–	*	*	**	**	–

*($\overline{\text{BRTS}}$ LOW) and (BTD HIGH): 387Hz at TC
*($\overline{\text{BRTS}}$ HIGH) or (BTD LOW) : 0 volt at TC
*Meets new CCITT R20 frequency tolerance.
**387Hz at RC: $\overline{\text{BCD}}$ LOW
**No 387Hz at RC: $\overline{\text{BCD}}$ HIGH

Frequency tolerance is less than ±0.4Hz with 2.4576MHz Crystal. Except Bell 202 which is +1Hz (1200 Hz, mark)

TABLE 3(b). TIMING PARAMETERS (Refer to Figures 9, 10 and 11 for Timing Diagrams)

Symbol	Description	Bell 103 Orig	Bell 103 Ans	CCITT V.21 Orig	CCITT V.21 Ans	CCITT V.23 Mode 1	CCITT V.23 Mode 2	CCITT V.23 Mode 2 EQ	Bell 202	Bell 202 EQ	CCITT V.23 Back	Bell 202 Back	Units
$t_{RC(On)}$	Request-to-Send to Clear-to-Send ON Delay	208.3	208.3	400	400	208.3	208.3	208.3	183.3	183.3	–	–	msec ±0.3%
$t_{RC(Off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	–	–	msec ±0.25%
$t_{BRC(On)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay	–	–	–	–	–	–	–	–	–	82.3	–	msec ±0.64%
$t_{BRC(Off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay	–	–	–	–	–	–	–	–	–	0.5	–	msec ±25%
$t_{CD(On)}$	Carrier Detect ON Delay	94-106	94-106	301-312	301-312	11.4-15.4	11.4-15.4	11.4-15.4	18-22	18-22	–	–	msec
$t_{CD(Off)}$	Carrier Detect OFF Delay	21-40	21-40	21-40	21-40	5.4-13.3	5.4-13.3	5.4-13.3	12.4-23.4	12.4-23.4			msec
$t_{BCD(On)}$	Back Channel Carrier Detect ON Delay	–	–	–	–	–	–	–	–	–	17-25	17-25	msec
$t_{BCD(Off)}$	Back Channel Carrier Detect OFF Delay	–	–	–	–	–	–	–	–	–	21-38	21-38	msec
t_{AT}	Answer Tone Duration	–	1.9	–	3.0	3.0	3.0	3.0	1.9	1.9	–	–	sec ±0.44%
t_{SIL}	Silence Interval before Transmission	1.3	1.3	1.9	1.9	1.9	1.9	1.9	1.3	1.3	–	–	sec ±0.64%
t_{SQ}	Receiver Squelch Duration	–	–	–	–	156.3	156.3	156.3	156.3	156.3	–	–	msec ±3.3%
t_{STO}	Transmitter Soft Turn-Off Duration	–	–	–	–	–	–	–	24	24	–	–	msec ±2.3%
t_{RI}	Minimum $\overline{\text{RI}}$ Low Duration	–	25	–	25	25	25	25	25	25	–	–	µs

CALL ESTABLISHMENT

Before two modems can exchange data, an electrical connection through the phone system must be established. Although it may assist in call establishment, a modem typically does not play a major role. A call may be originated manually or automatically and it may be answered manually or automatically.

Manual Calling – Manual calling is performed by a person who dials the number, waits for an answer , then places the calling modem into data transmission mode.

Automatic Calling – Automatic calling is typically performed by an automatic calling unit (ACU) which generates the appropriate dialing pulse or dual-tone sequence required to call the remote (called) modem. The ACU also has the ability to detect an answer tone from the called modem and place the calling modem into data transmission mode.

Manual Answering – Manual answering is performed by a person who hears the phone ring, lifts the receiver, causes the called modem to send an answer tone to the calling modem, and places the called modem into data transmission mode.

Automatic Answering – Automatic answering is performed by a called modem with a data access arrangement (DAA). The DAA detects a ringing signal, takes the phone circuit off-hook (corresponding to lifting the receiver) and instructs the called modem to commence the auto-answer sequence. Next the called modem sends out silence on the line, followed by an answer tone. When this tone is detected by the calling modem, the connection is considered to have been established.

The EF7910 provides assistance for automatic answering through the $\overline{\text{RING}}$ signal as follows. Observe the upper right-hand portion of Figure 7(a). Assume that DATA TERMINAL READY ($\overline{\text{DTR}}$) has recently been asserted to cause exit from the initial conditions. Note that if $\overline{\text{DTR}}$ remains OFF, $\overline{\text{RING}}$ is ignored. Assume also that $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are OFF and that the mode control lines (MCO-MC4) select a normal modem configuration, not a loopback mode. Automatic answering is initiated by receipt of a LOW level at the $\overline{\text{RING}}$ input, causing entrance to the auto-answer sequence depicted in Figure 7(c).

The EF7910 outputs silence (0.0 volt) at its TRANSMITTED CARRIER (TC) output for a time, t_{SIL}, followed by the answer tone for a time, t_{AT}. The $\overline{\text{CARRIER DETECT}}$ ($\overline{\text{CD}}$) pin is clamped OFF and the RECEIVED DATA (RD) signal is therefore clamped to a MARK (HIGH) during the auto-answer sequence. Upon completion of the answer tone, $\overline{\text{CD}}$ is released. If the mode lines (MCO-MC4) select a 202 or V.23 mode, the transmit filters are set to the forward channel and the receive filters are set to the back channel during the auto answer sequence.

At the end of the auto-answer sequence, return is made to point A in the loop at the upper right-hand portion of Fig. 7(a). Note that since the answer flag has been set, the auto-answer sequence cannot be entered again unless $\overline{\text{DTR}}$ is first turned OFF, then ON. At this point the phone line connection has been established and data transmission or reception may begin.

The $\overline{\text{RING}}$ input may be activated from a conditioned DAA Ring Indicator output for automatic answering or it may be activated by a switch for manual answering. Tying $\overline{\text{RING}}$ HIGH will disable the auto-answer function of the EF7910.

DATA TRANSMISSION

Full Duplex

Following call establishment, full duplex data transmission can be started by either the called or calling modem. In other words, if the connection has been established and the modem is looping through point A in Figure 7(a), it no longer matters which is the called and which is the calling modem. Data transmission is initiated by asserting $\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$). At this time the TRANSMITTED DATA (TD) input will be released and a modulated carrier can appear at the TRANSMITTED CARRIER (TC) output. Following a delay, t_{RCON}, $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) will turn ON. At this time, data may be transmitted through the TD input. It is a common protocol for the user to always present a MARK at the TD input before $\overline{\text{RTS}}$ is asserted and during the t_{RCON} delay.

Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. Following a short delay, t_{RCOFF}, $\overline{\text{CTS}}$ turns OFF. As soon as $\overline{\text{RTS}}$ goes OFF, the TD input is ignored and the TC output is set to 0.0 volt (silence). After $\overline{\text{CTS}}$ turns OFF, the state machine returns to point A in Figure 7(a).

Half Duplex

When a half duplex mode is selected (202 or V.23), data transmission can be either on the main channel at 1200/600 baud or on the back channel at 5/75 baud. In normal half duplex operation a single modem is either transmitting on the main and receiving on the back channel or vice versa. In the EF7910 control of the transmitter and receiver filters to the proper channel is performed by $\overline{\text{RTS}}$. When $\overline{\text{RTS}}$ is asserted, the transmitter filters and synthesizer are set to transmit on the main channel; the receiver filters are set to receive on the back channel. Therefore, whenever $\overline{\text{RTS}}$ is on, $\overline{\text{BRTS}}$ should not be asserted since the transmitter cannot be used for the back channel. When $\overline{\text{RTS}}$ is OFF and a half duplex mode is selected, the transmitter filters and synthesizer are set to the back channel; the receiver filters are set to the main channel. If $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are asserted simultaneously, $\overline{\text{RTS}}$ will take precedence. However, if $\overline{\text{BRTS}}$ is asserted before $\overline{\text{RTS}}$ and the back channel data transmission sequence has been entered (Figure 7(b)), $\overline{\text{RTS}}$ will be ignored until $\overline{\text{BRTS}}$ is turned OFF.

The state machine sequences for main and back channel transmission differ slightly and are depicted in Figure 7. Assume the state machine is idling through point A in Figure 7(a).

Main Channel

This transmission sequence is entered if a 202 or V.23 mode is selected and $\overline{\text{RTS}}$ is asserted. Since the receiver is now forced to the back channel, the RECEIVED DATA (RD) signal is clamped to a MARK; and the $\overline{\text{CARRIER DETECT}}$ signal is clamped OFF. The TRANSMITTED DATA input (TD) is released and a carrier appears at the TRANSMITTED CARRIER output which follows the MARK/SPACE applied to TD. $\overline{\text{RTS}}$ turning ON initiates a delay, t_{RCON}, at the end of which the $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) output goes LOW. When $\overline{\text{CTS}}$ goes LOW data may be transmitted through input TD. Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. At this time several events are initiated. First a delay, t_{RCOFF}, is initiated at the end of which $\overline{\text{CTS}}$ turns OFF. The TD input is ignored as soon as $\overline{\text{RTS}}$ goes OFF. If a 202 mode is selected, a soft turn-off tone appears at the TC output for a time, t_{STO}, followed by silence (0.0 volt). For both 202 and V.23 modes a squelch period, t_{SQ}, is initiated when $\overline{\text{RTS}}$ goes OFF. During this period the $\overline{\text{CD}}$ output is clamped OFF, forcing the RD output to a MARK condition. The squelch period begins as soon as $\overline{\text{RTS}}$ goes OFF and thus overlaps both t_{RCOFF} and t_{STO}. At the end of the squelch period, the state machine returns to the idle loop at point A in Figure 7(a).

The reasons for squelch and soft-turnoff are as follows:

Soft Turn-Off: When $\overline{\text{RTS}}$ is turned OFF at the end of a message, transients occur which may cause spurious space signals to be received at a remote modem. During soft turn-off the modem transmits a soft carrier frequency for a period, t_{STO}, after $\overline{\text{RTS}}$ is

turned OFF. This results in a steady MARK on the RECEIVED DATA (RD) line of the remote modem.

Squelch: The local receiver must be turned OFF after $\overline{RTS}$ is OFF, until the start of carrier detect, so that line transients are not demodulated. The process of disabling the receiver after $\overline{RTS}$ is turned OFF is called squelching.

Back Channel

This transmission sequence, shown in Figure 7(b), is entered if a 202 or V.23 mode is selected, $\overline{RTS}$ is OFF, and $\overline{BRTS}$ is asserted. The BACK CARRIER DETECT ($\overline{BCD}$) output is forced OFF and the BACK RECEIVED DATA (BRD) output is clamped to a MARK. The BACK TRANSMITTED DATA input (BTD) is released and a carrier appears at the TC output which follows the MARK/SPACE applied to BTD. Turning ON $\overline{BRTS}$ initiates a delay, t_{BRCON}, at the end of which the BACK CLEAR TO SEND ($\overline{BCTS}$) output goes LOW. When $\overline{BCTS}$ goes LOW data may be transmitted through input BTD. Data transmission continues until $\overline{BRTS}$ is turned OFF. The input BTD is immediately ignored and the TC output is silenced (set to 0.0 volt). Following a short delay, t_{BRCOFF}, the output $\overline{BCTS}$ goes OFF. The signals $\overline{BCD}$ and BRD are released and the state machine returns to idle at point A of Figure 7(a).

In 202 back channel mode, BTD should be tied HIGH. Then $\overline{BRTS}$ controls the ON/OFF keying modulation. When $\overline{BRTS}$ is LOW, 387Hz appears at the TC output; when $\overline{BRTS}$ is HIGH, 0 volt appears at TC.

DATA RECEPTION

Data reception is controlled by state machine 2 and depicted in Figure 8. At power on the machine enters initial conditions and remains there until $\overline{DTR}$ is asserted. It then loops until either CARRIER DETECT($\overline{CD}$) or BACK CARRIER DETECT ($\overline{BCD}$) occurs.

Full Duplex

In full duplex data reception, CARRIER DETECT may appear at any time after the phone connection has been established. Reception is independent of transmission. When the receiver detects a valid carrier for at least a time, t_{CDON}, the output $\overline{CD}$ is turned ON, the RECEIVED DATA (RD) output is released, and valid data can be obtained at RD. Data is received until the receiver detects loss of carrier for at least a time, t_{CDOFF}. At this time the $\overline{CD}$ output is turned OFF and RD is clamped to a MARK. The state machine returns to the idle loop at point E.

Half Duplex

As discussed in the data transmission section above, when a half duplex mode has been selected, the signal $\overline{RTS}$ controls whether the main channel is transmitting or receiving. The back channel can only do the opposite from the main. If $\overline{RTS}$ is OFF, then CARRIER DETECT may be asserted and the data reception sequence is identical to that discussed above for full duplex reception. As long as $\overline{RTS}$ remains OFF, BACK CARRIER DETECT will never be asserted. If $\overline{RTS}$ is ON, then CARRIER DETECT will never be asserted. Instead the receiver will look for a valid carrier in the back channel frequency band. If a valid carrier exists for at least a time, t_{BCDON}, the output BACK CARRIER DETECT ($\overline{BCD}$) is turned ON, the BACK RECEIVED DATA (BRD) output is released and valid data can be obtained at BRD. Data is received until the receiver detects loss of back channel received signal for at least time, t_{BCDOFF}. At this time the $\overline{BCD}$ output is turned OFF. Data output, BRD, is clamped to a MARK if a V.23 mode is selected. For 202 back channel mode, $\overline{BCD}$ represents the received data. The BRD output can be ignored. The state machine returns to the idle loop at point E.

LOOPBACK

Ten modes exist to allow both analog and digital loopback for each modem specification met by the EF7910. When a loopback mode is selected, the signal processing (filters, etc.) for both the transmitter and receiver is set to process the same channel or frequency band. This allows the analog output, TRANSMITTED CARRIER, and the analog input, RECEIVED CARRIER, to be connected for local analog loopback. Alternatively the digital data signals, TD and RD or BTD and BRD, can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back.

When a loopback mode is selected, the state machine sequences are altered slightly. First, auto-answer is disabled. Second, if a half duplex loopback mode is selected (202 or V.23), the local CARRIER DETECT/$\overline{BCD}$ is not forced OFF when $\overline{RTS}$/$\overline{BRTS}$ is asserted.

The 202 and V.23 main loopback modes allow use in a 4-wire configuration at 1200 bps.

EF79'7a MODEM

87D 08632 DT-75-33-05

Figure 7(a). Transmit Main Channel State Diagram

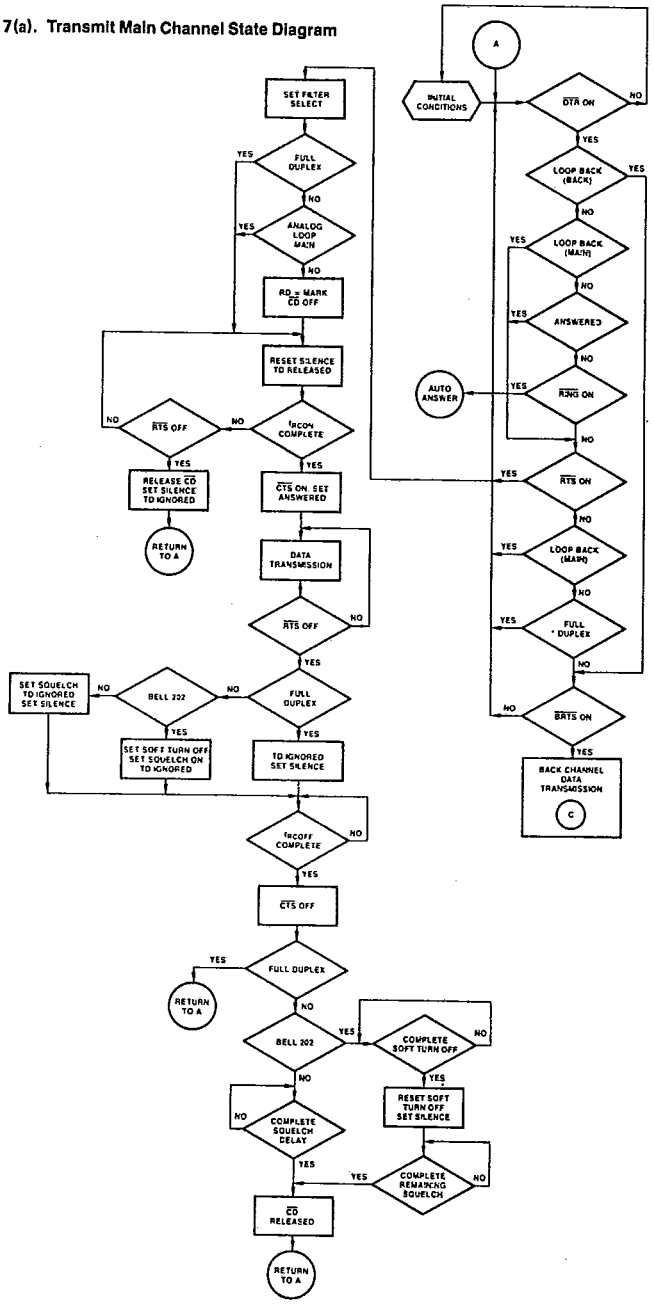


Figure 7(b). Transmit Back Channel State Diagram

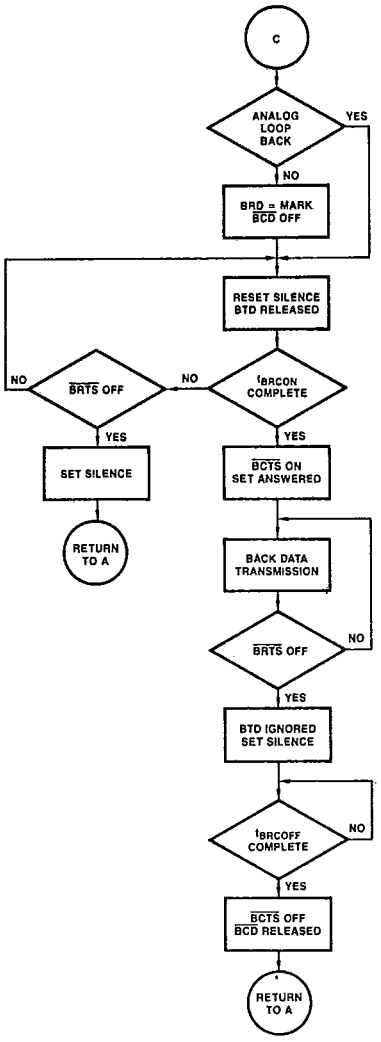


Figure 7(c). Auto Answer State Diagram

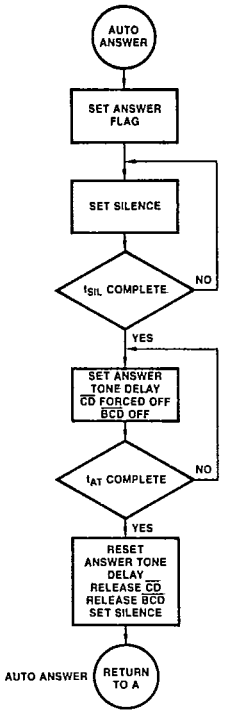
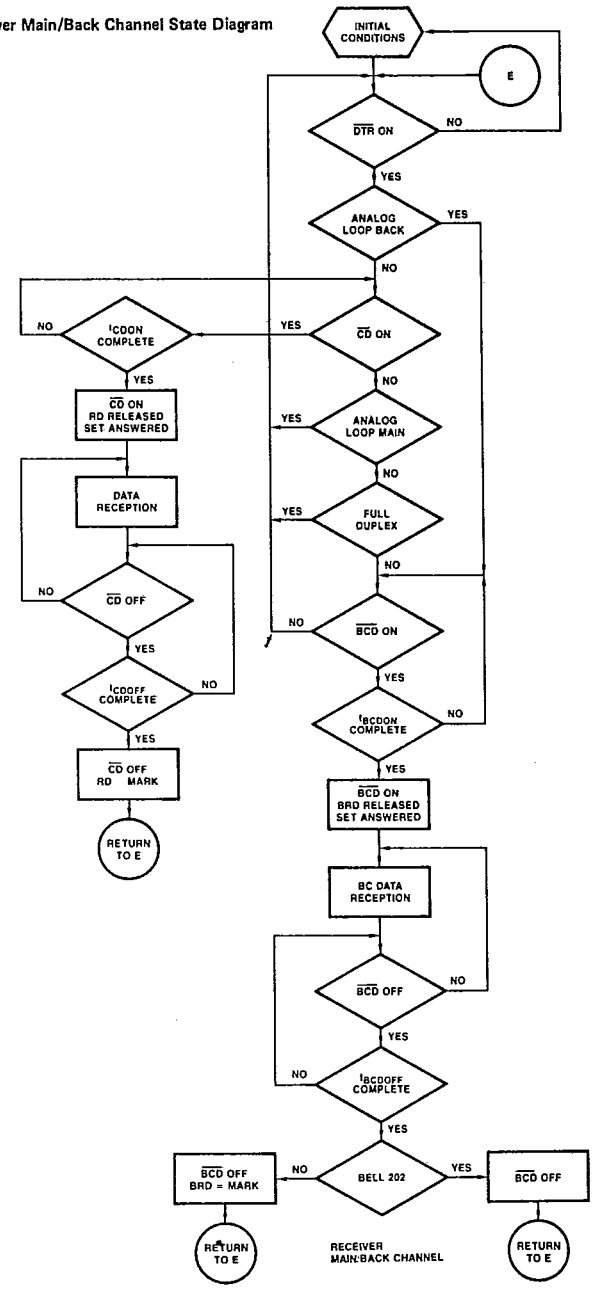


Figure 8. Receiver Main/Back Channel State Diagram



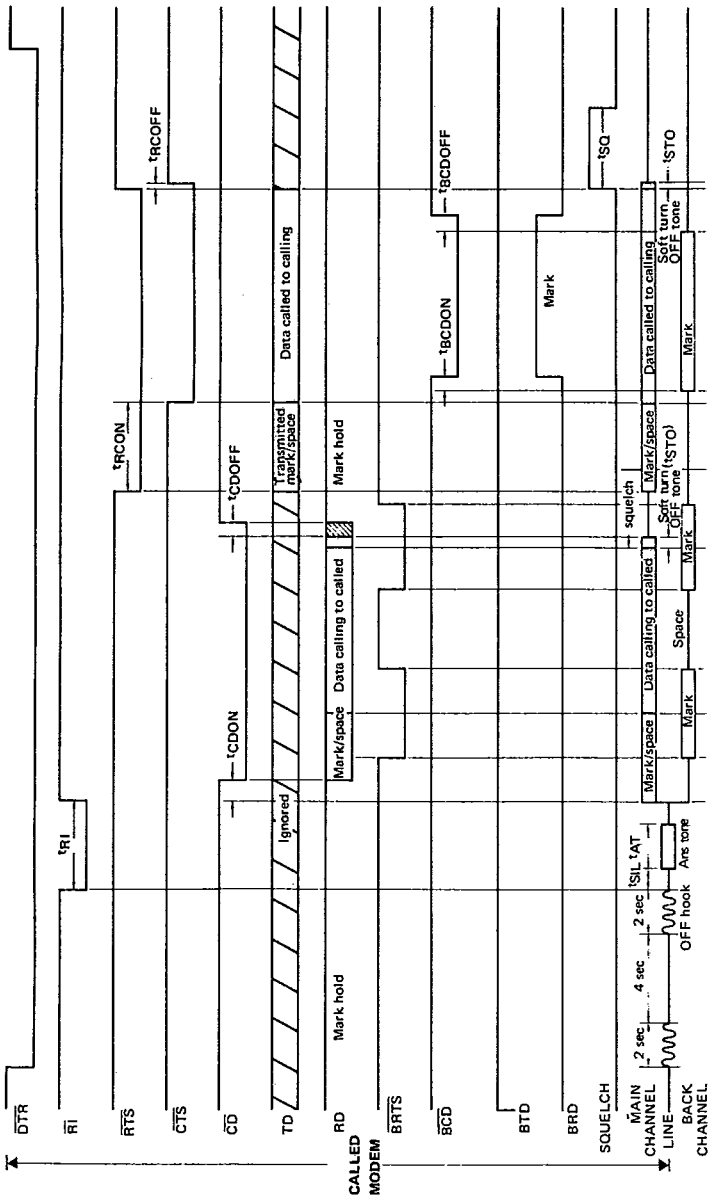


Figure 9. BELL 202 Handshake Timing

87D 08636 D T-75-33-05

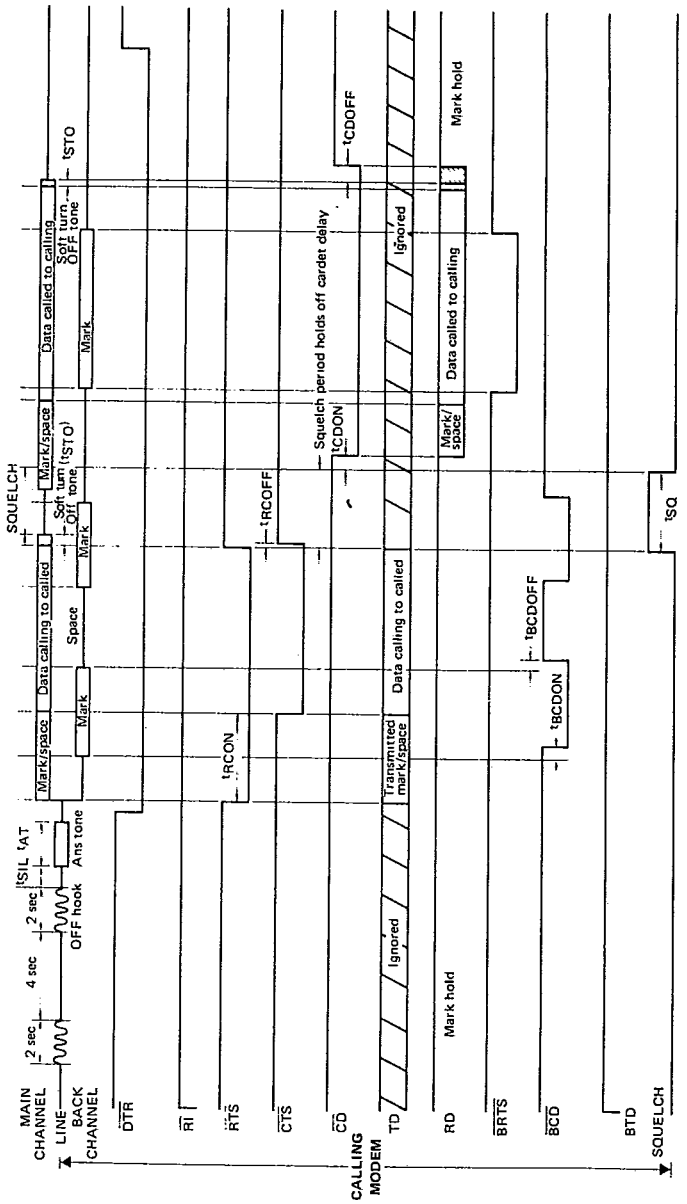


Figure 9. BELL 202 Handshake Timing (continued)

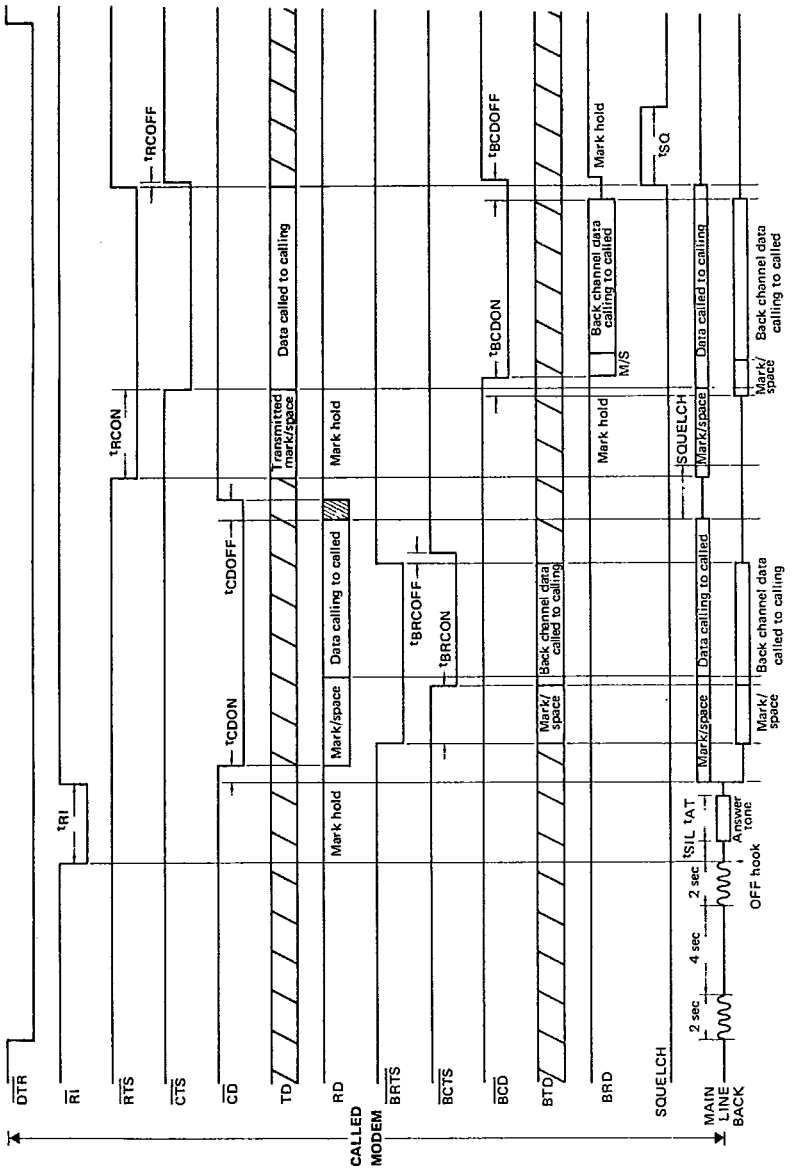


Figure 10. CCITT V.23 Handshake Timing

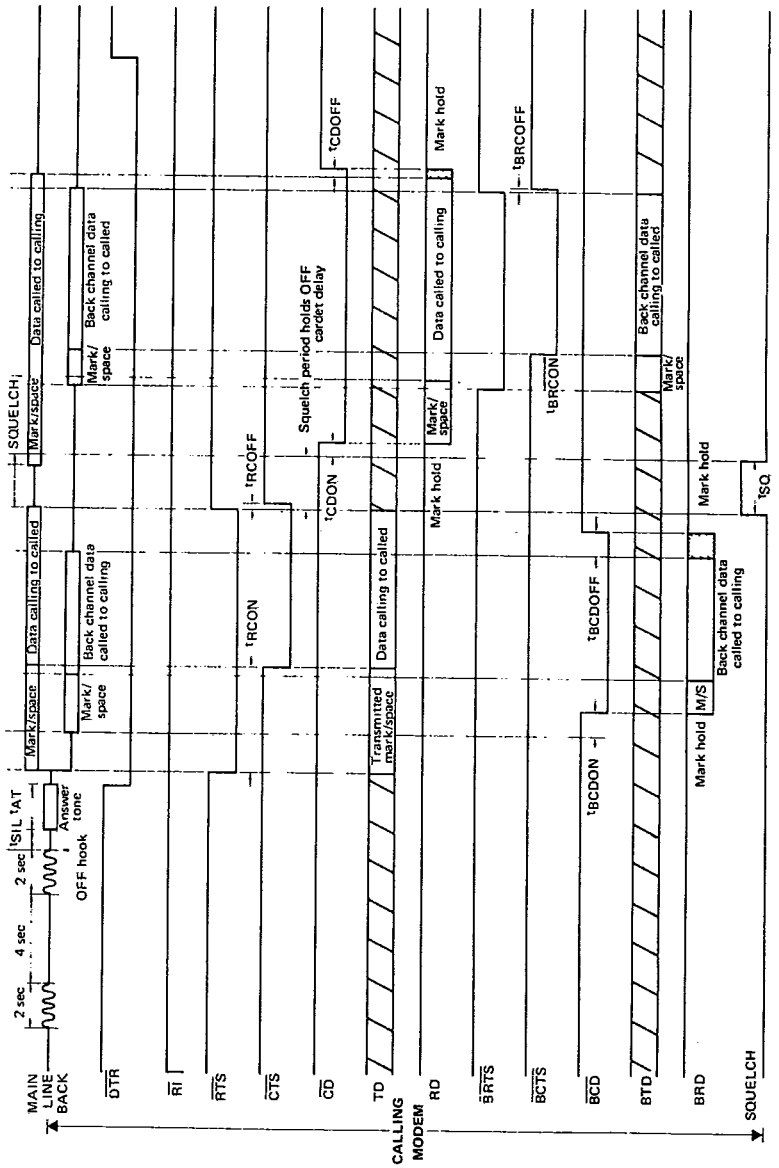
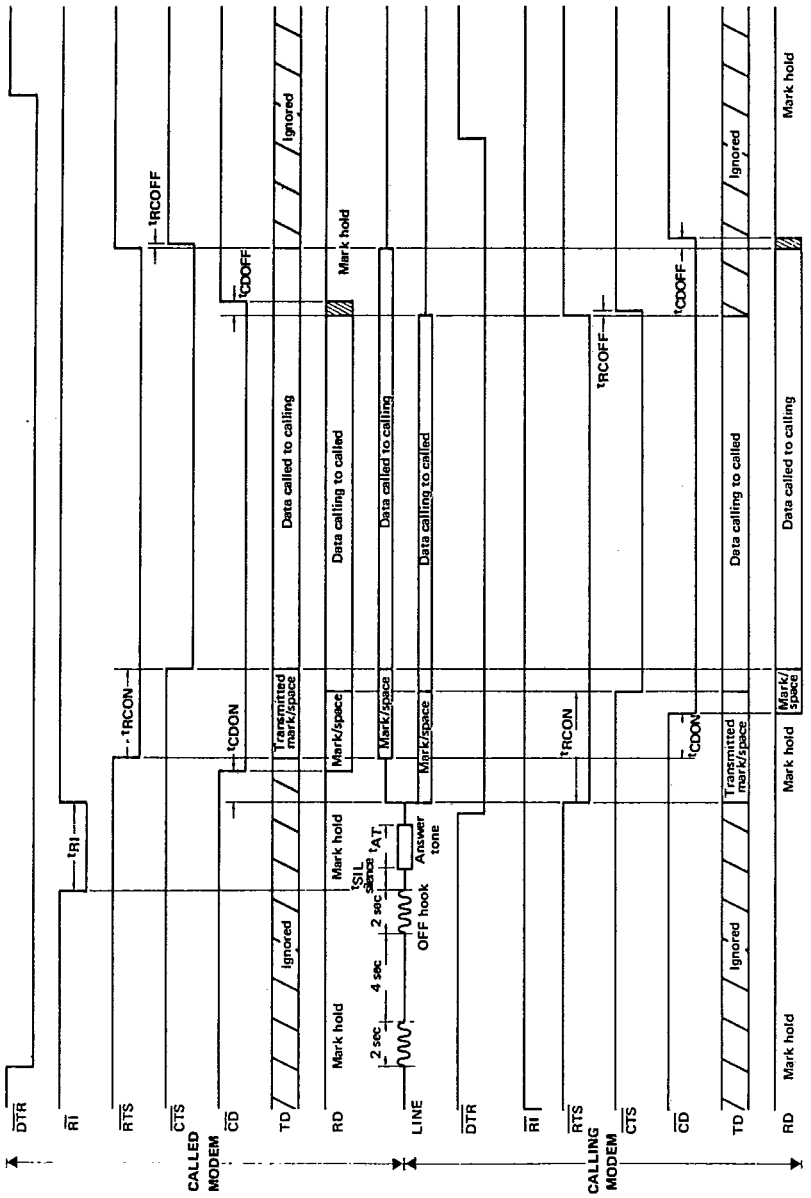


Figure 10. CCITT V.23 Handshake Timing (continued)

87D 08639 D T-75-33-05

Figure 11. BELL 103/CCITT V.21 Handshake Timing



CLOCK GENERATION

Master timing of the modem is provided by either a crystal connected to the $XTAL_1$ and $XTAL_2$ inputs or an external clock applied to the $XTAL_1$ input.

Crystal

When a crystal is used it should be connected as shown in Figure 12. The crystal should be a parallel resonance type, and its value must be 2.4576MHz ±.01%. A list of crystal suppliers is shown below.

External Clock

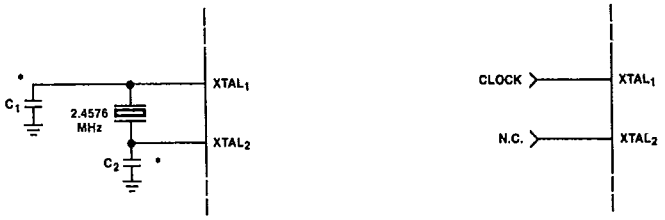
This clock signal could be derived from one of several crystal-driven baud rate generators. It should be connected to the $XTAL_1$ input and the $XTAL_2$ input must be left floating. The timing parameters required of this clock are shown in Figure 12 and the values are listed in Table 4.

Figure 12. Clock Generation

Crystal Information (f_C = 2.4576MHz)

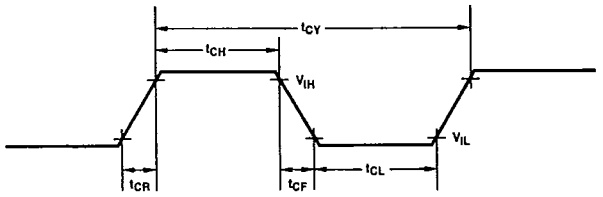
Manufacturer	P/N	C_1	C_2
M-Tron	MP-2	20pF	20pF
Monitor Products	MM-33	20pF	20pF

Note: Rise time of V_{CC} must be greater than 5msec to insure proper crystal oscillator start-up.



*Capacitors values vary with different crystal manufacturers.

(a)



(b)

TABLE 4.
CLOCK PARAMETERS

Symbol	Parameters	Min	Typ	Max	Units
t_{CY}	Clock Period	406.86	406.9	406.94	ns
t_{CH}	Clock High Time	165			ns
t_{CL}	Clock Low Time	165			ns
t_{CR}	Clock Rise Time			20	ns
t_{CF}	Clock Fall Time			20	ns

87D 08641 D T-75-33-05

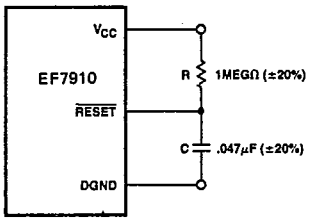
POWER ON RESET

The reset circuit operates in either of two modes.

Automatic Reset

In this mode an internal reset sequence is automatically entered when power is applied to the device. One resistor and one capacitor must be connected externally as shown in Figure 13. Values shown will work with most power supplies. Power supply (V_{CC}) rise time should be less than one half the RC time constant.

Figure 13. Automatic Reset

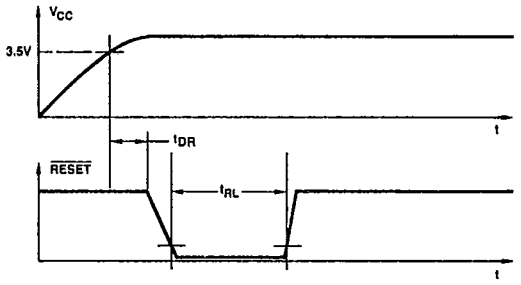


External Reset

In this mode the device may be forced into the reset sequence by application of an active LOW pulse applied to the $\overline{RESET}$ input. The reset must not be applied until the V_{CC} supply has reached at least 3.5 V. Timing is diagrammed in Figure 14.

Figure 14. External Reset

TIMING DIAGRAMS



t_{DR} = delay from the time V_{CC} reaches 3.5V and the falling edge of $\overline{RESET}$ signal (>1μs)
t_{RL} = $\overline{RESET}$ LOW duration time (>t_{MCK} = 406ns)

NOMINAL PERFORMANCE SPECIFICATIONS
TRANSMITTER (All Modem Types)

Input Data Format: Serial, asynchronous, standard TTL levels
Modulation Technique:
Binary, phase-coherent Frequency Shift Keying (FSK)
TC Output Level: −3dBm into 600Ω
Frequency Accuracy:
±0.4Hz all modems except Bell 202 (mark)
+1.0Hz Bell 202 (mark)
Harmonics: −45dB from fundamental for single tones

Delay uncertainty for TD logic input change to TC frequency change: ≤8.3μs

Out-of-band energy : See Figure 15

RECEIVER

Output Data Format: Serial, asynchronous, TTL levels
Demodulation Technique: Differential FM Detection
Sensitivity at Receiver Input: 0dBm to −48dBm
Frequency Deviation Tolerance: ±16Hz
Carrier Detect Threshold:

ON	>−43dBm ±1dB
OFF	<−48dBm ±1dB

TEST MEASUREMENT SETUP

EF7910 performance is characterized using the test equipment setup shown in Figure 16. The HP1645A data error analyzer is used to generate 511-bit pseudo random binary sequences (PRBS) at D_{OUT} for testing the modem. The 1645A also receives and analyzes the 511-bit digital pattern at D_{IN} after it has progressed around the test loop. A reference transmitter converts the digital sequence generated by the HP1645A into an FSK signal. The FSK signal is typically adjusted to different levels from −12 to −45dBm. The level-adjusted FSK signal or incident signal then passes through three pieces of equipment which comprise the telephone line simulator. The Wandel and Golterman TLN-1 and DLZ-4 simulate amplitude and group delay characteristics typical of a wide variety of phone lines. Line perturbations, such as amplitude hits and phase hits, may be injected by the Bradley 2A/2B.

The summing amplifier which drives the modem under test has three inputs. One of these inputs is the incident FSK signal which has been passed through a simulated phone line. The second input is from an optionally filtered noise source in order to simulate noise conditions which may be encountered on phone lines. The third input is from the transmitter of the EF7910 under test. This third input simulates the adjacent channel signal seen at the input of the EF7910 receiver due to the duplexer used on 2-wire lines. If 4-wire testing is being performed, the adjacent channel would not normally be included.

The HP3551A or HP3552A Transmission Test Set is used for measuring various levels which the modem under test is to receive. The levels of each of the three inputs to the summing amplifier should be measured independently of the other two inputs. For instance, the incident signal level should be measured by the transmission test set with no adjacent channel or noise present. The dashed line from the noise generator shows that the noise may or may not be measured at the output of the noise generator, depending on whether or not an optional filter is used, or on the characteristics of the filter.

Figure 15. Out-of-Band Transmitter Energy

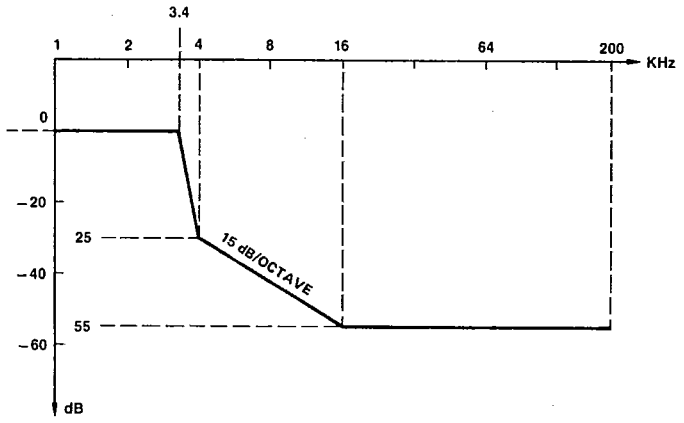
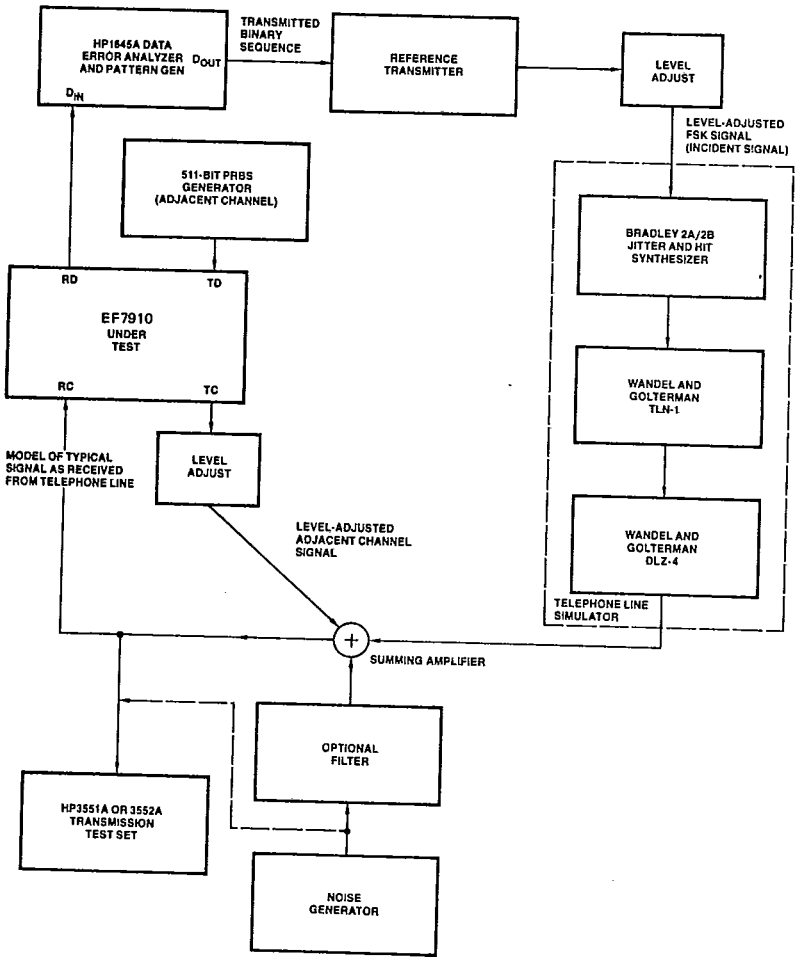


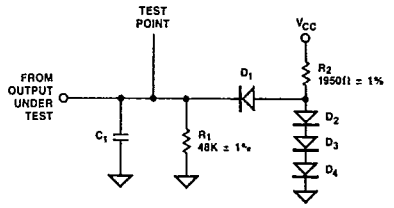
Figure 16. BER and Distortion Measurement Test Setup

87D 08643 D T-75-33-05



87D 08644 D T-75-33-05

STANDARD LOAD CIRCUIT



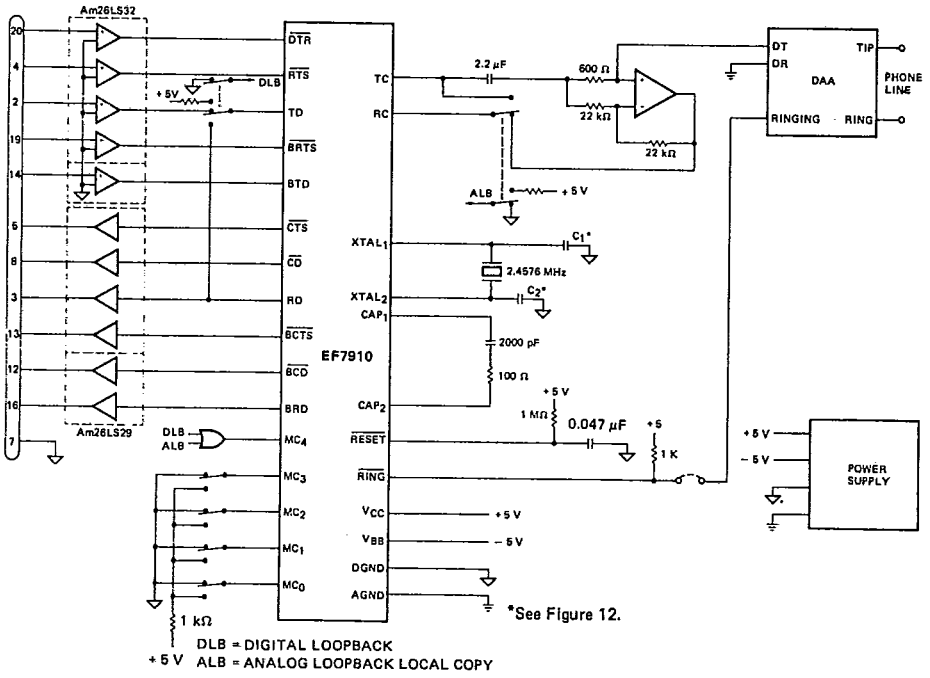
Notes: 1. C_1 = 50pF including stray and wiring capacitance
2. All diodes are 1N3064 or equivalent
3. All resistors are 1/8 watt
4. V_{CC} = 5 volts ±1%

APPLICATIONS

Figure 18 depicts a stand-alone EF7910 configuration. An op amp and three resistors provide a duplexor function to put the transmitter output onto the line while receiving adjacent channel data from the line. Connection to the line is via a Data Access Arrangement (DAA). Note the lack of external analog filters. The TTL handshake signals may be level converted to RS-232, RS-422, or V.24 using appropriate devices. Mode control lines are hardwired or connected to switches.

Figure 19 depicts an application of the EF7910 with the THOMSON SEMICONDUCTEURS EF6805CT microcomputer. The duplexor/line interface is identical to the above configuration. However, the handshake signals interface directly with the UART included inside the EF6805CT. The mode control lines might also be controlled by the MCU while keeping the address and data bus of the EF6805CT available for customer applications. The main features of the EF6805CT are given at the end of this data sheet.

Figure 18. Stand-Alone EF7910 Application



87D 08645 D T-75-33-05

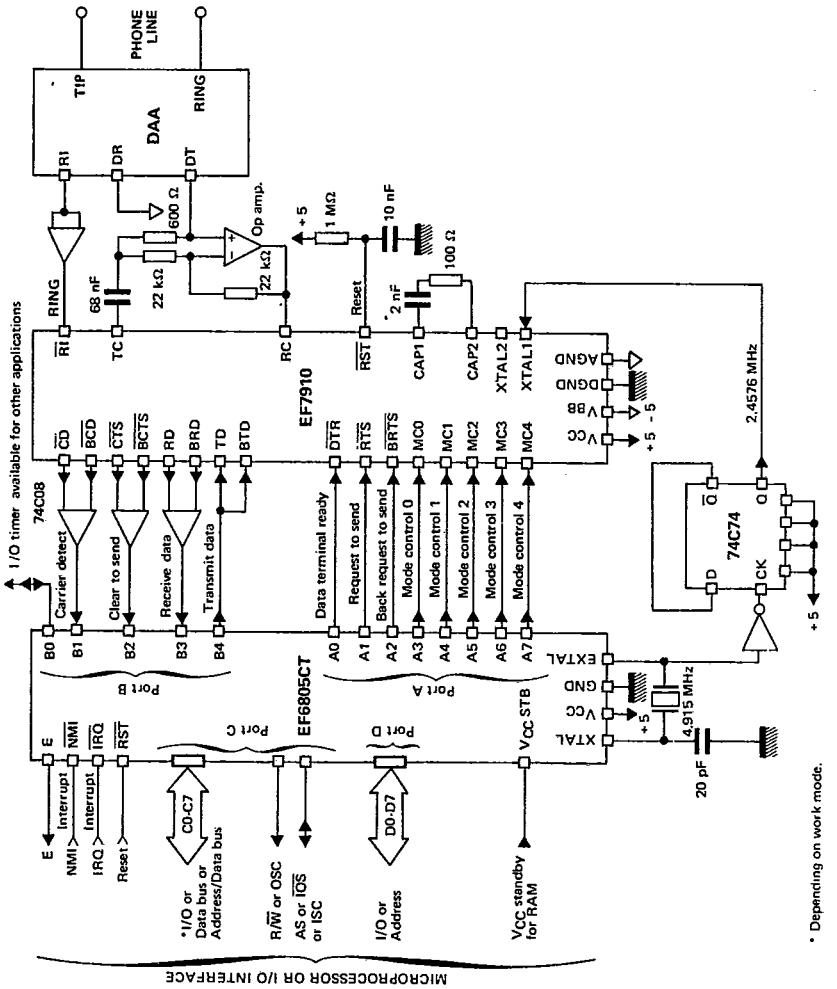


Figure 19. Microprocessor typical application

87D 08646 D T-75-33-05

MAXIMUM RATINGS

Rating	Value	Unit
Storage temperature	-65 to +125	°C
Ambient temperature under bias	0 to +70	°C
V_{CC} with respect to V_{DGND}	+6 / -0.4	V
V_{BB} with respect to V_{DGND}	-6 /+0.4	V
All signal voltages with respect to V_{DGND}	±5	V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL DC CHARACTERISTICS over operating range, referred to V_{DGND}
$0°C \leq T_A \leq +70°C$, $V_{CC} = +5.0\ V \pm 5\ \%$, $V_{BB} = -5.0\ V \pm 5\ \%$, $V_{AGND} = 0\ V \pm 50\ mV$, $V_{DGND} = 0\ V$
Digital inputs : TD, $\overline{RTS}$, MC_0-MC_4, $\overline{DTR}$, $\overline{RING}$, BTD, $\overline{BRTS}$
Digital outputs : RD, $\overline{CTS}$, $\overline{CD}$, BRD, $\overline{BCTS}$, $\overline{BCD}$

Characteristic	Symbol	Min	Typ	Max	Unit
Output HIGH voltage ($I_{OH} = -60\ \mu A$, $C_{LD} = 50\ pF$)	V_{OH}	2.4	–	–	V
Output LOW voltage ($I_{OL} = +2\ mA$, $C_{LD} = 50\ pF$)	V_{OL}	–	–	0.4	V
Input HIGH voltage	V_{IH}	2.0	–	V_{CC}	V
Input LOW voltage	V_{IL}	-0.5	–	+0.8	V
External clock input HIGH ($XTAL_1$)	V_{IHC}	3.8	–	V_{CC}	V
External clock input LOW ($XTAL_1$)	V_{ILC}	-0.5	–	0.8	V
External reset input HIGH ($\overline{RESET}$)	V_{IHR}	3.8	–	V_{CC}	V
External reset input LOW ($\overline{RESET}$)	V_{ILR}	-0.5	–	0.8	V
Digital input leakage current ($0 \leq V_{IN} \leq V_{CC}$)	I_{IL}	-10	–	+10	µA
V_{CC} supply current	I_{CC}	–	–	125	mA
V_{BB} supply current	I_{BB}	–	–	25	mA
Output capacitance ($f_C = 1.0$ MHz)	C_{OUT}	–	5	15	pF
Input capacitance ($f_C = 1.0$ MHz)	C_{IN}	–	5	15	pF
ANALOG INPUT (RC) :					
Input resistance ($-1.6\ V < V_{RC} < +1.6\ V$)	R_{IN}	50	–	–	kΩ
Operating input signal	V_{RC}	-1.6	–	+1.6	V
Allowed DC input offset (REF V_{AGND})	V_{RCOS}	-30	–	+30	mV
ANALOG OUTPUT (TC) :					
Output voltage ($R_L = 600\ \Omega$)	V_{TC}	-1.1	–	+1.1	V
Output DC offset	V_{TCOS}	–	±200	–	mV

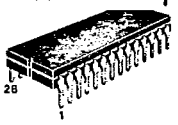
ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP.RANGE	QUALITY LEVEL			
	J	L*	Std**	D	G	B
EF7910	●	●	●	Available on request		
Example : EF7910JL						

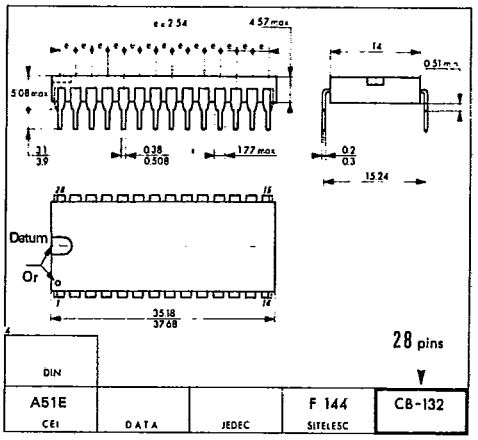
J : Cerdip, L* : 0° to +70°C, * : may be omitted.
Quality levels in accordance with NFC 96883. ** : No end-suffix for standard level products.

CASE CB-132

87D 08647 D T-75-33-05



J SUFFIX
CERDIP PACKAGE

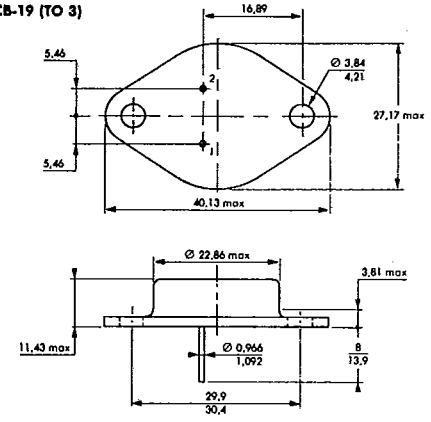


This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

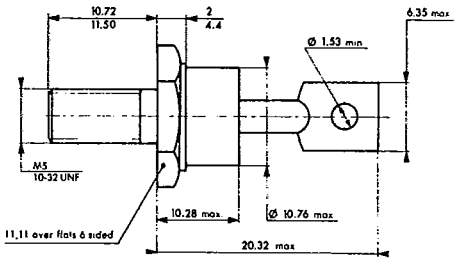
87D 09185 D T-75-11-33

case outlines

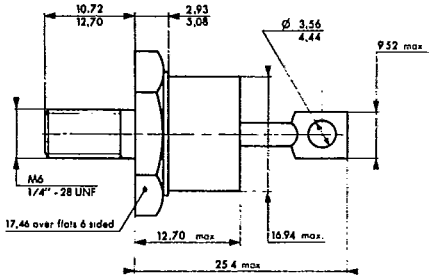
CB-19 (TO 3)



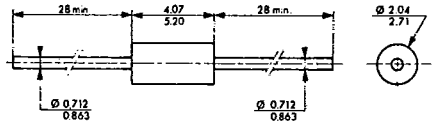
CB-33 (DO 4)



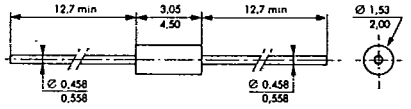
CB-34 (DO 5)



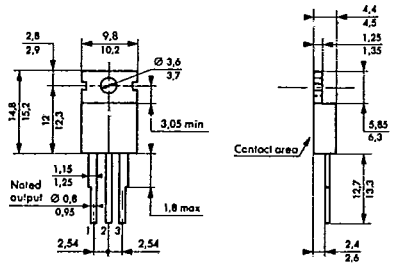
CB-101 (DO 41)



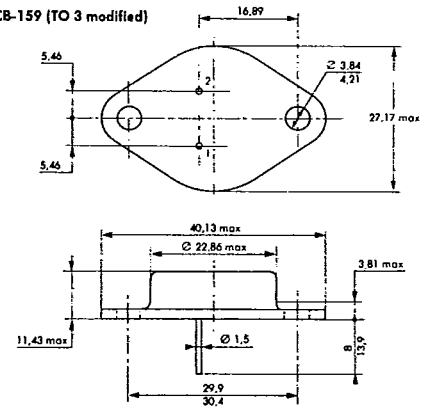
CB-102 (DO 35)



CB-117 (TO 220 AB) for power transistors



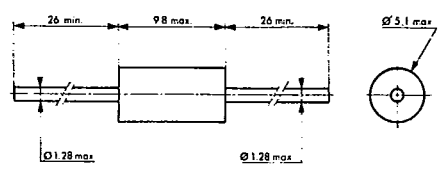
CB-159 (TO 3 modified)



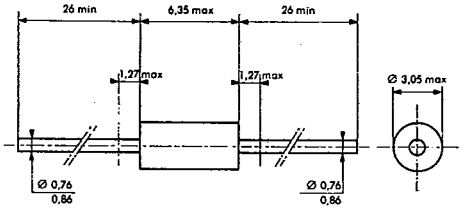
87D 09186 D T-75-11-33

case outlines

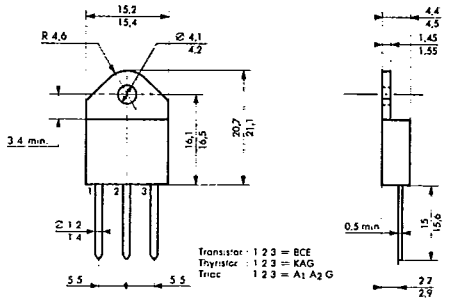
CB-197 (DO 27 A)



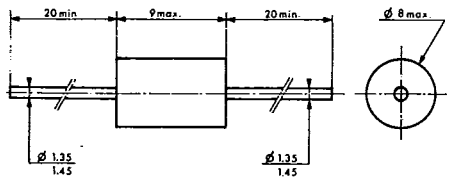
CB-210 (F 126)



CB-244 (TO 218 - TOP 3)



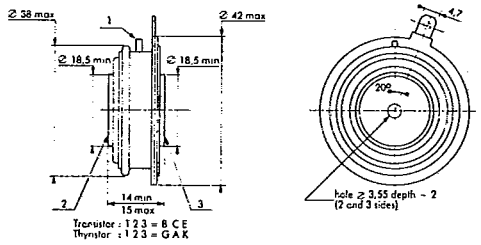
CB-257 (AG)



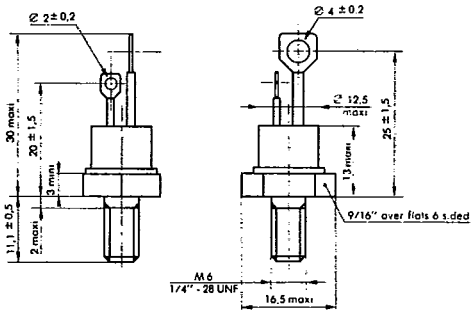
CB-263 (MU 86)

Transistor :
Base lead = Braid 2 mm²
Approx. length = 120 mm

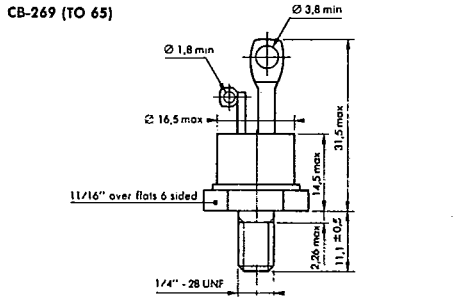
Thyristor :
Gate lead : white
Cathode lead : red
Approx. length = 200 mm



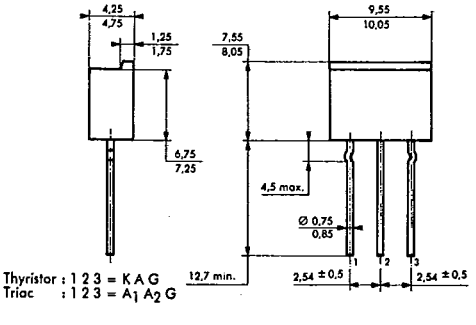
CB-267 (TO 48)



CB-269 (TO 65)



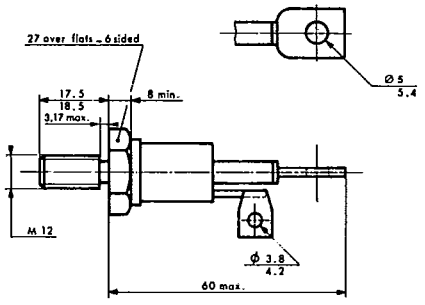
CB-274 (TL)



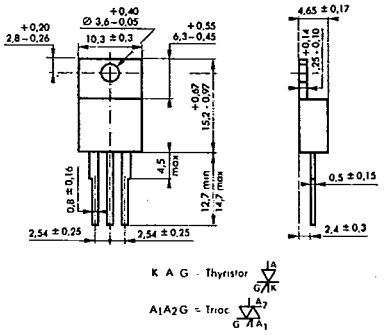
87D 09187 D T-75-11-33

case outlines

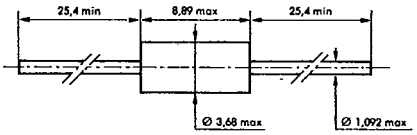
CB-338 (TO 83)



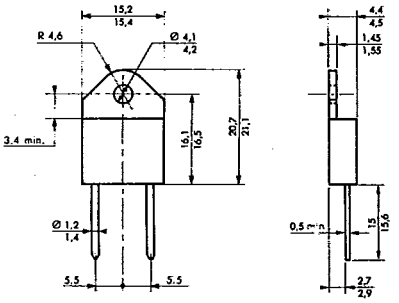
CB-415 (TO 220 AB) for thyristors and triacs



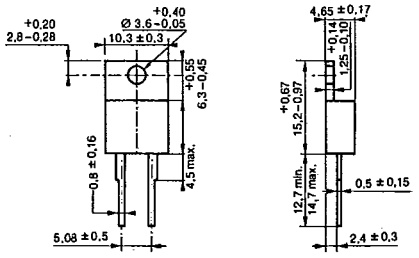
CB-417



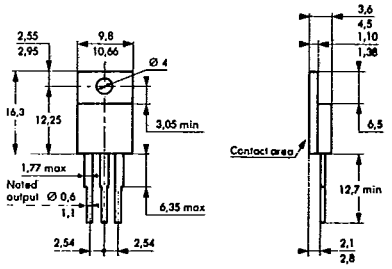
CB-425 (DOP 3)



CB-426 (DO 220 AB) for insulated types



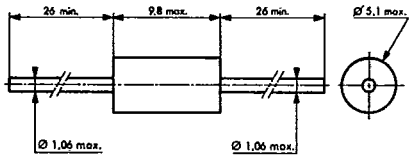
CB-428 (TO 220 AB) for duo diodes



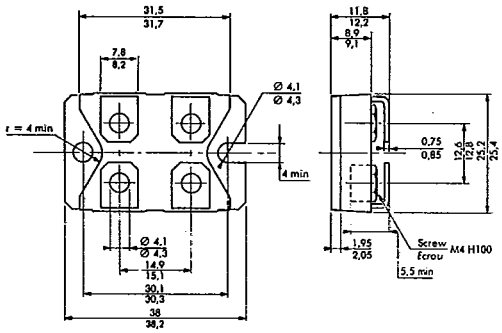
87D 09188 D T-75-11-33

case outlines

CB-429

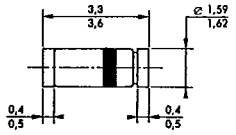


CB-452 (ISOTOP)

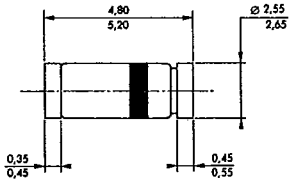


Pin B2 may be omitted for a transistor.

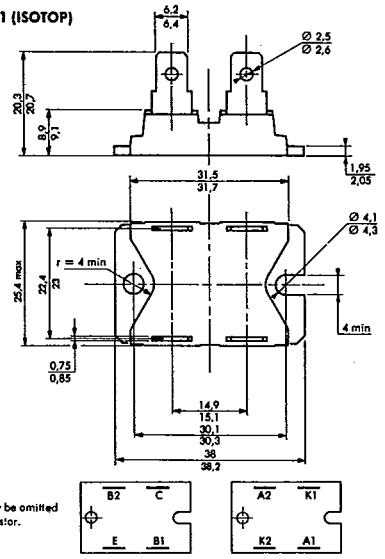
CB-465 (MINIMELF)



CB-466 (MELF)

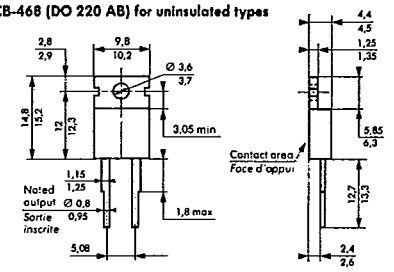


CB-451 (ISOTOP)

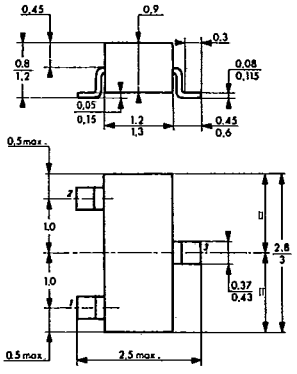


Pin B2 may be omitted for a transistor.

CB-468 (DO 220 AB) for uninsulated types



CB-474



Dimensions in millimeters