Power MOSFET

40 V, 10 m Ω , 34 A, Dual N–Channel Logic Level, Dual SO–8FL

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5853NLWF Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	T _{mb} = 25°C	I _D	34	Α
		T _{mb} = 100°C		24	
Power Dissipation R _{ΨJ-mb} (Notes 1, 2, 3)		T _{mb} = 25°C	P_{D}	24	W
		T _{mb} = 100°C		12	
Continuous Drain Current R _{0.IA} (Notes 1, 3		T _A = 25°C	I _D	12	Α
(8.4)	Steady State	T _A = 100°C		8.5	
Power Dissipation R _{0JA} (Notes 1 & 3)		T _A = 25°C	P_{D}	3.0	W
		T _A = 100°C		1.5	
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	165	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	34	Α
Single Pulse Drain-to-Source Avalanche Energy (T_J = 25°C, V_{GS} = 10 V, $I_{L(pk)}$ = 28.3 A, L = 0.1 mH, R_G = 25 Ω)			E _{AS}	40	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) - Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	6.2	
Junction-to-Ambient - Steady State (Note 3)		51	°C/W
Junction-to-Ambient - Steady State (min foot-print)	$R_{\theta JA}$	162	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

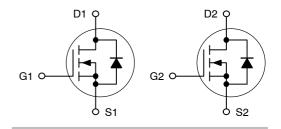


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
40 V	10 mΩ @ 10 V	34 A
	15 mΩ @ 4.5 V	0 4 A

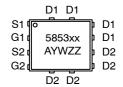
Dual N-Channel





CASE 506BT

MARKING DIAGRAM



5853NL = Specific Device Code

for NVMFD5853NL

5853LW = Specific Device Code

for NVMFD5853NLWF

A = Assembly Location

Y = Year W = Work Week

ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]		
NVMFD5853NLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel		
NVMFD5853NLWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condi	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		L		•	•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	do 75			37.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1.0	μΑ
		$V_{DS} = 40 \text{ V}$	T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	= 250 μA	1.4		2.4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.9		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$			8.4	10	mΩ
					12.7	15	1
Forward Transconductance	9 _{FS}	V _{DS} = 5 V, I _D = 5 A			22		S
CHARGES AND CAPACITANCES							
Input Capacitance	C _{iss}				1100		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V, f = 1.0 MH	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		152		
Reverse Transfer Capacitance	C _{rss}				100		
Total Gate Charge	Q _{G(TOT)}				12.8		nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{D}$	_S = 32 V,		1.0		1
Gate-to-Source Charge	Q_{GS}	I _D = 15 A			3.7		1
Gate-to-Drain Charge	Q_{GD}		-		7.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 15 A			23		nC
SWITCHING CHARACTERISTICS (No	ote 6)		- -		-	·=	-
Turn-On Delay Time	t _{d(on)}				10		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{D}$	_S = 20 V,		53		
Turn-Off Delay Time	t _{d(off)}	$I_D = 15 \text{ A}, R_G$	= 2.5 Ω		17		
Fall Time	t _f		-		30		1
Turn-On Delay Time	t _{d(on)}				9.0		ns
Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DS}$	_s = 20 V,		23		7
Turn-Off Delay Time	t _{d(off)}	$I_{D} = 15 \text{ A}, R_{G} = 2.5 \Omega$			22		7
Fall Time	t _f				4.3		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	rd Diode Voltage	V _{GS} = 0 V,	T _J = 25°C		0.84	1.1	V
		I _S = 20 A	T _J = 125°C		0.69		1
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } d_{IS}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 15 \text{ A}$			20		ns
Charge Time	ta				12		1
Discharge Time	t _b				8.1		1
Reverse Recovery Charge	Q _{RR}				12.1		nC

^{5.} Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

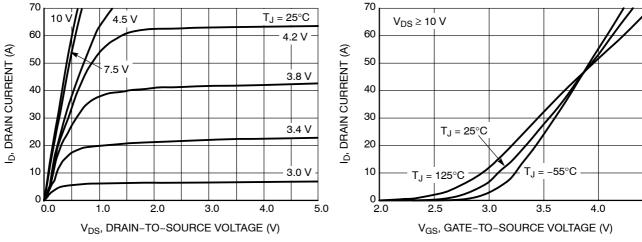


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

4.5

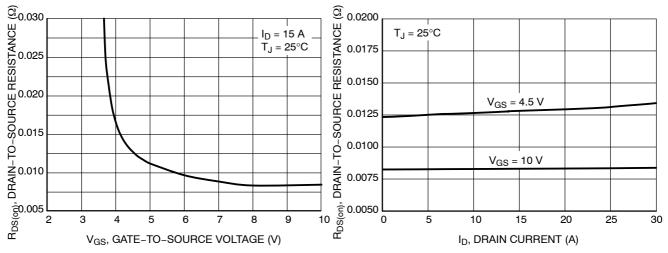


Figure 3. On-Resistance vs. V_{GS}

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

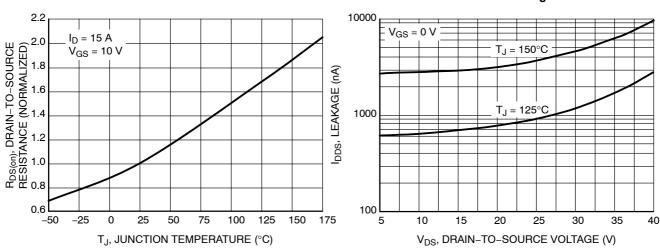


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

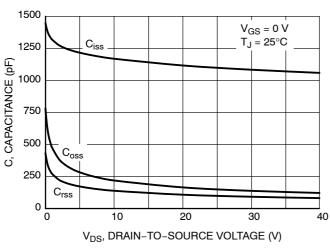


Figure 7. Capacitance Variation

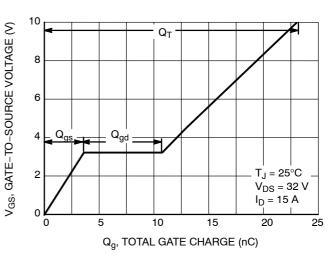


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

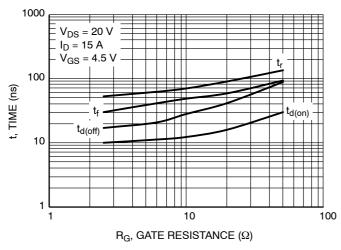


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

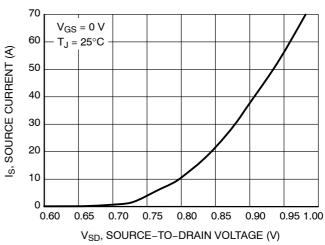


Figure 10. Diode Forward Voltage vs. Current

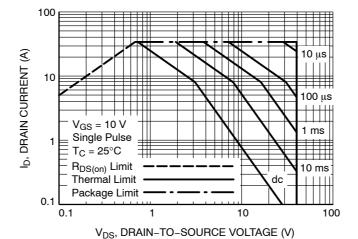


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

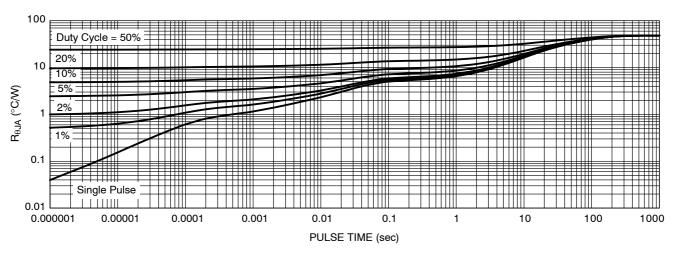
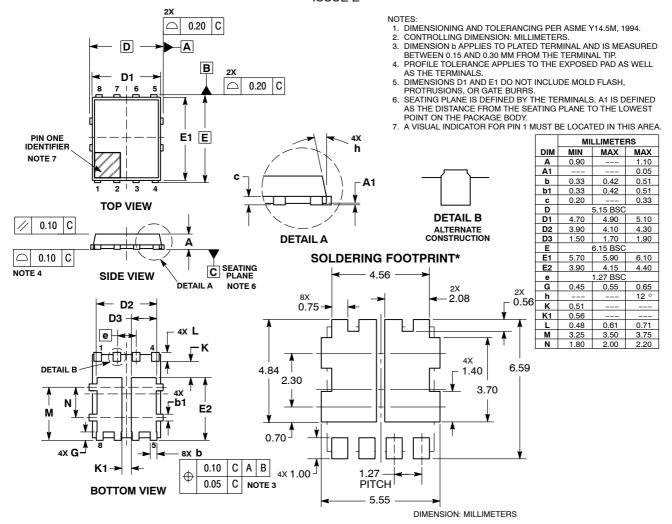


Figure 12. Thermal Response

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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