H0538A
H0539A
Serial Input
Dot Matrix LCD Driver

HUGHES
AIRCRAFT COMPANY

SEMICONDUCTOR DIVISION
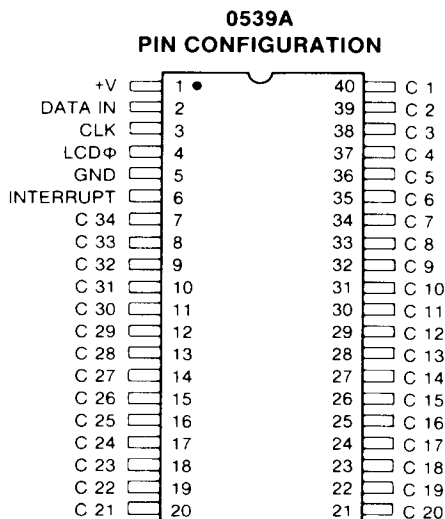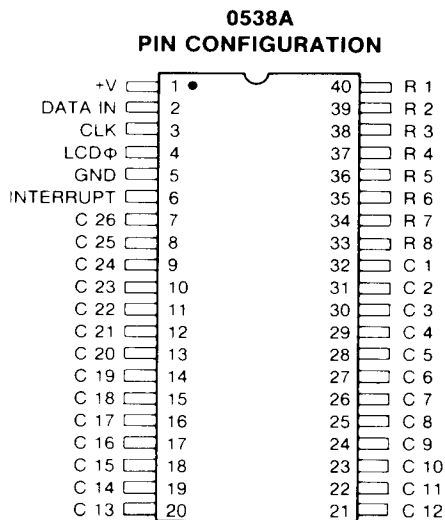Industrial Electronics Group

DESCRIPTION

Hughes 0538A and 0539A are a set of CMOS/LSI circuits that drive a dot matrix LCD display under microcomputer control. The intended display is a 5 x 7 or 5 x 8 alphanumeric dot matrix with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this set of circuits.

The 0538A is organized as 8 rows x 26 columns, and thus can handle up to five characters by itself. The 0539A is organized as 0 rows x 34 columns and is used in addition to the 0538A when more than 26 columns are required. Data is serially input to maximize the number of output pins and minimize the number of control pins. This circuit set drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0538A and 0539A are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  Wide supply voltage range
  Low power operation
  High noise immunity
  Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
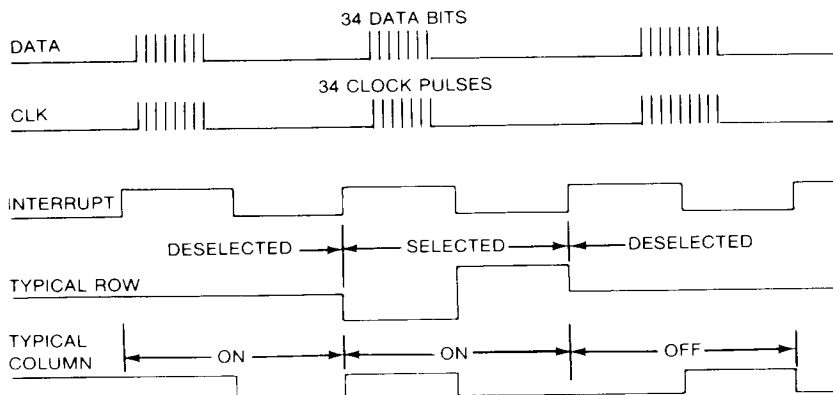- Interrupt output to request data from microcomputer

0538A
PIN CONFIGURATION

+V	1 ●		40	R 1
DATA IN	2		39	R 2
CLK	3		38	R 3
LCDΦ	4		37	R 4
GND	5		36	R 5
INTERRUPT	6		35	R 6
C 26	7		34	R 7
C 25	8		33	R 8
C 24	9		32	C 1
C 23	10		31	C 2
C 22	11		30	C 3
C 21	12		29	C 4
C 20	13		28	C 5
C 19	14		27	C 6
C 18	15		26	C 7
C 17	16		25	C 8
C 16	17		24	C 9
C 15	18		23	C 10
C 14	19		22	C 11
C 13	20		21	C 12

0539A
PIN CONFIGURATION

+V	1 ●		40	C 1
DATA IN	2		39	C 2
CLK	3		38	C 3
LCDΦ	4		37	C 4
GND	5		36	C 5
INTERRUPT	6		35	C 6
C 34	7		34	C 7
C 33	8		33	C 8
C 32	9		32	C 9
C 31	10		31	C 10
C 30	11		30	C 11
C 29	12		29	C 12
C 28	13		28	C 13
C 27	14		27	C 14
C 26	15		26	C 15
C 25	16		25	C 16
C 24	17		24	C 17
C 23	18		23	C 18
C 22	19		22	C 19
C 21	20		21	C 20

ABSOLUTE MAXIMUM RATINGS

V_{DD} . . . . — .3 to + 15 volts
Inputs . . . . + V_{DD} — 17 to + V_{DD} + .3 volts
Power Dissipation . . . . 250 mW
Operating Temperature
    Ceramic Package . . . . — 55 to + 125°C
    Plastic Package . . . . — 40 to + 85°C
Storage Temperature . . . . — 65 to + 125°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = +25° and V_{DD} = 5V unless otherwise noted.
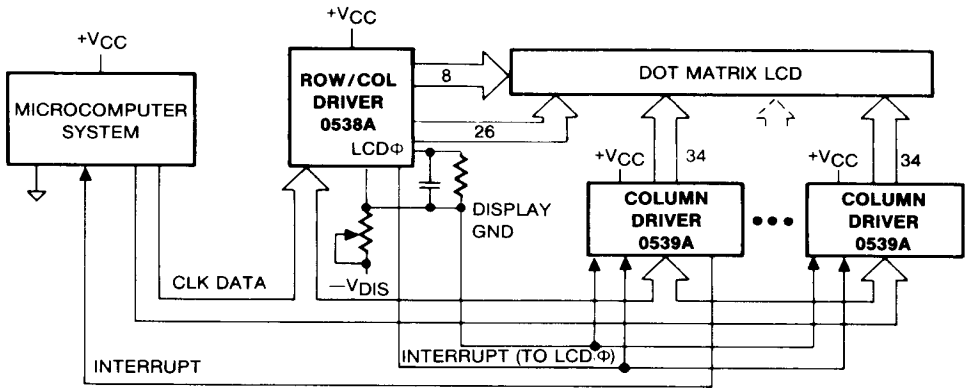
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current	I_{DD}			750	μA
Input High Level	V_{IH}		.8 V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}—15	.5V_{DD}	V
Input Leakage	I_L			5	A
Input Capacitance	C_I			5	f
Row and Column Output Impedance	R_{ON}	I_L = 10 μA		40	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100 μA		3	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ to Interrupt Output Delay	t_D		600		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ
DC Offset Voltage, Any Display Element	V_{OFF}			15	mV
Row Output High	V_{OH}	Typical	V_{DD}		V
Row Output Low	V_{OL}	Typical	0		V
Row Output Unselected	V_{OM}	Typical	.5V_{DD}		V
Column Output High	V_{OH}	Typical	.68V_{DD}		V
Column Output Low	V_{OL}	Typical	.32V_{DD}		V

TYPICAL WAVEFORMS

CLK

DATA IN → | 34 BIT STATIC SHIFT REGISTER |

+V$_{DD}$ →
GND →

LOAD → | 34 LATCHES |

LCDΦ → | LCD AC CKT |

| 8 ROW DRIVERS | | 26 COLUMN DRIVERS |

→ INTERRUPT
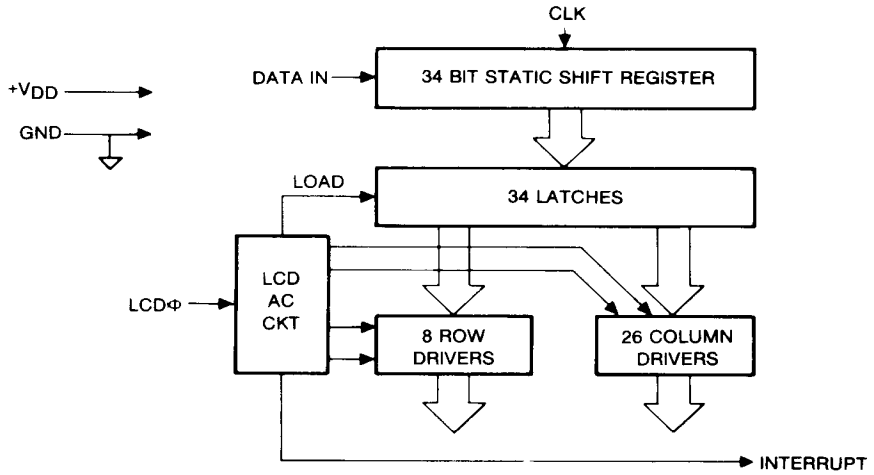
TYPICAL SYSTEM BLOCK DIAGRAM

+V$_{CC}$

+V$_{CC}$

| MICROCOMPUTER SYSTEM |

| **ROW/COL DRIVER 0538A** | 8 → | DOT MATRIX LCD |

LCDΦ 26

+V$_{CC}$ 34   +V$_{CC}$ 34

| **COLUMN DRIVER 0539A** | • • • | **COLUMN DRIVER 0539A** |

DISPLAY GND

CLK DATA

−V$_{DIS}$

INTERRUPT (TO LCD.Φ)

INTERRUPT

TIMING DIAGRAM

DATA IN   DATA VALID

t_{DS} t_{DH}

CLOCK

89
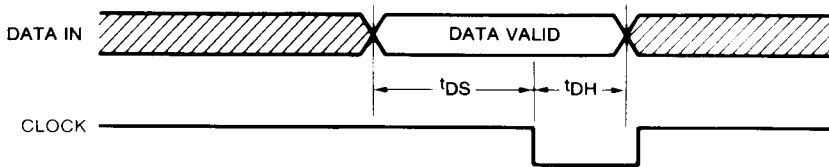
OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.

2. A logic 1 on Data In causes a segment to be visible.

3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.

4. Row waveforms are out of phase with Interrupt Output if selected and at midpoint voltage otherwise Levels are V_{DD}, 0, and $V_{DD}/2$.

5. Column waveforms are in phase with Interrupt Output if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.

6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCD input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.

7. The LCD pin can be used in two modes. If LCD is driven, the Interrupt Output will follow it. LCD will also oscillate if a resistor and capacitor are connected in parallel to ground.

The resistor value should be at least 1M Ω. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrupt Output.

8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCD of all other circuits (thus one oscillator provides frequency control for all circuits) or connect LCD of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select.

9. There are two obvious signal races to be avoided.
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.

10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.

11. Output locations correspond to a clockwise advancing shift register, thus R 1 is the last data loaded and C 30 is the first data loaded.

12. The RMS voltages this circuit delivers to individual LCD pixels depends on V_{DD} and the number of backplanes (N) used according to the following equations:

$$V_{OFF} = V_{DD} \sqrt{\frac{.0324 N + .07}{N}}$$

$$V_{ON} = V_{DD} \sqrt{\frac{.0324 N + .43}{N}}$$