élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2041C
Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- Open loop unity bandwidth—90 MHz
- Unity gain stable
- High gain—10k typ.
- High slew rate—250 V/μs
- Low offset voltage—0.5 mV typ., 2 mV max.
- Low supply current—13 mA typ., 17 mA max.
- Wide supply operation $\pm$5V to $\pm$15V
- Output voltage swing—$\pm$11V
- Power bandwidth—4 MHz
- Fast settling time
- Pin compatible with HA2541

Applications

- Pulse and video amplifiers
- Fast integrators
- Wideband filters
- High speed sample and hold circuits
- Fast, precise D/A converter output amplifier
- High speed A/D input amplifier

Ordering Information

| Part No.	Temp. Range	Package	Outline #
EL2041CN	0°C to +75°C	8-Pin P-DIP	MDP0031

General Description

The EL2041 is a unity gain stable monolithic operational amplifier with a 90 MHz open loop unity bandwidth. This unprecedented bandwidth is accomplished with a 45° phase margin and a 6.5 dB gain margin. Unlike other wideband amplifiers, the patented EL2041 operates on standard $\pm$15V supplies, swings $\pm$11V at its output, and maintains an 80 dB open loop gain into a 1k load.

In addition, the EL2041 has a 250 V/μs slew rate while drawing only 13 mA of supply current. Zener Zap techniques are used to trim the offset voltage to 2 mV maximum, making the EL2041 an excellent choice for applications requiring both speed and accuracy.

Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

Connection Diagram

Plastic DIP

Pin	Name		Pin	Name
1	BALANCE		8	BALANCE
2	−IN		7	+V$_S$
3	+IN		6	OUTPUT
4	−V$_S$		5	NC
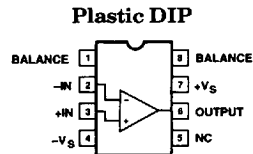
2041-3

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

Absolute Maximum Ratings $(T_A = 25°C)$

Voltage between V+ and V−		35V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage		6V	Maximum Junction Temperature	150°C
Output Current	Continuous	25 mA	Lead Temperature (Soldering, 5 seconds)	300°C
	Peak	50 mA		
Internal Power Dissipation	See Curves			
Operating Temperature Range		0°C to +75°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $V_S = \pm 15V; R_L = 1\ k\Omega$, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	+25°C		0.5	5	I	mV
		Full			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	μV/°C
I_B	Bias Current	+25°C		5	15	I	μA
		Full			20	III	μA
I_{OS}	Offset Current	+25°C		1	4	I	μA
		Full			6	III	μA
R_{IN}	Input Resistance	+25°C		20		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±8	±11		II	V
e_{IN}	Input Noise Voltage ($f = 1$ kHz, $R_G = 0\Omega$)	+25°C		10		V	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain (Notes 1, 2)	+25°C	5k	10k		I	V/V
		Full	4k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	60	80		II	dB
V_O	Output Voltage Swing	Full	±11	±12		II	V
I_O	Output Current (Note 11)	Full	±25	±50		I	mA
R_O	Output Resistance	+25°C		40		V	Ω
I_S	Supply Current	Full		13	17	II	mA
PSRR	Power Supply Rejection Ratio (Note 7)	Full	60	80		II	dB

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AC Electrical Characteristics $V_S = \pm 15V; R_L = 1\,k\Omega$, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
f_u	Open Loop Unity Bandwidth (Notes 4, 10)	$+25°C$		90		V	MHz
FPBW	Full Power Bandwidth (Notes 1, 5)	$+25°C$	2.8	4		I	MHz
t_r	Rise Time (Note 6)	$+25°C$		4		V	ns
OS	Overshoot (Note 6)	$+25°C$		10		V	%
SR	Slew Rate (Note 6)	$+25°C$	180	250		I	$V/\mu s$
t_s	Settling Time (Notes 8, 9, 10) 10V Step to 0.05%	$+25°C$		90		V	ns

Note 1: $V_O = \pm 10V$.
Note 2: $R_L = 1\,k\Omega$.
Note 3: Two tests are performed. $V_{CM} = 0V$ to $+8V$ and $V_{CM} = 0V$ to $-8V$.
Note 4: $V_O = 90$ mV.
Note 5: Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \dfrac{\text{Slew Rate}}{2\pi\,V\text{peak}}$.
Note 6: Refer to Test Circuits section of data sheet.
Note 7: Two tests are performed. $V+ = +15V$, and $V-$ is changed from $-7V$ to $-15V$. $V- = -15V$, and $V+$ changed from $+7$ to $+15V$.
Note 8: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 9: $A_V = +1$, $R_L = 1k$.
Note 10: 200Ω, 20 pF output snubber, see application section.
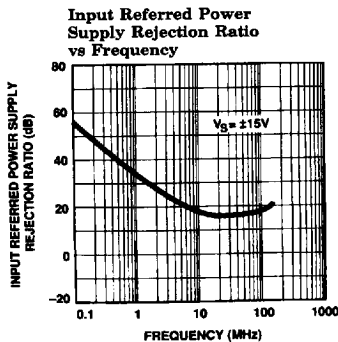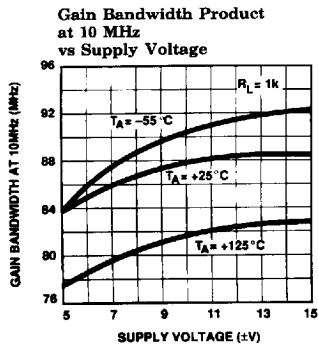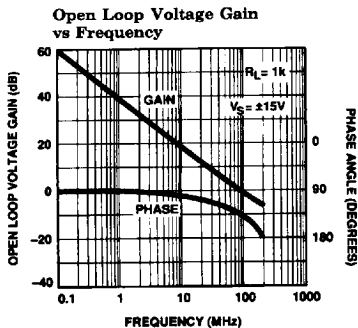Note 11: $R_L = 200\Omega$.

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Typical Performance Curves

Input Offset Voltage vs Supply Voltage

Supply Current vs Supply Voltage

Input Current vs Temperature (2 Typical units)

Input Offset Voltage vs Temperature (3 Typical units)

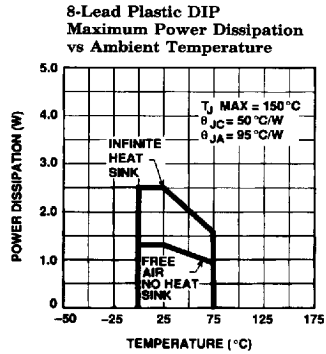**Voltage Gain vs Supply Voltage**

2041–4
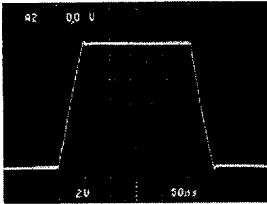
1-63
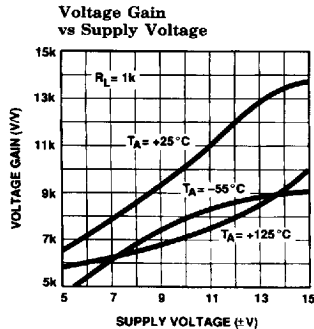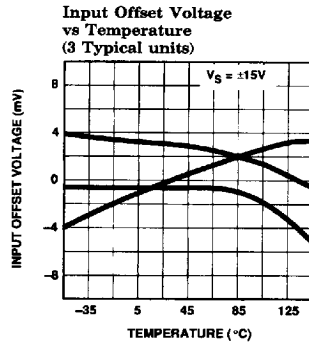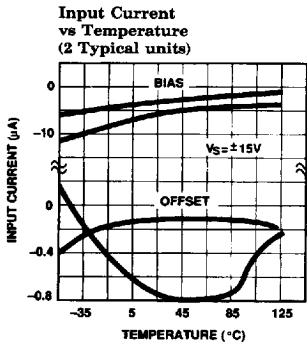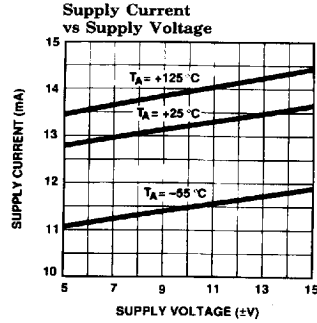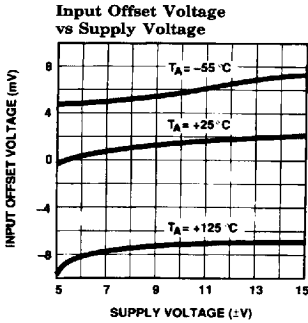
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Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage

Output Voltage Swing vs Frequency

Open Loop Voltage Gain vs Frequency

Gain Bandwidth Product at 10 MHz vs Supply Voltage

Input Referred Power Supply Rejection Ratio vs Frequency

2041–5

1-64

Typical Performance Curves — Contd.

Input Referred Common Mode Rejection Ratio vs Frequency

Settling Time $A_V = +1$

Input Noise Voltage vs Frequency

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

2041-6

3129557 0002881 448
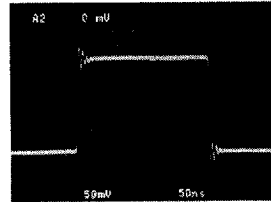
Typical Performance Curves — Contd.

Large Signal Response

2041-7

$A_V = +1$
$V_{IN} = \pm 5V$
$V_O = \pm 5V$

Small Signal Response

2041-8

$A_V = +1$
$V_{IN} = \pm 100 \text{ mV}$
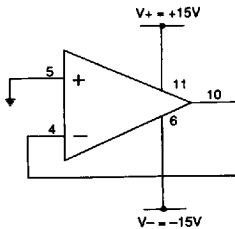$V_O = \pm 100 \text{ mV}$

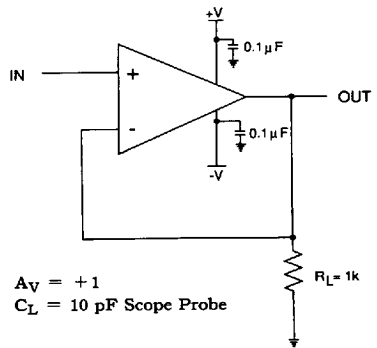### Open Loop Gain and Phase Response
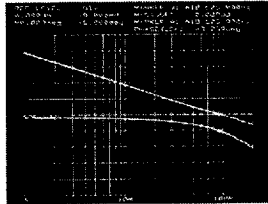
2041-9

Burn-In Circuit

2041-10

Pin numbers are for 14-Lead cerDIP. Burn-in circuit is identical for all package types.

Test Circuit

$A_V = +1$
$C_L = 10 \text{ pF Scope Probe}$

2041-11

Application Hints

Product Description

The EL2041 is a wideband monolithic operational amplifier built on Elantec's proprietary Complementary Bipolar process. Unlike many ±5V wideband op amps available today, the EL2041 operates from ±5V to ±15V and is capable of driving ±11V at its output. The large signal swing and open loop voltage gain of 80 dB with a 1 kΩ load, differentiate the EL2041 from other op amps that do not have sufficient load isolation. Another unusual characteristic of the amplifier is the extremely wide unity gain bandwidth of 90 MHz. This bandwidth is accomplished with a 45° phase margin, a 6.5 dB gain margin, and a slew rate of 250 V/μs. These AC characteristics are realized with a 13 mA supply current, which means lower power dissipation and higher reliability than competing products.

Power Supply Bypass

It is important to bypass the power supplies of the EL2041 with 0.1 μF or 0.01 μF ceramic disc capacitors. Failure to do this will result in oscillation or signal distortion. Although the lead length is not critical, it should not be more than ½″ from the IC pins.
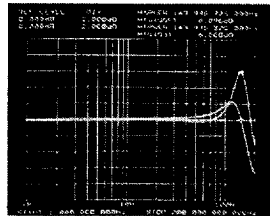
Capacitive Loading

Like all high speed op amps, the EL2041 is sensitive to capacitive loading. There are at least two ways to approach this problem: The use of a snubber (Q spoiler), or the use of feedback isolation.

The first approach is to consider the output stage of the amplifier as a highly inductive element due to the application of feedback. When this output stage is loaded with a capacitance a natural resonance occurs. By putting a series RC at the output of the amplifier, the energy of the tank can be absorbed, quenching the instability. The way to select the RC values for the Q spoiler is to drive a small signal (few 100 mV) squarewave into the desired capacitive load. Place a small resistor (few 100Ω) at the output to ground, and note the reduction in ringing. When the desired

response has been obtained, the capacitance value can be chosen. Start with a few 10's of pico farads in series with the selected resistor. Adjust the capacitor for the desired response. The capacitor value cannot be chosen arbitrarily large because of the reduction in open loop gain the series resistor will cause. In the example shown, the effects of a 15 pF load have been eliminated. Larger values of load capacitance can be tamed with a different RC value.
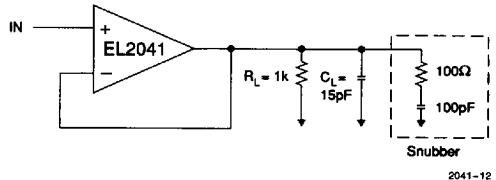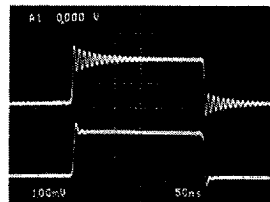

2041–12

2041–13

Frequency Response +6 dB Peak without Snubber and +2 dB with 200Ω, 20 pF Snubber.

2041–14

Top Trace is without Snubber; Bottom Trace is 100Ω, 100 pF Snubber.

Another way to look at the effect of capacitive loading is in the frequency domain. The open loop output impedance of the EL2041 is about 40Ω; when the output is loaded with 15 pF, an output pole is formed at 265 MHz. This pole sounds innocent enough until it's realized that it causes a phase shift of $\tan^{-1} \omega RC$, and at 100 MHz that is 21°. If the amplifier has a 45°
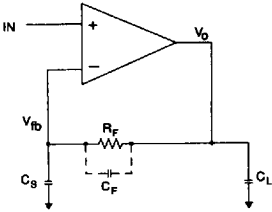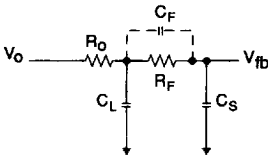
Application Hints — Contd.

phase margin with no capacitive loading, then with 15 pF it will reduce to 24° and considerable ringing will occur. Some help can be obtained by isolating the output from the capacitance on the inverting input.

Voltage Follower with Feedback Isolation

2041-15

Equivalent Circuit for Signal, Fed Back

2041-16

The signal fed back is:

$$\frac{V_{FB}}{V_O} = \frac{1}{(1+SC_LR_O)(1+SR_FC_S)}$$

The situation now appears to have been made worse with an output pole and a feedback pole, but with the addition of a capacitor C_F, the effects of the stray capacitance at the inverting input can be swamped.

$$\frac{V_{FB}}{V_O} = \frac{1+SC_FR_F}{(1+SC_LR_O)(1+SR_F[C_F+C_S])}$$

The trick here is to pick C_F large enough to overwhelm C_S and cancel the feedback pole. However C_F cannot be made too large or it will look like an AC short and C_S will again appear in parallel

with C_L. Some typical values to begin design work are: $R_F = 200$, $C_F = 15$ pF, for $C_L = 15$ pF, and C_S depends on board layout (try to minimize). It should also be realized that these values of R_F and C_F will begin to roll-off the close loop gain at 40 MHz.

Input Overdrive

It is important not to overdrive the input of the EL2041. Input slew rates in excess of 180 V/µs can cause distortion in the large signal square wave response, and this will show up as an increase in settling time (see typical performance curves). There are several solutions to this: Slew rate limit the input source, put clamp diodes across the amplifier inputs, or take some voltage gain in the amplifier.

Slew rate limit the input: For example with a 10 $V_{p\text{-}p}$ step at the input, the input rate should be limited to:
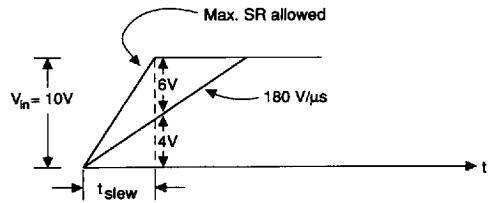
2041-17

$$t_{SLEW} = \frac{V_{IN} - V_{ZENER}}{min\ SR},$$
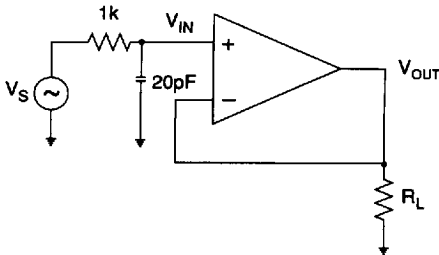
$$\text{Max source } SR = \frac{V_{IN}}{t_{SLEW}}$$

or

$$\frac{10-6}{180\ V/\mu s} = 22\ ns \quad , \quad \text{Max SR} = \frac{10}{22\ ns} = 450\ V/\mu s$$

If the input slew rate is limited by a 1k resistor, how large a capacitor is needed?

$$\frac{10V}{1k} = 10\ mA = C\frac{dv}{dt} \quad , \quad C = \frac{10\ mA}{450\ V/\mu s} = 22\ pF$$

## Application Hints — Contd.

2041-18

This value of R and C will give a -3 dB bandwidth of 8 MHz through the op amp. This technique should be avoided if the intended use is a small signal sinewave application.

Clamp diodes across the inputs: To obtain full slew rate at elevated temperature requires a V_{BE} of overdrive across the inputs. To insure adequate protection and slew rate requires two diodes in each direction across the inputs. A small series resistance in the input will limit the current through the diodes.
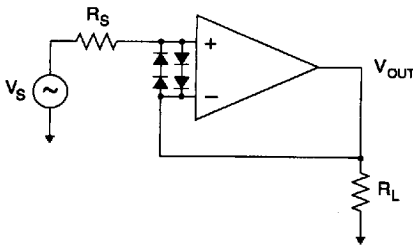
2041-19

Take voltage gain in the op amp: By taking voltage gain, the input stage does not have to handle as large a signal swing for a given output swing. For a voltage gain of 2, remember that the closed loop bandwidth will go to 45 MHz.
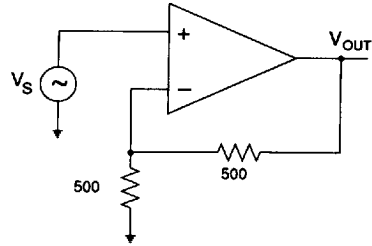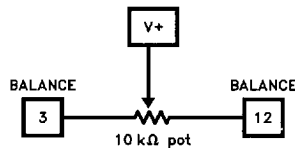

2041-20

Using the BALANCE Pins on the EL2041 Operational Amplifier

The BALANCE pins on the EL2041 can be used to tune out or adjust the input offset voltage of the op amp. To use these pins, ignore the connections shown on the simplified schematic on page 1-171. The adjust current is mirrored up to pnp current sources near V+ and the BALANCE adjustment pot goes between the collectors of two same-sex transistors. Take a 10 kΩ potentiometer (or lower) and connect the ends of the pot to the BALANCE pins and then connect the wiper to +V as shown (see Figure below). Moving the wiper between the two values should zero out the offset voltage.

In hooking up the example test circuit and measuring the voltage between pins 4 and 5 of an EL2041J, with supply voltages of ± 15V and a 10 kΩ pot between pins 3 and 12, an example adjustment range of $+10.3$ mV to -13.4 mV for V_{OS} was measured. The adjust range can be increased by lowering the size of the trim pot and decreased by increasing it. Adjustment range will vary slightly from part to part.
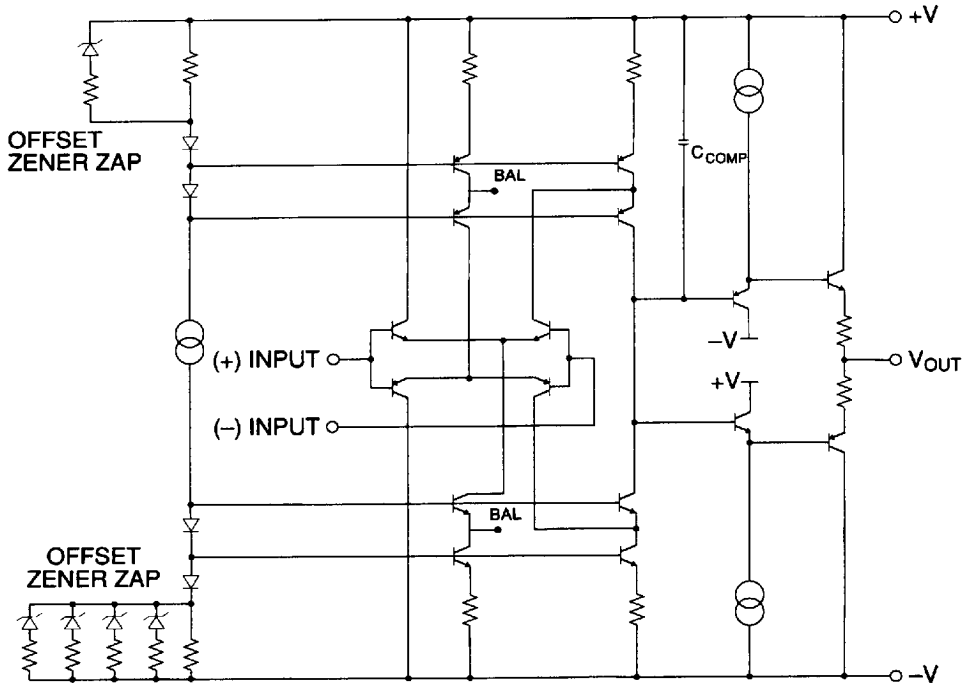

2041-23

Simplified Schematic

2041-21

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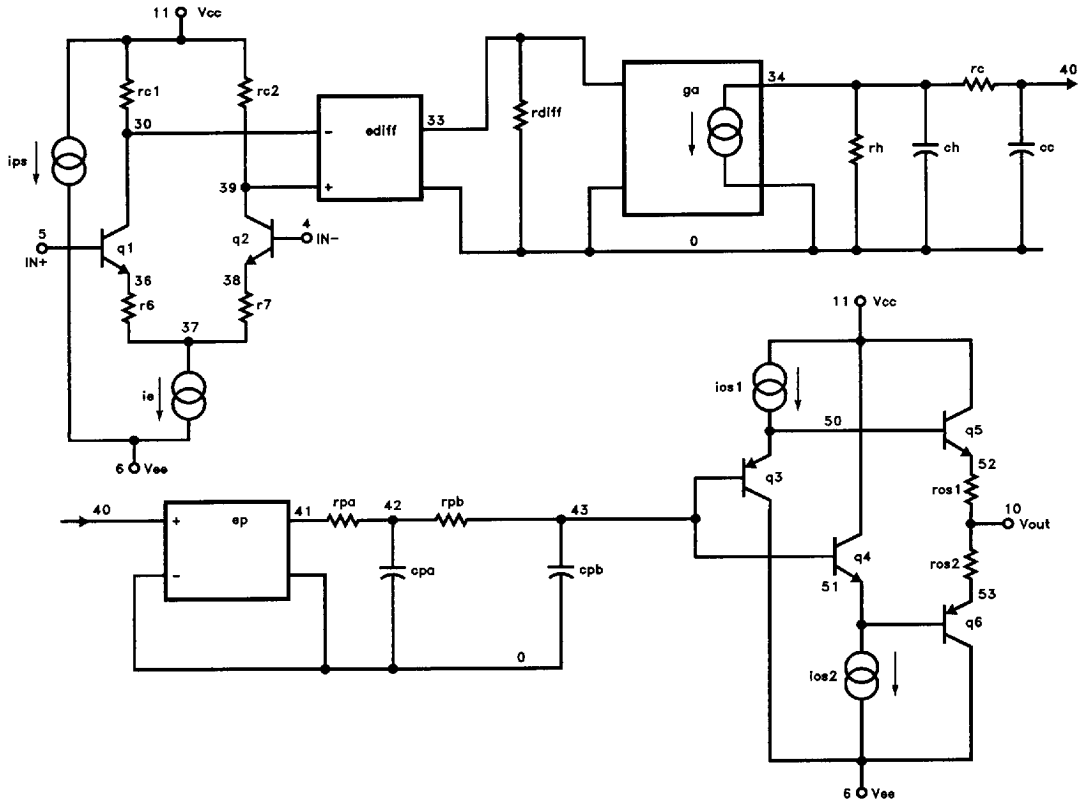
EL2041 Macromodel

```
* Connections:     + input
*                  |    − input
*                  |    |    + Vsupply
*                  |    |    |    − Vsupply
*                  |    |    |    |    output
*                  |    |    |    |    |
.subckt M2041      5    4    11   6    10
* Input stage
ie 37 6 3.7mA
r6 36 37 75
r7 38 37 75
rc1 11 30 75
rc2 11 39 75
q1 30 5 36 qn
q2 39 4 38 qna
ediff 33 0 39 30 3
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 5.2m
rh 34 0 1Meg
ch 34 0 16pF
rc 34 40 300
cc 40 0 1.5pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 2pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 11 50 1.25mA
ios2 51 6 1.25mA
q3 6 43 50 qp
q4 11 43 51 qn
q5 11 50 52 qn
q6 6 51 53 qp
ros1 52 10 25
ros2 10 53 25
* Power Supply Current
ips 11 6 6.5mA
* Models
.model qn npn(is = 800.0E − 18 bf = 340 tf = 0.2nS)
.model qna npn(is = 864E − 18 bf = 400 tf = 0.2nS)
.model qp pnp(is = 800E − 18 bf = 60 tf = 0.2nS)
.ends
```

EL2041 Macromodel — Contd.

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