**MOSEL VITELIC** *V53C316580000*

# *3.3 VOLT 8M X 8 FAST PAGE MODE CMOS DYNAMIC RAM*

| V53C316580000 | 40 | 50 | 60 |
|---|---|---|---|
| Max. $\overline{RAS}$ Access Time, ($t_{RAC}$) | 40 ns | 50 ns | 60 ns |
| Max. Column Address Access Time, ($t_{CAA}$) | 20 ns | 25 ns | 30 ns |
| Min. Fast Page Mode Cycle Time, ($t_{PC}$) | 30 ns | 35 ns | 40 ns |
| Min. Read/Write Cycle Time, ($t_{RC}$) | 75 ns | 90 ns | 110 ns |

- 8M x 8-bit organization
- Fast Page Mode for a sustained data rate of 33 MHz
- $\overline{RAS}$ access time: 40, 50, 60 ns
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh
- Self Refresh (L-version only)
- Refresh Interval: 4096 cycles/64 ms
- Available in 32-pin 400 mil SOJ, and 32-pin 400 mil TSOP-II
- Single +3.3 V ±0.3 V Power Supply
- TTL Interface

## *Description*

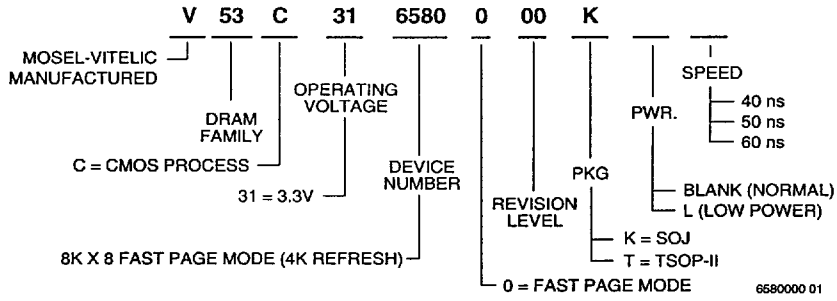
The V53C316580000 is a 8,388,608 x 8 bit high-performance CMOS dynamic random access memory. The V53C316580000 offers Page mode operation. The V53C316580000 has an asymmetric address, 12-bit row and 11-bit column.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 2048 x 8 bits, within a page, with cycle times as short as 30 ns.

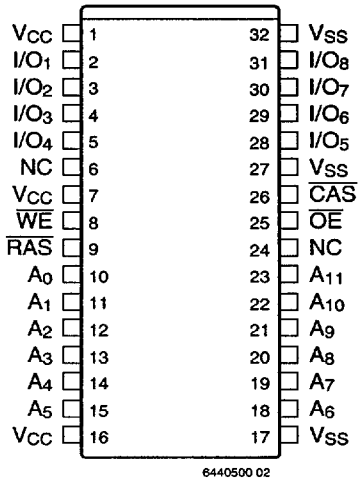
These features make the V53C316580000 ideally suited for a wide variety of high performance computer systems and peripheral applications.

## *Device Usage Chart*

| Operating Temperature Range | Package Outline | | Access Time (ns) | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|---|
| | K | T | 40 | 50 | 60 | Std. | L | |
| 0°C to 70 °C | • | • | • | • | • | • | • | Blank |




### *32 Pin Plastic SOJ /TSOP-II*
### *PIN CONFIGURATION*
### *Top View*




| Description | Pkg. | Pin Count |
|---|---|---|
| SOJ | K | 32 |
| TSOP-II | T | 32 |

### *Pin Names*

| | |
|---|---|
| $A_0$–$A_{11}$ | Row, Column Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $I/O_1$–$I/O_8$ | Data Input, Output |
| $V_{CC}$ | +3.3V Supply |
| $V_{SS}$ | 0V Supply |
| NC | No Connect |

### *Absolute Maximum Ratings**

Operating temperature range .....0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Soldering temperature .....260 °C
Soldering time .....10 s
Input/output voltage .... -0.5 to min ($V_{CC}$+0.5, 4.6) V
Power supply voltage .....-0.5V to 4.6 V
Power dissipation .....1.0 W
Data out current (short circuit) .....50 mA

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

### *Capacitance**

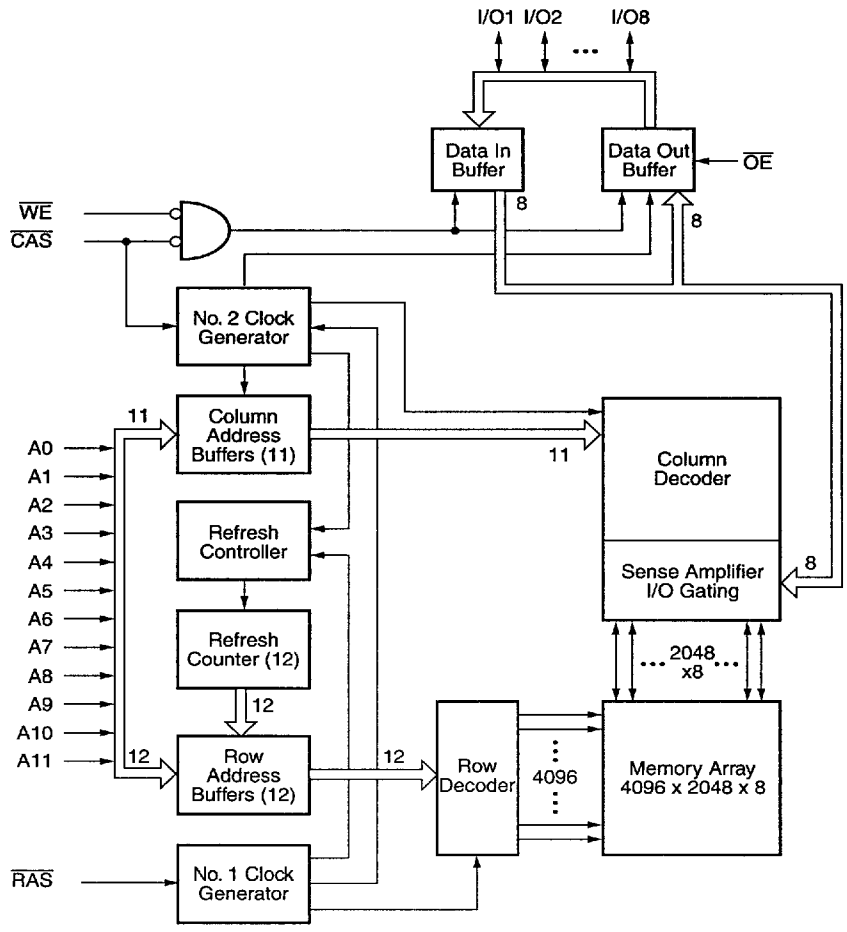
$T_A$ = 25°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V, f = 1 Mhz

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN1}$ | Address Input | — | 5 | pF |
| $C_{IN2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | — | 7 | pF |
| $C_{OUT}$ | Data Input/Output | — | 7 | pF |

***Note:** Capacitance is sampled and not 100% tested.

### *Block Diagram*

**8M x 8**



## DC and Operating Characteristics (1, 2)

$T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V, unless otherwise specified.

| Symbol | Parameter | Access Time | V53C316580000 Min. | Typ. | Max. | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current (any input pin) | | –2 | | 2 | µA | $V_{SS} \le V_{IN} \le V_{CC}$ | |
| $I_{LO}$ | Output Leakage Current (for High-Z State) | | –2 | | 2 | µA | $V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ | |
| $I_{CC1}$ | $V_{CC}$ Supply Current, Operating | 40 | | | 155 | mA | $t_{RC} = t_{RC}$ (min.) | 2, 3, 4 |
| | | 50 | | | 130 | | | |
| | | 60 | | | 105 | | | |
| $I_{CC2}$ | $V_{CC}$ Supply Current, TTL Standby | | | | 2 | mA | $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ other inputs ≥ $V_{SS}$ | |
| $I_{CC3}$ | $V_{CC}$ Supply Current, $\overline{RAS}$-Only Refresh | 40 | | | 155 | mA | $t_{RC} = t_{RC}$ (min.) | 2, 4 |
| | | 50 | | | 130 | | | |
| | | 60 | | | 105 | | | |
| $I_{CC4}$ | $V_{CC}$ Supply Current, Fast Page Mode Operation | 40 | | | 70 | mA | Minimum Cycle | 2, 3, 4 |
| | | 50 | | | 60 | | | |
| | | 60 | | | 50 | | | |
| $I_{CC5}$ | $V_{CC}$ Supply Current, CMOS Standby | | | | 900 | µA | $\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V | |
| $I_{CC5}$ | $V_{CC}$ Supply Current, CMOS Standby (L-Version) | | | | 200 | µA | $\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V | |
| $I_{CC6}$ | Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RASS}$ min., (L-version) $\overline{CAS}$ held low, $\overline{WE}$ = $V_{CC}$ – 0.2V, Address and $D_{IN}$ = $V_{CC}$ – 0.2V or 0.2V | | | | 400 | µA | | |
| $I_{CC7}$ | $V_{CC}$ Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh | 40 | | | 155 | mA | | 2, 4 |
| | | 50 | | | 130 | | | |
| | | 60 | | | 105 | | | |
| $V_{IL}$ | Input Low Voltage | | –0.3 | | 0.8 | V | | 1 |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+0.3 | V | | 1 |
| $V_{OL}$ | Output Low Voltage (LVTTL) | | | | 0.4 | V | $I_{OL}$ = 2 mA | 1 |
| $V_{OH}$ | Output High Voltage (LVTTL) | | 2.4 | | | V | $I_{OH}$ = –2 mA | 1 |
| $V_{OL}$ | Output Low Voltage (LVCMOS) | | | | 0.2 | V | $I_{OL}$ = 100 µA | 1 |
| $V_{OH}$ | Output High Voltage (LVCMOS) | | $V_{CC}$–0.2 | | | V | $I_{OH}$ = –100 µA | 1 |

## TRUTH TABLE

| FUNCTION | | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{OE}$ | ROW ADDR | COL ADDR | I/O1-I/O4 |
|---|---|---|---|---|---|---|---|---|
| Standby | | H | H → X | X | X | X | X | High Impedance |
| Read | | L | L | H | L | ROW | COL | Data Out |
| Early-Write | | L | L | L | X | ROW | COL | Data In |
| Delayed-Write | | L | L | H → L | H | ROW | COL | Data In |
| Read-Modify-Write | | L | L | H → L | L → H | ROW | COL | Data Out, Data In |
| Fast Page Mode Read | 1st Cycle | L | H → L | H | L | ROW | COL | Data Out |
| | 2nd Cycle | L | H → L | H | L | N/A | COL | Data Out |
| Fast Page Mode Early Write | 1st Cycle | L | H → L | L | X | ROW | COL | Data In |
| | 2nd Cycle | L | H → L | L | X | N/A | COL | Data In |
| Fast Page Mode RMW | 1st Cycle | L | H → L | H → L | L → H | ROW | COL | Data Out, Data In |
| | 2nd Cycle | L | H → L | H → L | L → H | N/A | COL | Data Out, Data In |
| $\overline{RAS}$ only refresh | | L | H | X | X | ROW | N/A | High Impedance |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh | | H → L | L | H | X | X | N/A | High Impedance |
| Test Mode Entry | | H → L | L | L | X | X | N/A | High Impedance |
| Hidden Refresh | READ | L→H→L | L | H | L | ROW | COL | Data Out |
| | WRITE | L→H→L | L | L | X | ROW | COL | Data In |

## AC Characteristics (6,7,8)

$T_A$ = 0 to 70 °C, $V_{CC}$ = 3.3 V±0.3V

| # | Symbol | Parameter | -40 | | - 50 | | - 60 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | min. | max. | | |
| | **Common Parameters** | | | | | | | | | |
| 1 | $t_{RC}$ | Random read or write cycle time | 75 | – | 90 | – | 110 | – | ns | |
| 2 | $t_{RAS}$ | $\overline{RAS}$ pulse width | 40 | 100k | 50 | 100k | 60 | 100k | ns | |
| 3 | $t_{CAS}$ | $\overline{CAS}$ pulse width | 10 | 100k | 13 | 100k | 15 | 100k | ns | |
| 4 | $t_{RP}$ | $\overline{RAS}$ precharge time | 25 | – | 30 | – | 40 | – | ns | |
| 5 | $t_{CP}$ | $\overline{CAS}$ precharge time | 10 | – | 10 | – | 10 | – | ns | |
| 6 | $t_{ASR}$ | Row address setup time | 0 | – | 0 | – | 0 | – | ns | |
| 7 | $t_{RAH}$ | Row address hold time | 5 | – | 7 | – | 10 | – | ns | |
| 8 | $t_{ASC}$ | Column address setup time | 0 | – | 0 | – | 0 | – | ns | |
| 9 | $t_{CAH}$ | Column address hold time | 5 | – | 7 | – | 10 | – | ns | |
| 10 | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ delay time | 15 | 30 | 17 | 37 | 20 | 45 | ns | |
| 11 | $t_{RAD}$ | $\overline{RAS}$ to column address delay | 10 | 20 | 12 | 25 | 15 | 30 | ns | |
| 12 | $t_{RSH}$ | $\overline{RAS}$ hold time | 10 | – | 13 | | 15 | – | ns | |
| 13 | $t_{CSH}$ | $\overline{CAS}$ hold time | 40 | – | 50 | | 60 | – | ns | |
| 14 | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ precharge time | 5 | – | 5 | – | 5 | – | ns | |
| 15 | $t_T$ | Transition time (rise and fall) | 1 | 30 | 1 | 30 | 1 | 30 | ns | 7 |
| 16 | $t_{REF}$ | Refresh period for 4k-refresh | – | 64 | – | 64 | – | 64 | ms | |
| 17 | $t_{REF}$ | Refresh period for L-versions | – | 256 | – | 256 | – | 256 | ms | |
| **Read Cycle** | | | | | | | | | | |
| 18 | $t_{RAC}$ | Access time from $\overline{RAS}$ | – | 40 | – | 50 | – | 60 | ns | 8, 9 |
| 19 | $t_{CAC}$ | Access time from $\overline{CAS}$ | – | 10 | – | 13 | – | 15 | ns | 8, 9 |
| 20 | $t_{CAA}$ | Access time from column address | – | 20 | – | 25 | – | 30 | ns | 8,10 |
| 21 | $t_{OEA}$ | $\overline{OE}$ access time | – | 10 | – | 13 | – | 15 | ns | 8 |
| 22 | $t_{RAL}$ | Column address to $\overline{RAS}$ lead time | 20 | – | 25 | – | 30 | – | ns | |
| 23 | $t_{RCS}$ | Read command setup time | 0 | – | 0 | – | 0 | – | ns | |
| 24 | $t_{RCH}$ | Read command hold time | 0 | – | 0 | – | 0 | – | ns | 11 |
| 25 | $t_{RRH}$ | Read command hold time referenced to $\overline{RAS}$ | 0 | – | 0 | – | 0 | – | ns | 11 |
| 26 | $t_{CLZ}$ | $\overline{CAS}$ to output in low-Z | 0 | – | 0 | – | 0 | – | ns | 8 |
| 27 | $t_{OFF}$ | Output buffer turn-off delay | 0 | 10 | 0 | 13 | 0 | 15 | ns | 12 |
| 28 | $t_{OEZ}$ | Output buffer turn-off delay from $\overline{OE}$ | 0 | 10 | 0 | 13 | 0 | 15 | ns | 12 |
| 29 | $t_{DZO}$ | Data to $\overline{OE}$ low delay | 0 | – | 0 | – | 0 | – | ns | 13 |

## AC Characteristics [6,7,8] (Continued)

$T_A$ = 0 to 70 °C, $V_{CC}$ = 3.3 V±0.3V

| # | Symbol | Parameter | -40 | | - 50 | | - 60 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | min. | max. | | |
| 30 | $t_{CDD}$ | $\overline{CAS}$ high to data delay | 10 | – | 13 | – | 15 | – | ns | 14 |
| 31 | $t_{ODD}$ | $\overline{OE}$ high to data delay | 10 | – | 13 | – | 15 | – | ns | 14 |
| **Write Cycle** | | | | | | | | | | |
| 32 | $t_{WCH}$ | Write command hold time | 5 | – | 7 | – | 10 | – | ns | |
| 33 | $t_{WP}$ | Write command pulse width | 5 | – | 7 | – | 10 | – | ns | |
| 34 | $t_{WCS}$ | Write command setup time | 0 | – | 0 | – | 0 | – | ns | 15 |
| 35 | $t_{RWL}$ | Write command to $\overline{RAS}$ lead time | 10 | – | 13 | – | 15 | – | ns | |
| 36 | $t_{CWL}$ | Write command to $\overline{CAS}$ lead time | 10 | – | 13 | – | 15 | – | ns | |
| 37 | $t_{DS}$ | Data setup time | 0 | – | 0 | – | 0 | – | ns | 16 |
| 38 | $t_{DH}$ | Data hold time | 5 | – | 7 | – | 10 | – | ns | 16 |
| 39 | $t_{DZC}$ | $\overline{CAS}$ delay time from Din | 0 | – | 0 | – | 0 | – | ns | 13 |
| **Read-modify-Write Cycle** | | | | | | | | | | |
| 40 | $t_{RWC}$ | Read-write cycle time | 105 | – | 126 | – | 150 | – | ns | |
| 41 | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ delay time | 55 | – | 68 | – | 80 | – | ns | 15 |
| 42 | $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ delay time | 25 | – | 31 | – | 35 | – | ns | 15 |
| 43 | $t_{AWD}$ | Column address to $\overline{WE}$ delay time | 35 | – | 43 | – | 50 | – | ns | 15 |
| 44 | $t_{OEH}$ | $\overline{OE}$ command hold time | 5 | – | 7 | – | 10 | – | ns | |
| **Fast Page Mode Cycle** | | | | | | | | | | |
| 45 | $t_{PC}$ | Fast Page Mode cycle time | 30 | – | 35 | – | 40 | – | ns | |
| 46 | $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | – | 25 | – | 30 | – | 35 | ns | 7 |
| 47 | $t_{RAS}$ | $\overline{RAS}$ pulse width in EDO page mode | 40 | 200k | 50 | 200k | 60 | 200k | ns | |
| 48 | $t_{RHPC}$ | $\overline{CAS}$ precharge to $\overline{RAS}$ Delay | 25 | – | 30 | – | 35 | – | ns | |
| **Fast Page Mode Read-modify-Write Cycle** | | | | | | | | | | |
| 49 | $t_{PRWC}$ | EDO page mode read-write cycle time | 60 | – | 71 | – | 80 | – | ns | |
| 50 | $t_{CPWD}$ | $\overline{CAS}$ precharge to $\overline{WE}$ | 40 | – | 48 | – | 55 | – | ns | |

## AC Characteristics [6,7,8] (Continued)

$T_A$ = 0 to 70 °C, $V_{CC}$ = 3.3 V±0.3V

| # | Symbol | Parameter | -40 | | - 50 | | - 60 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | min. | max. | | |
| **$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle** | | | | | | | | | | |
| 51 | $t_{CSR}$ | $\overline{CAS}$ setup time | 5 | – | 5 | – | 5 | – | ns | |
| 52 | $t_{CHR}$ | $\overline{CAS}$ hold time | 5 | – | 5 | – | 10 | – | ns | |
| 53 | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ precharge time | 0 | – | 0 | – | 0 | – | ns | |
| 54 | $t_{WRP}$ | Write to $\overline{RAS}$ precharge time | 5 | – | 5 | – | 10 | – | ns | |
| 55 | $t_{WRH}$ | Write hold time referenced to $\overline{RAS}$ | 5 | – | 5 | – | 10 | – | ns | |
| **Self Refresh Cycle (L-versions only)** | | | | | | | | | | |
| 56 | $t_{RASS}$ | $\overline{RAS}$ pulse width | 100k | | 100k | – | 100k | – | ns | 17 |
| 57 | $t_{RPS}$ | $\overline{RAS}$ precharge time | 75 | – | 90 | – | 110 | – | ns | 17 |
| 58 | $t_{CHS}$ | $\overline{CAS}$ hold time | -50 | – | -50 | – | -50 | – | ns | 17 |
| **Test Mode Cycle** | | | | | | | | | | |
| 59 | $t_{WTS}$ | Write command setup time | 5 | – | 5 | – | 5 | – | ns | 18 |
| 60 | $t_{WTH}$ | Write command hold time | 5 | – | 5 | – | 5 | – | ns | 18 |

***Notes:***

1) All voltages are referenced to VSS.

   $V_{IH}$ may overshoot to $V_{CC}$ + 0.2V for pulse widths of < 4ns with 3.3V. $V_{IL}$ may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

2) $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ and $I_{CC7}$ depend on cycle rate.

3) $I_{CC1}$ and $I_{CC4}$ depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$. In the case of $I_{CC4}$ it can be changed once or less during a fast page mode cycle ($t_{PC}$).

5) An initial pause of 100 µs is required after power-up followed by 8 $\overline{RAS}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume $t_T$ = 5 ns.

7) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.

8) Measured with the specified current load and 100 pF at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.

9) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If $t_{RCD}$ is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by $t_{CAC}$.

10) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If $t_{RAD}$ is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by $t_{CAA}$.

11) Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

12) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

13) Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.

14) Either $t_{CDD}$ or $t_{ODD}$ must be satisfied.

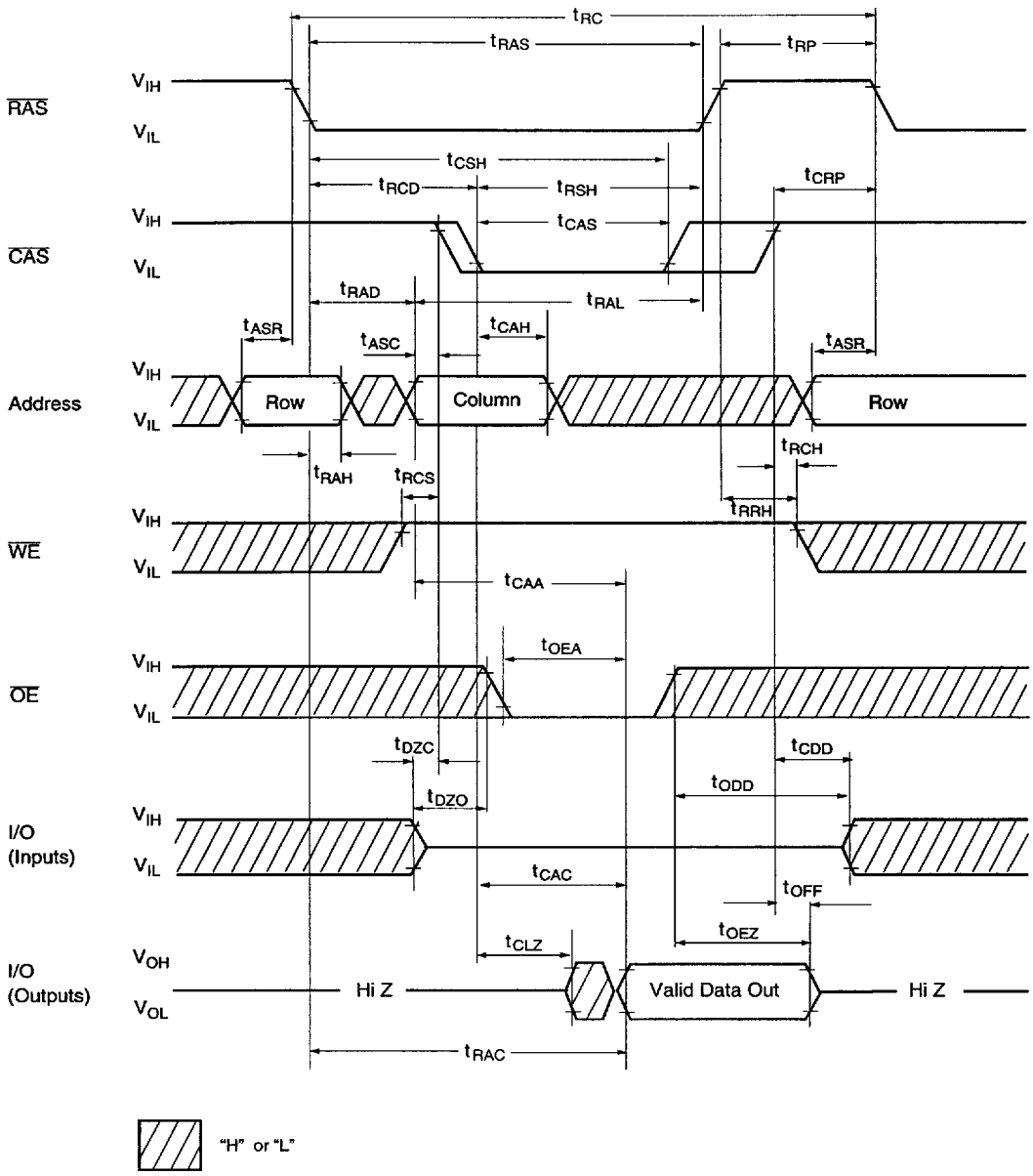
15) $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS}$ > $t_{WCS}$ (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD}$ > $t_{RWD\ (min.)}$, $t_{CWD}$ > $t_{CWD\ (min.)}$, $t_{AWD}$ > $t_{AWD\ (min.)}$ and $t_{CPWD}$ > $t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

16) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

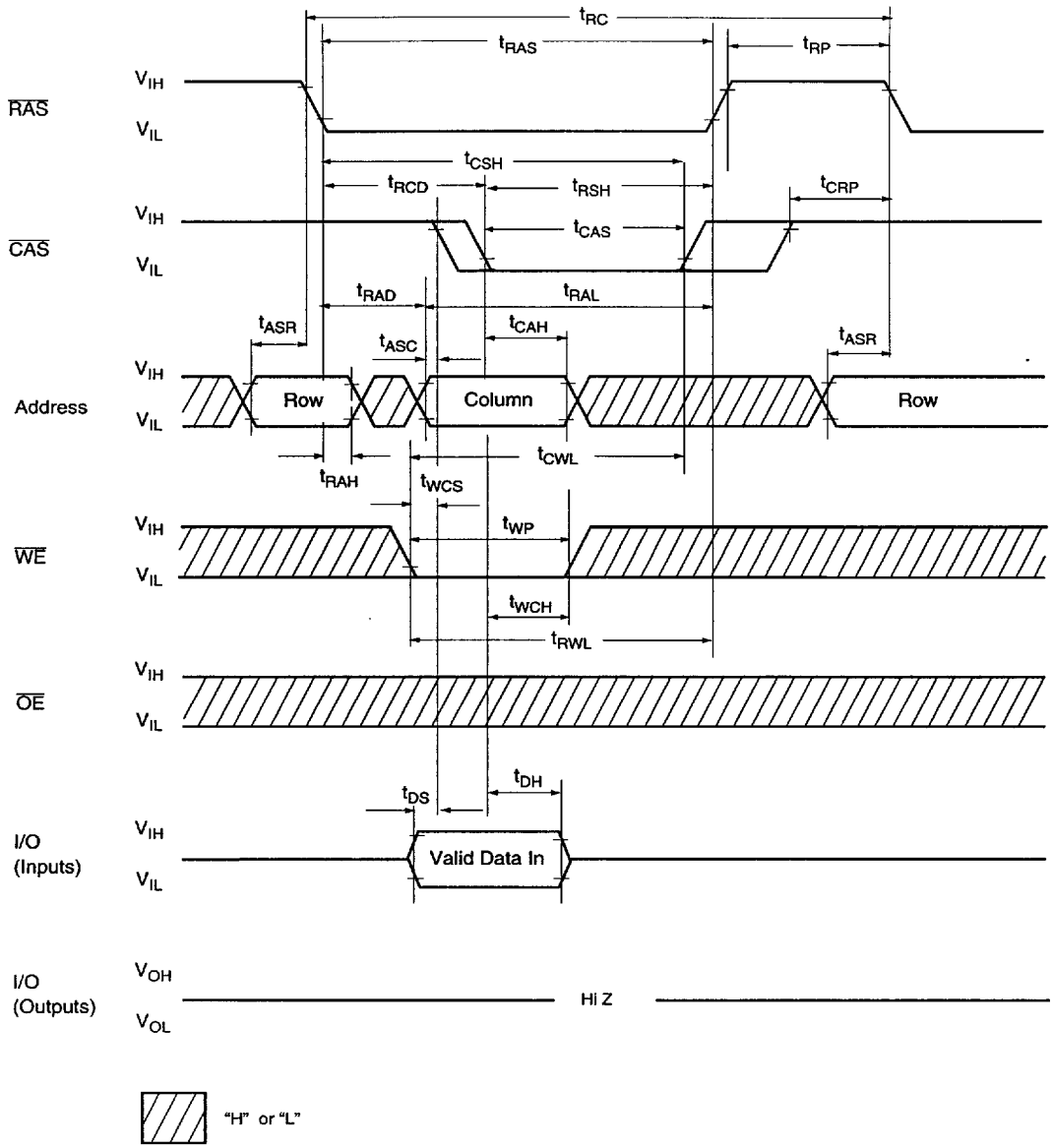
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
   If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh

18) In a Test Mode Read Cycle, the value of $t_{RAC}$, $t_{CAA}$, $t_{CAC}$ and $t_{CPA}$ are delayed by 5 ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must be adjusted by 5 ns.

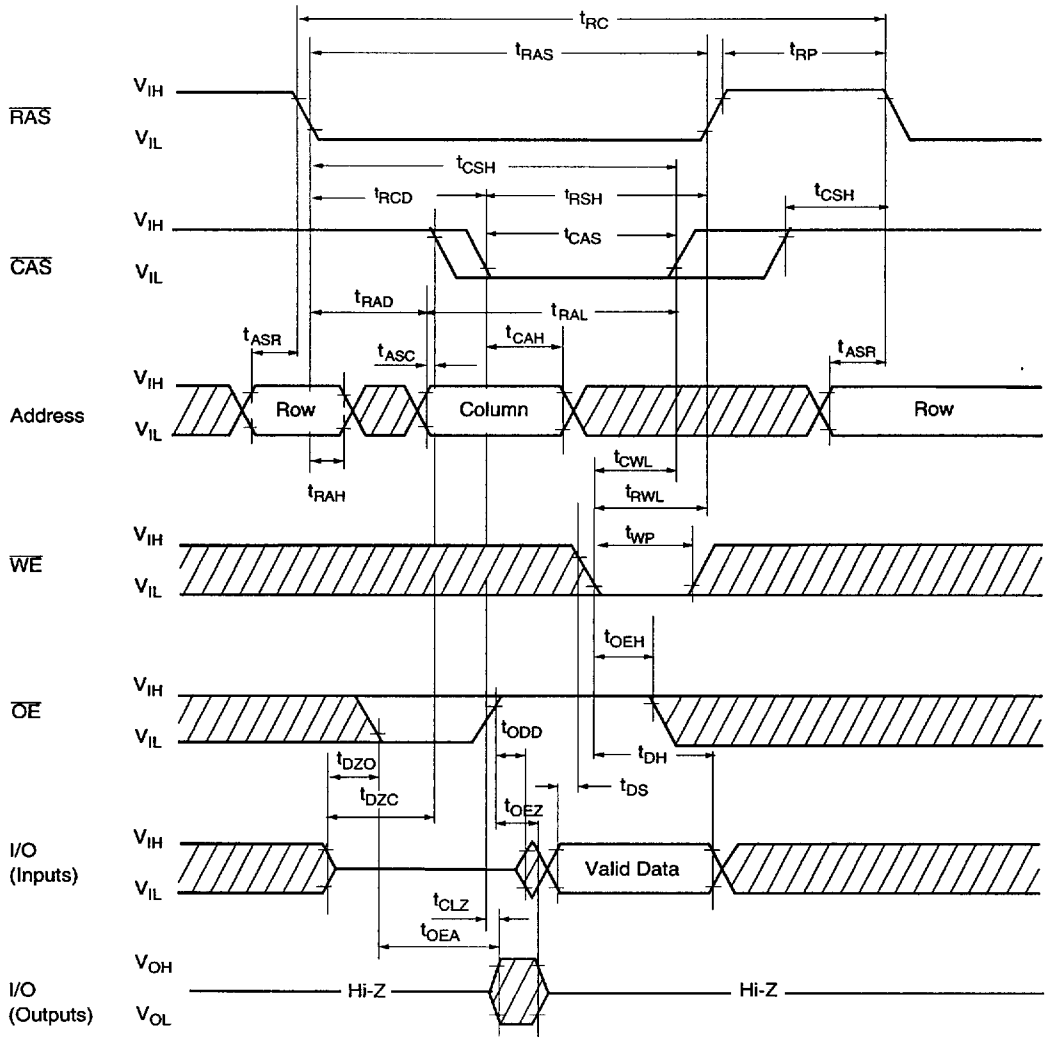
## Waveforms of Read Cycle



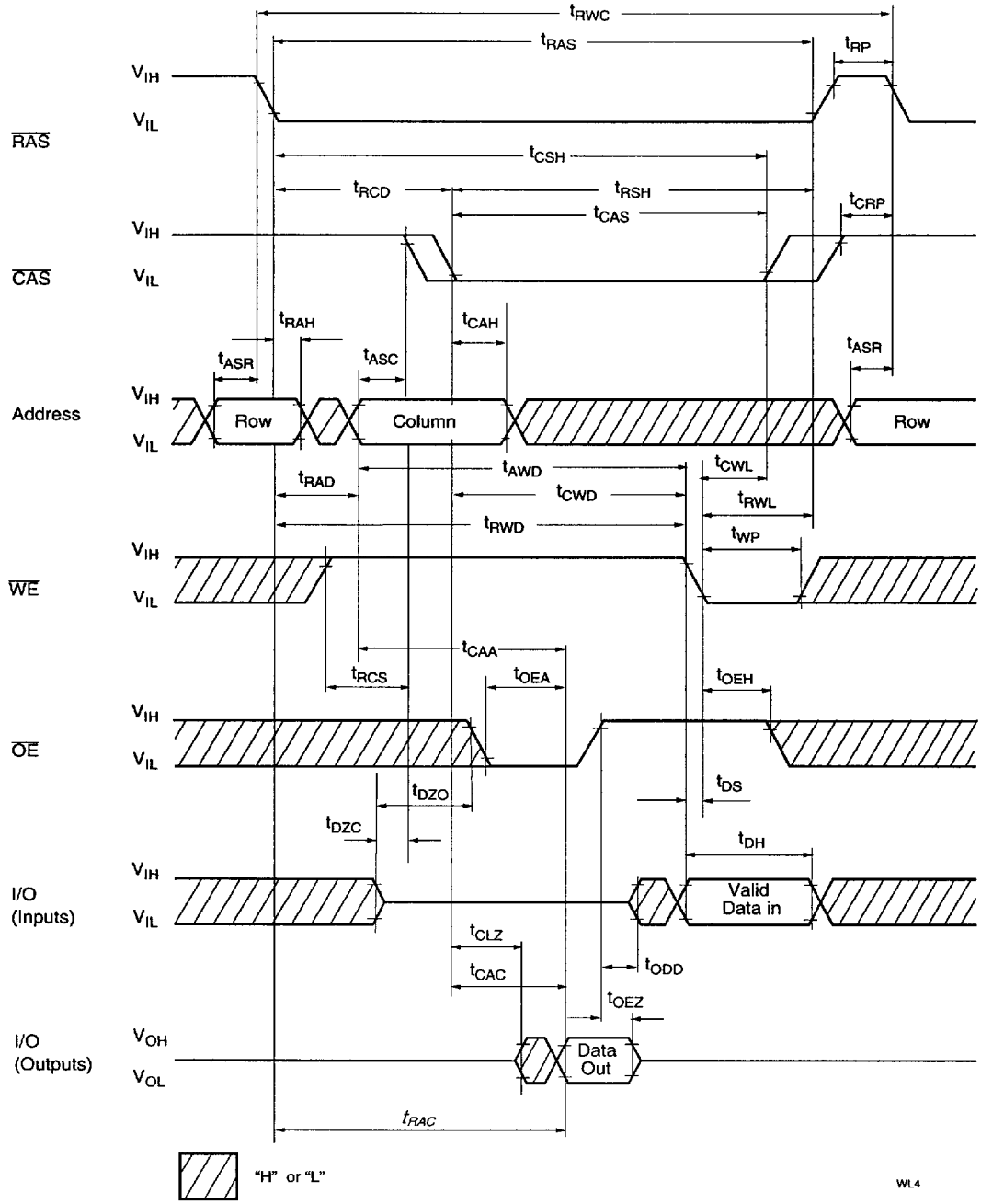
## Waveforms of Write Cycle (Early Write)



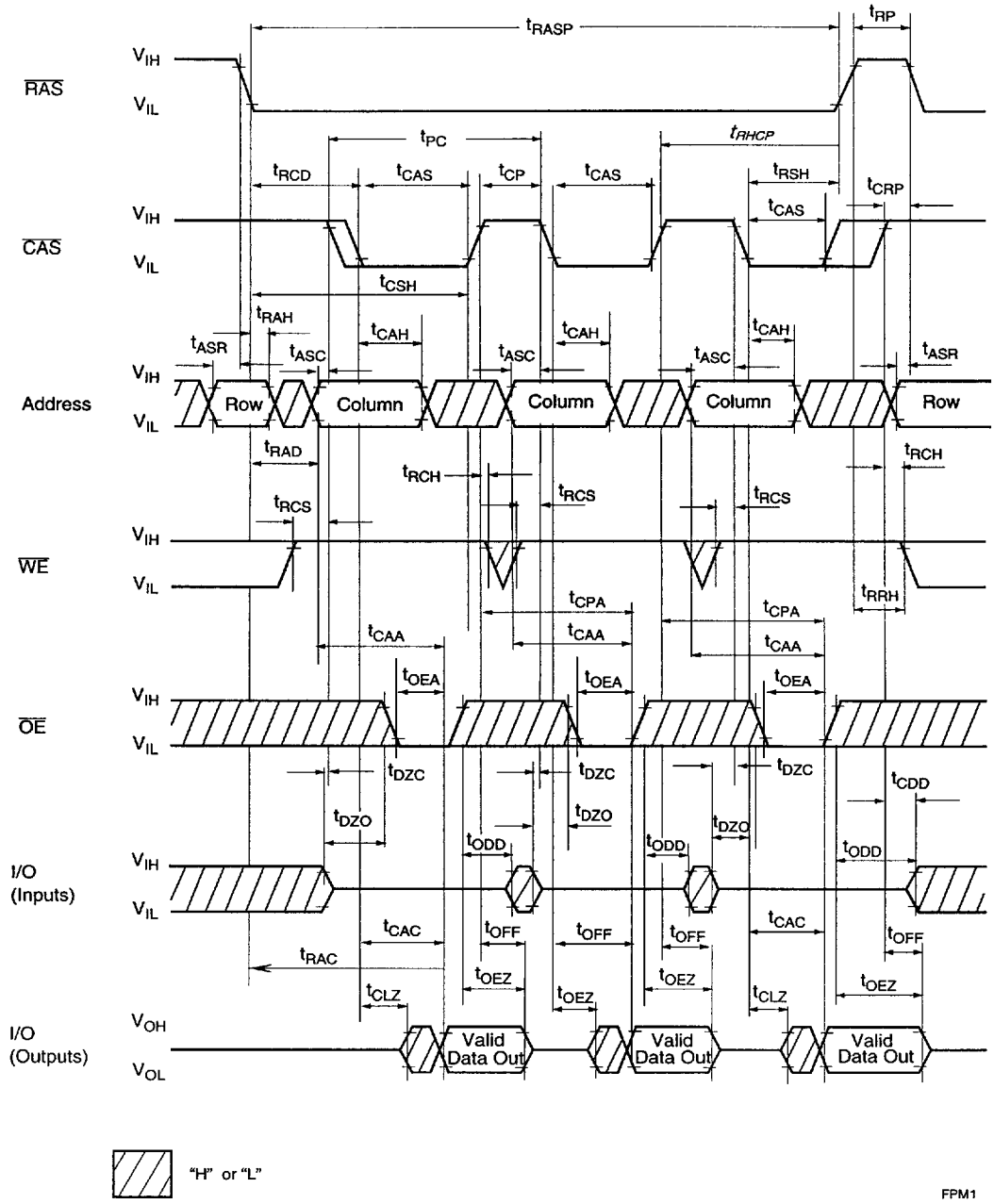
## Waveforms of Write Cycle ($\overline{OE}$ Controlled Write)



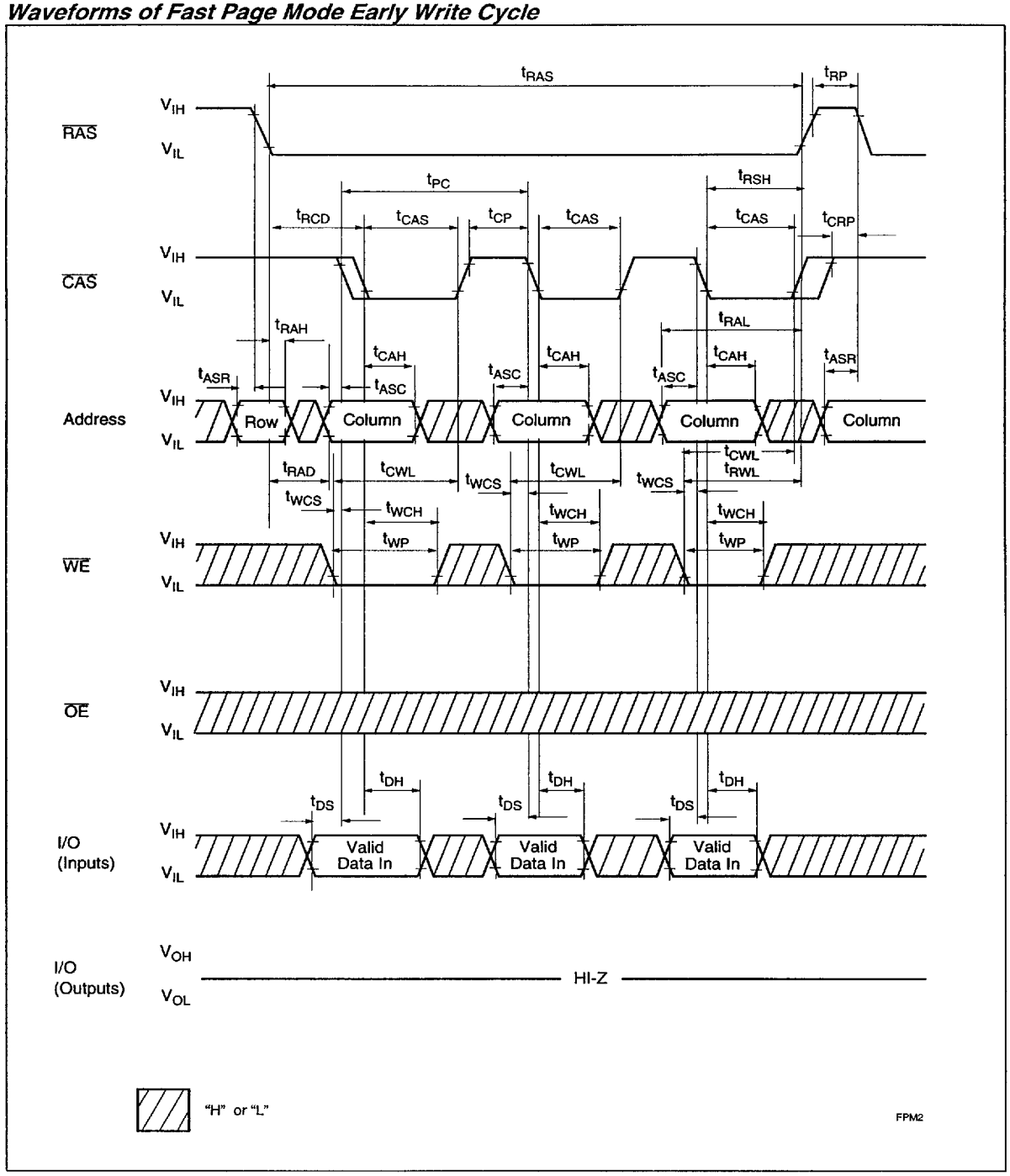
## Waveforms of Read-Write (Read-Modify-Write) Cycle



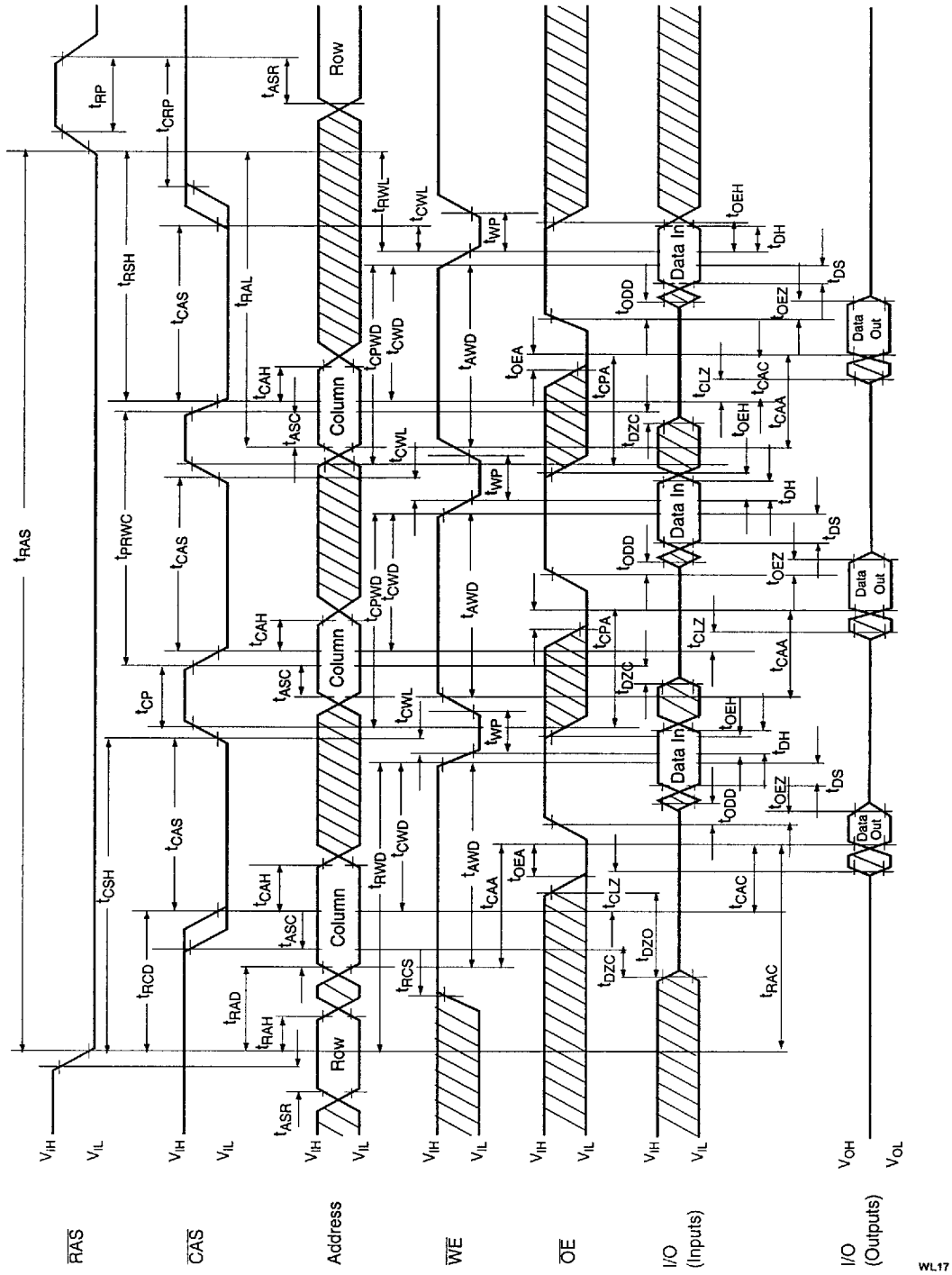
## Waveforms of Fast Page Mode Read Cycle



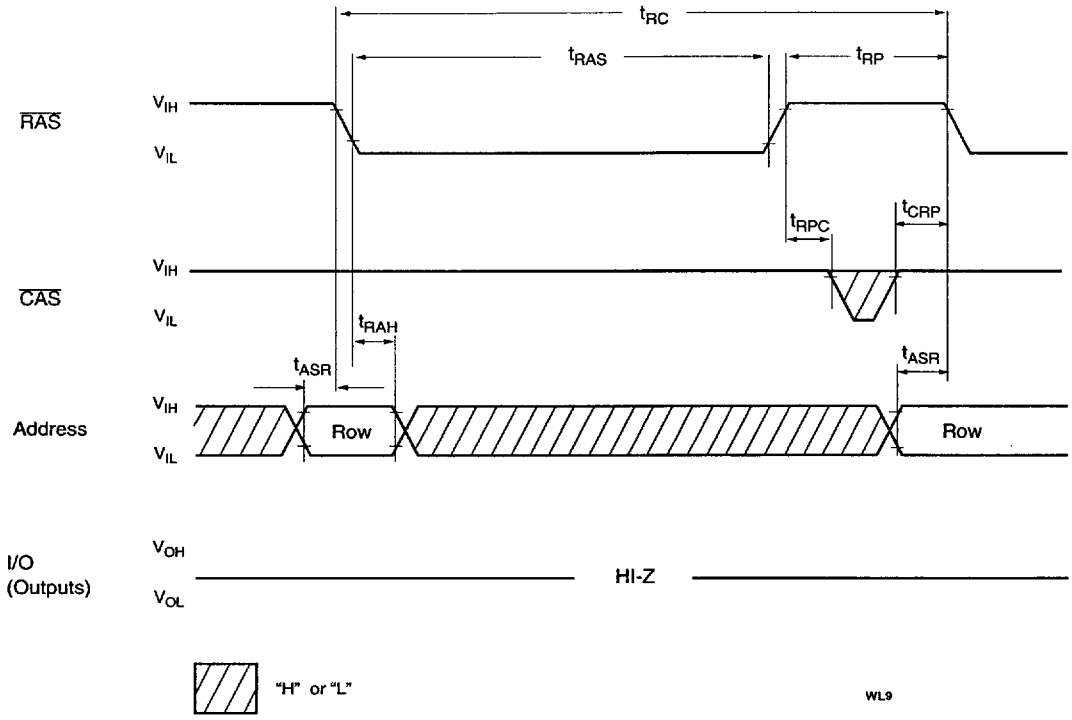
## Waveforms of Fast Page Mode Early Write Cycle



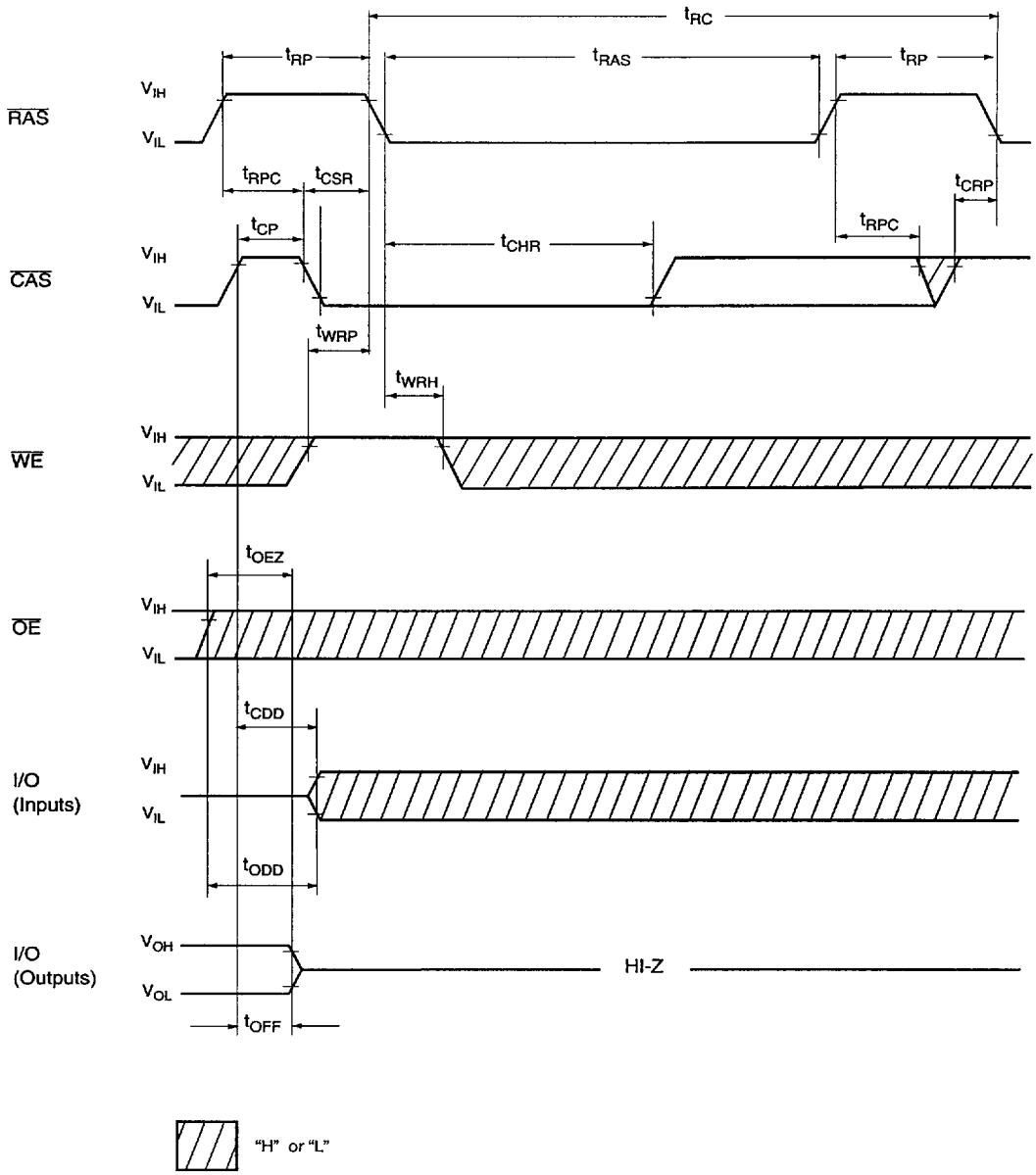
## Waveforms of Edo Page Mode Read-Modify-Write Cycle



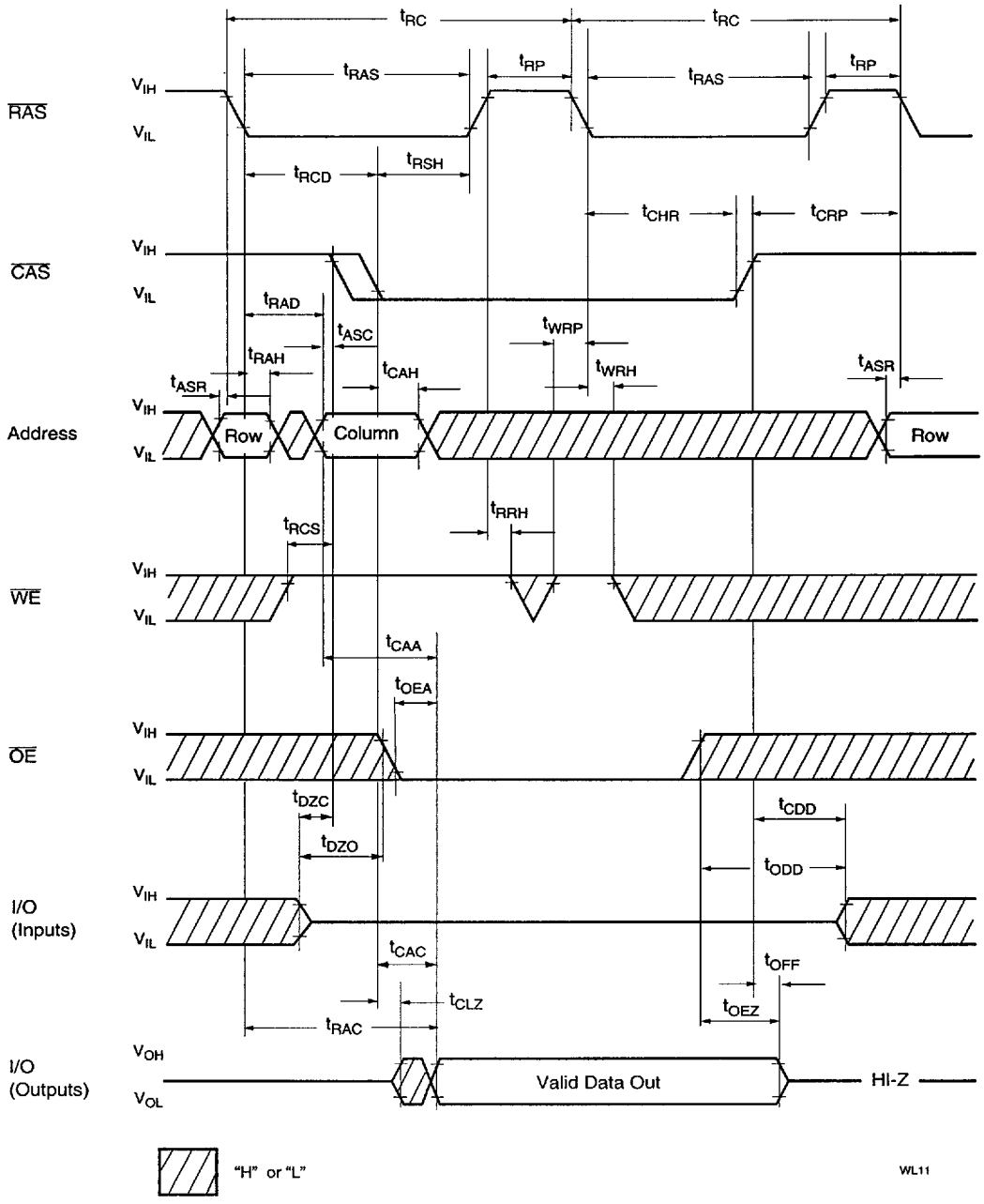
## Waveforms of $\overline{RAS}$ Only Refresh Cycle



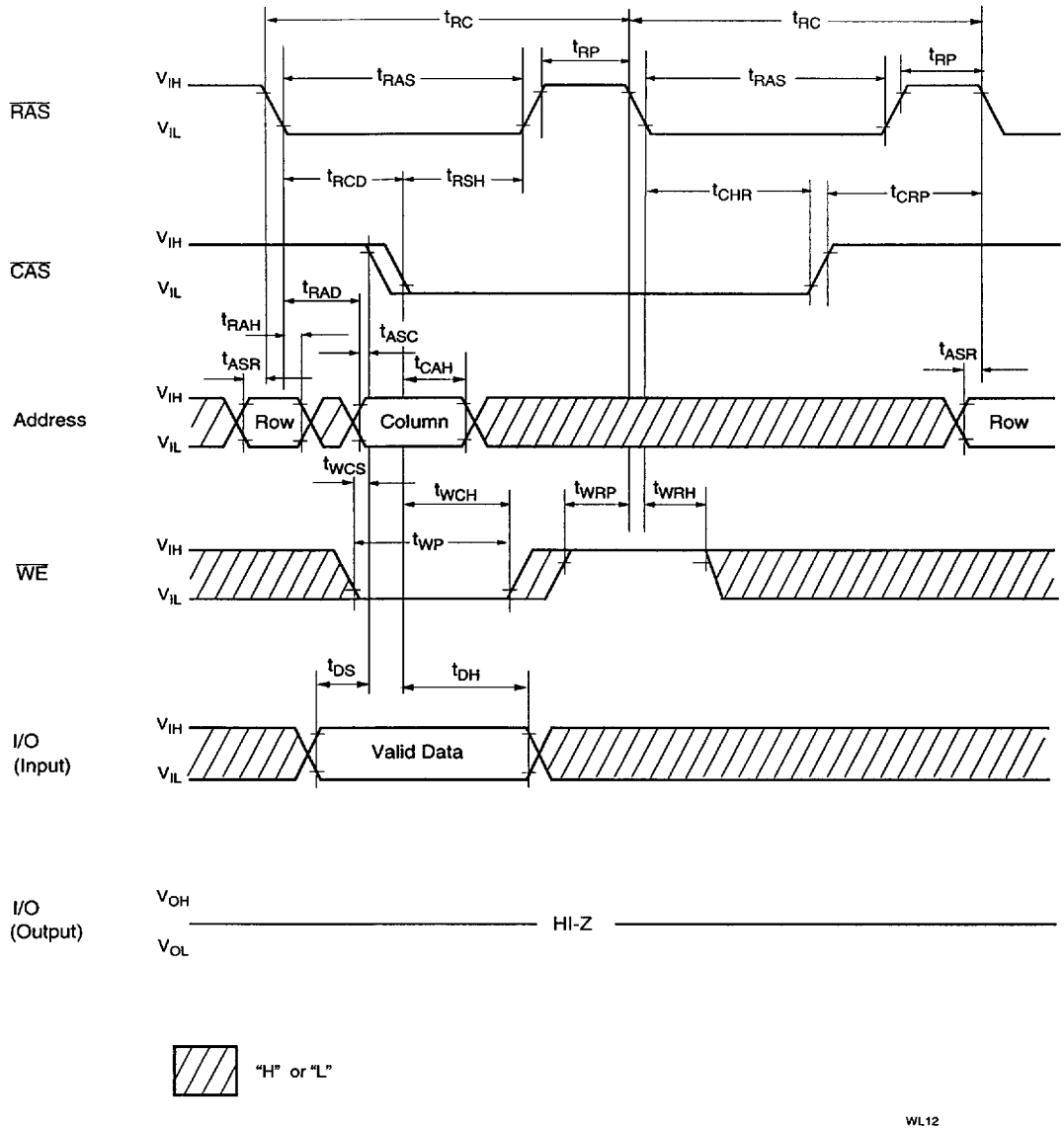
## *Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle*



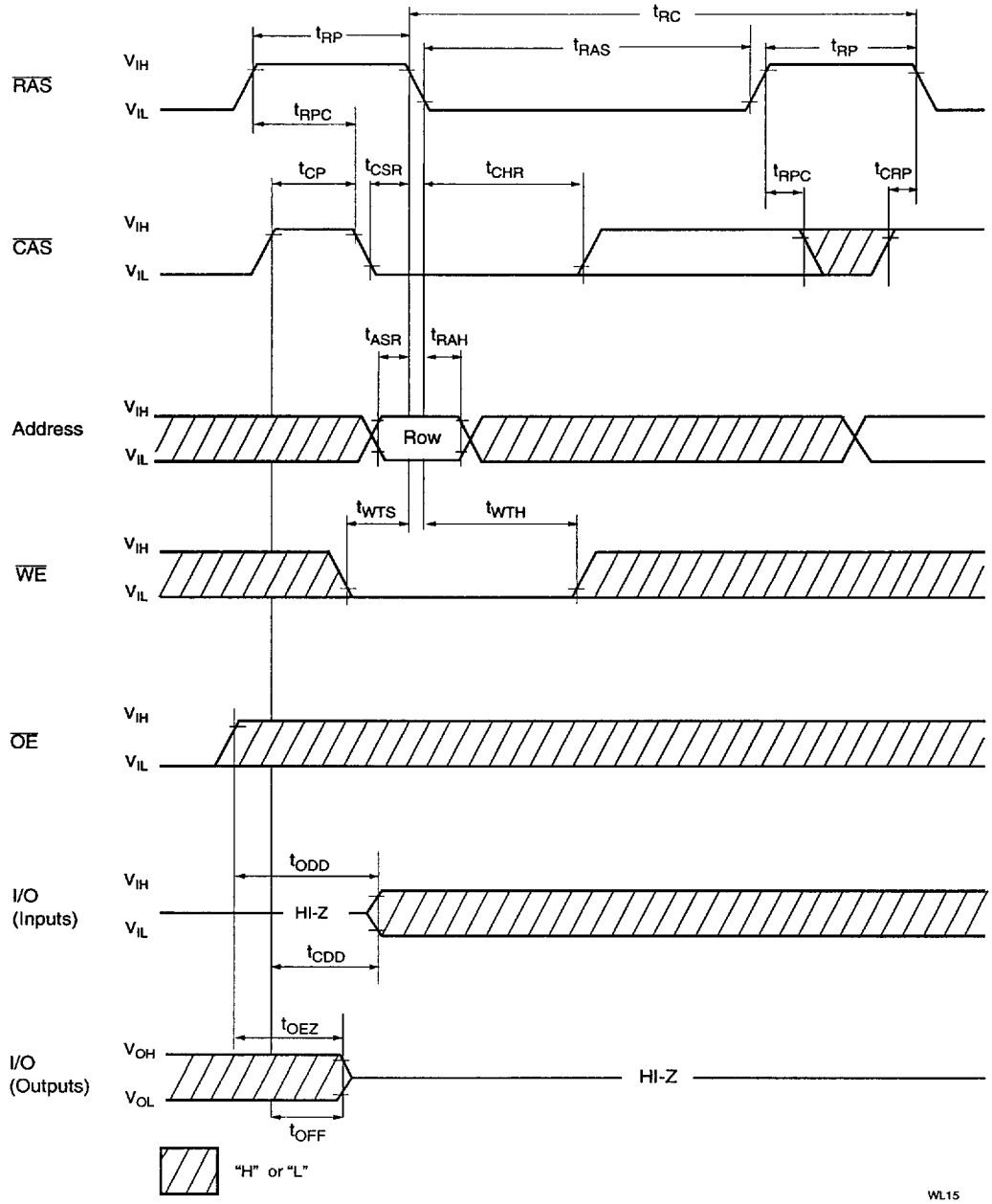
## Waveforms of Hidden Refresh Cycle (Read)



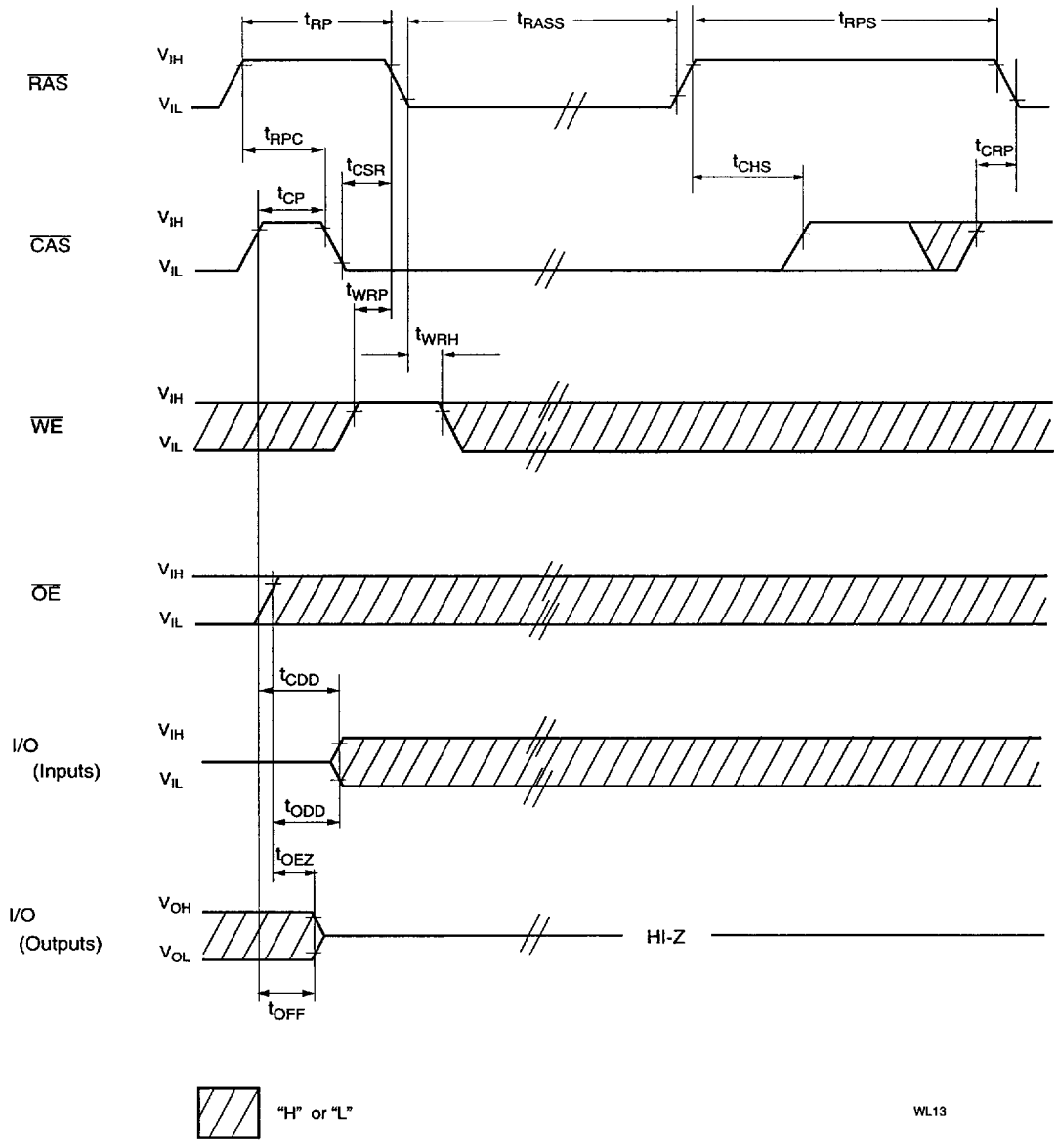
## Waveforms of Hidden Refresh Cycle (Early Write)



## Waveforms of Test Mode Entry Cycle



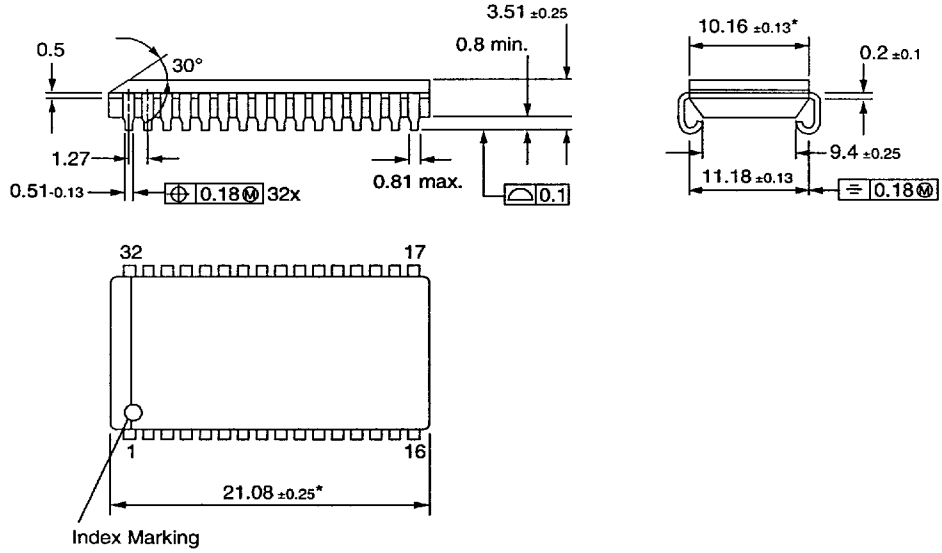
## Waveforms of Self Refresh (Sleep Mode) L-Version only



## Package Diagrams

### 32-pin 400 mil SOJ

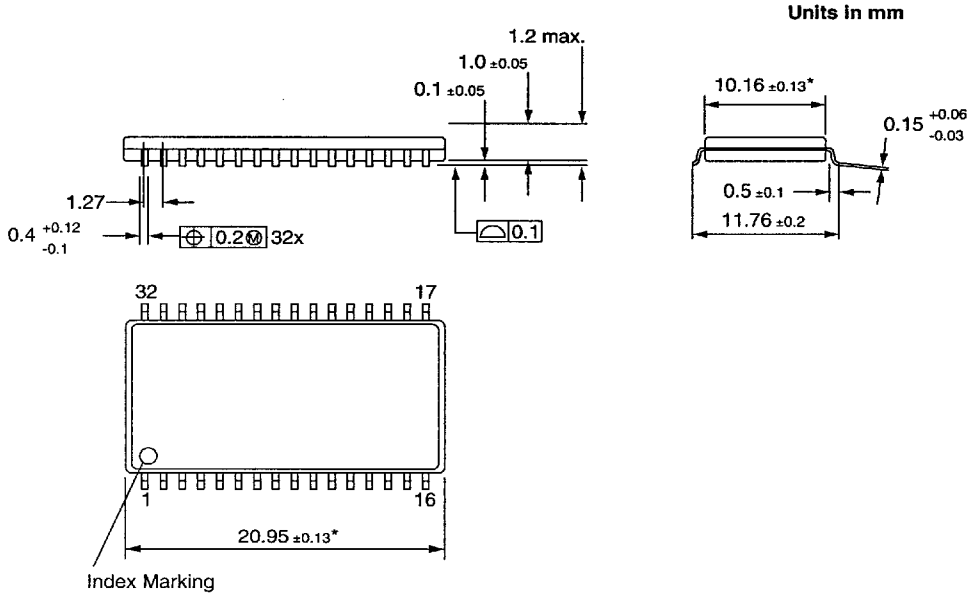
Units in mm




* Does not include plastic or metal protrusion of 0.15 max. per side

### 32-pin 400 mil TSOP-II

Units in mm




* Does not include plastic or metal protrusion of 0.25 max. per side