QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS Dual 4-Input Multiplexers

QS54/74FCT153T
QS54/74FCT253T
QS54/74FCT2153T

FEATURES/BENEFITS

- Pin and function compatible to the 74F153/253 74FCT153/253 and 74FCT153T/253T
- Industrial temperature –40°C to 85°C
- CMOS power levels: <7.5mW static
- Available in PDIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 153T, 253T

- JEDEC-FCT spec compatible
- A and C speed grades with 4.5ns t_{PD} for C
- I_{OL} = 48mA Ind., 32mA Mil.

FCT-T 2153T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A speed grade with 5.2ns t_{PD} for A
- I_{OL} = 12mA Ind.

DESCRIPTION

The QSFCT153T and QSFCT253T are high-speed CMOS TTL-compatible dual 4-input multiplexers. The 153 has TTL ouputs; the 253 has 3-state outputs. The QSFCT2153T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Ouputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

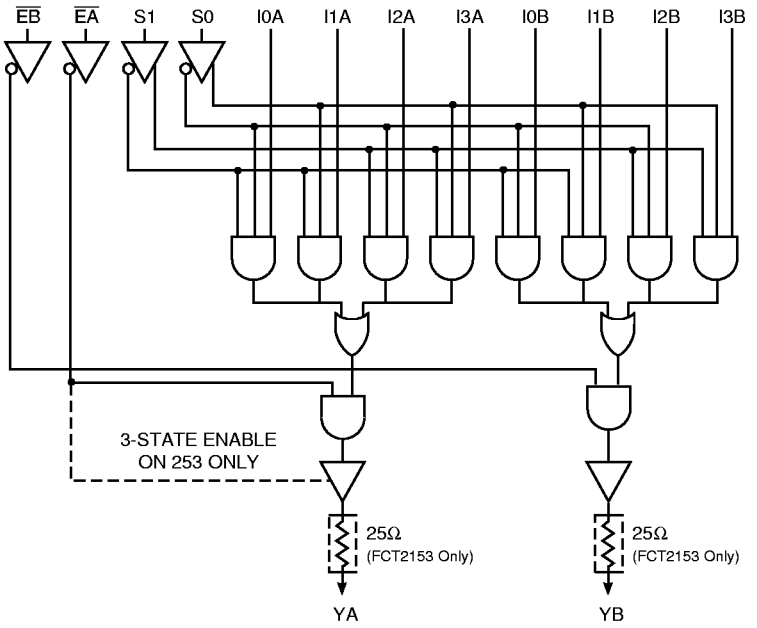
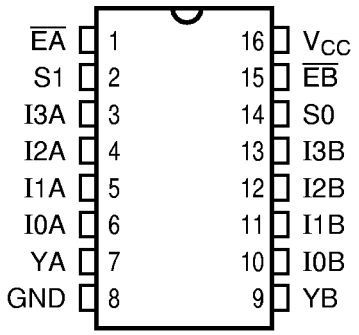
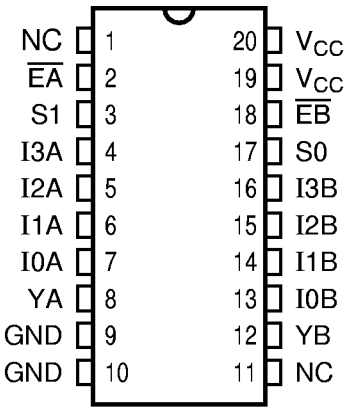


Figure 2. Pin Configurations (All Pins Top View)

PDIP, SOIC, QSOP



HQSOP



Note:
Available in both 150 mil wide SOIC (package code S1) and 300 mil wide SOIC (package code SO).

Table 1. Pin Description

Name	I/O	Description
I7-I0	I	Data In
S1-S0	I	Select
$\overline{EA}$, $\overline{EB}$	I	Enable
YA, YB	O	Data Out

Table 2. Function Table

Enable		Select		153, 2153		253		
$\overline{EA}$	$\overline{EB}$	S1	S0	YA	YB	YA	YB	Function
H	X	X	X	L	X	HI-Z	Z	Disable A
X	H	X	X	X	L	X	HI-Z	Disable B
L	L	L	L	I0A	I0B	I0A	I0B	S1-0 = 0
L	L	L	H	I1A	I1B	I1A	I1B	S1-0 = 1
L	L	H	L	I2A	I2B	I2A	I2B	S1-0 = 2
L	L	H	H	I3A	I3B	I3A	I3B	S1-0 = 3

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Capacitance(1)

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins(2)	SOIC	QSOP	PDIP	Unit
1-6, 10-15	4	4	5	pF
7, 9	8	8	9	pF

Notes:
1. Capacitance is characterized but not tested.
2. Pin reference for 16-pin package.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions(1)	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or V_{CC}-0.2V ≤ V_{IN} ≤ V_{CC}	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0(2)	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}(3,4)	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)(FCT253)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current FCTXXX	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive FCT2153	V_{CC} = Max., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12mA (MIL) I_{OH} = –15mA (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage FCTXXX	V_{CC} = Min., I_{OL} = 32mA (MIL) I_{OL} = 48mA (IND)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage FCT2153 (25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance FCT2153 (25Ω)	V_{CC} = Min., I_{OL} = 12mA (MIL) I_{OL} = 12mA (IND)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

Table 7. Switching Characteristics Over Operating Range

Industrial T_A = –40°C to 85°C, V_{CC} = 5.0V ±5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ±10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		153A 253A 2153A Min	153A 253A 2153A Max	153C 253C Min	153C 253C Max	Unit
t_{IY}	Propagation Delay In to Y, 153/253	Ind Mil	1.5 1.5	5.2 5.8	1.5	4.5	ns
t_{IY}	Propagation Delay In to Y, 2153	Ind Mil	1.5 1.5	5.2 5.8	1.5	4.5	ns
t_{SY}	Propagation Delay Sn to Y, 153/253	Ind Mil	1.5 1.5	6.6 7.4	1.5	5.6	ns
t_{SY}	Propagation Delay Sn to Y, 2153	Ind Mil	1.5 1.5	6.6 7.4	1.5	5.6	ns
t_{OEH} t_{OEL}	Output Enable Time $\overline{E}$ to Yi, 153	Ind Mil	1.5 1.5	5.2 5.8	1.5	4.8	ns
t_{OEH} t_{OEL}	Output Enable Time $\overline{E}$ to Yi, 2153	Ind Mil	1.5 1.5	5.2 5.8	1.5	4.8	ns
t_{PZH} t_{PZL}	Ouput Enable Time $\overline{E}$ to Yi, 253	Ind Mil	1.5 1.5	6.0 6.4	1.5	5.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] $\overline{E}$ to Yi, 253	Ind Mil	1.5 1.5	6 6.3	1.5	5.0	ns

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.