

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for N-CDMA base station applications with frequencies from 1805 to 1880 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

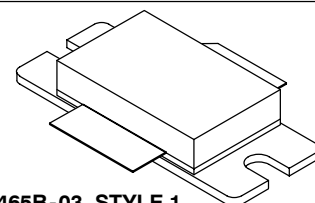
- Typical 2-Carrier N-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1200$ mA, $P_{out} = 29$ Watts Avg., Full Frequency Band, IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
Power Gain — 16 dB
Drain Efficiency — 27.5%
IM3 @ 2.5 MHz Offset — -36 dBc in 1.2288 MHz Bandwidth
ACPR @ 885 kHz Offset — -50.5 dBc in 30 kHz Bandwidth
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 1840 MHz, 140 Watts CW Output Power

Features

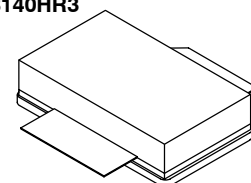
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- Lower Thermal Resistance Package
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- Low Gold Plating Thickness on Leads, 40 μ m Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF6S18140HR3
MRF6S18140HSR3

1805-1880 MHz, 29 W AVG., 28 V
2 x N-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
NI-880
MRF6S18140HR3



CASE 465C-02, STYLE 1
NI-880S
MRF6S18140HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 140 W CW Case Temperature 73°C, 29 W CW	$R_{\theta JC}$	0.31 0.35	°C/W

- Continuous use at maximum temperature will affect MTTF.
- MTTF calculator available at <http://www.freescal Semiconductor.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescal Semiconductor.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 1200\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.8	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3\text{ Adc}$)	$V_{DS(on)}$	0.1	0.22	0.3	Vdc

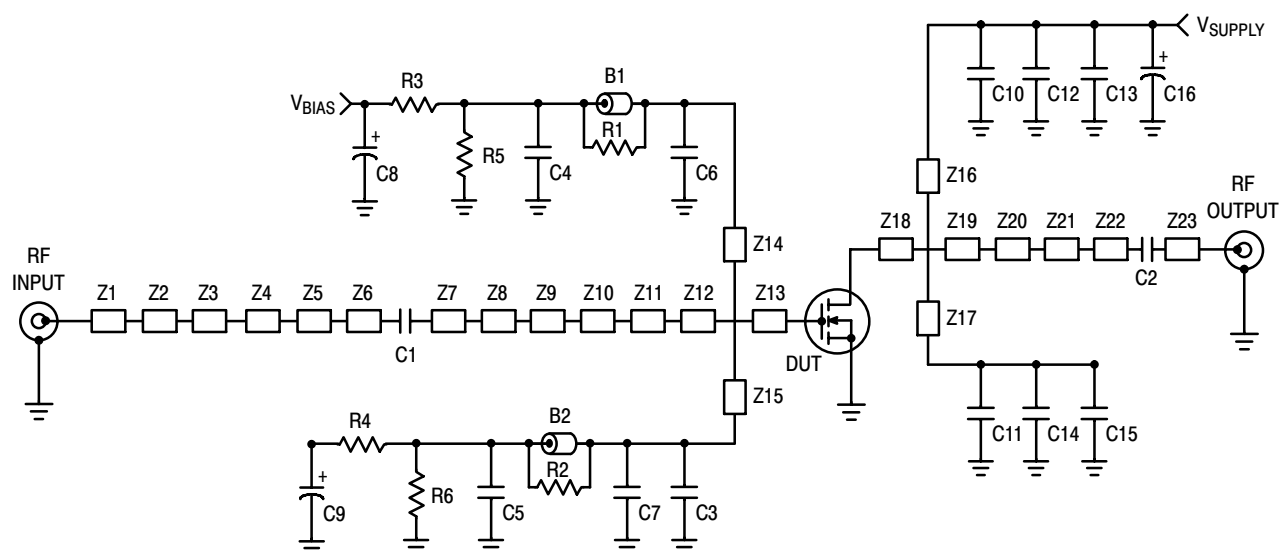
Dynamic Characteristics ⁽¹⁾

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	2.2	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	685	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, $P_{out} = 29\text{ W Avg.}$, $f_1 = 1805\text{ MHz}$, $f_2 = 1807.5\text{ MHz}$ and $f_1 = 1877.5\text{ MHz}$, $f_2 = 1880\text{ MHz}$, 2-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carriers. ACPR measured in 30 kHz Channel Bandwidth @ $\pm 885\text{ kHz}$ Offset. IM3 measured in 1.2288 MHz Channel Bandwidth @ $\pm 2.5\text{ MHz}$ Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	15	16	18	dB
Drain Efficiency	η_D	25.5	27.5	—	%
Intermodulation Distortion	IM3	—	-36	-34.5	dBc
Adjacent Channel Power Ratio	ACPR	—	-50.5	-48	dBc
Input Return Loss	IRL	—	-10.5	—	dB

1. Part internally matched both on input and output.



Z1	0.166" x 0.082" Microstrip	Z13	0.108" x 1.070" Microstrip
Z2	0.250" x 0.334" Microstrip	Z14	0.960" x 0.046" Microstrip
Z3	0.140" x 0.340" Microstrip	Z15	0.084" x 0.046" Microstrip
Z4	0.092" x 0.164" Microstrip	Z16	0.996" x 0.080" Microstrip
Z5	0.130" x 0.234" Microstrip	Z17	1.015" x 0.080" Microstrip
Z6	0.109" x 0.082" Microstrip	Z18	0.099" x 1.070" Microstrip
Z7	0.070" x 0.082" Microstrip	Z19	0.516" x 1.070" Microstrip
Z8	0.350" x 0.644" Microstrip	Z20	0.292" x 0.288" Microstrip
Z9	0.092" x 0.420" Microstrip	Z21	0.198" x 0.114" Microstrip
Z10	0.720" x 0.082" Microstrip	Z22	0.372" x 0.080" Microstrip
Z11	0.090" x 0.485" x 0.580" Taper	Z23	1.181" x 0.080" Microstrip
Z12	0.342" x 1.070" Microstrip	PCB	DS Electronics GX0300, 0.030", $\epsilon_r = 2.55$

Figure 1. MRF6S18140HR3(HSR3) Test Circuit Schematic

Table 5. MRF6S18140HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	47 Ω , 100 MHz Small Ferrite Beads, Surface Mount	2743019447	Fair-Rite
C1, C2	39 pF Chip Capacitors	700B390FW500XT	ATC
C3	0.1 pF Chip Capacitor	100B0R1BP500X	ATC
C4, C5, C12, C13, C14, C15	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C6, C7, C10, C11	9.1 pF Chip Capacitors	600B9R1BT250XT	ATC
C8, C9	47 μ F, 50 V Electrolytic Capacitors	MVK50VC47RM8X10TP	United Chemi-Con
C16	470 μ F, 63 V Electrolytic Capacitor	NACZF471M63V	Nippon Chemi-Con
R1, R2	12 Ω , 1/8 W Resistors	CRCW120612R0F100	Dale/Vishay
R3, R4	1.0 K Ω , 1/8 W Resistors	CRCW12061001F100	Dale/Vishay
R5, R6	560 K Ω , 1/8 W Chip Resistors	CRCW12065602F101	Dale/Vishay

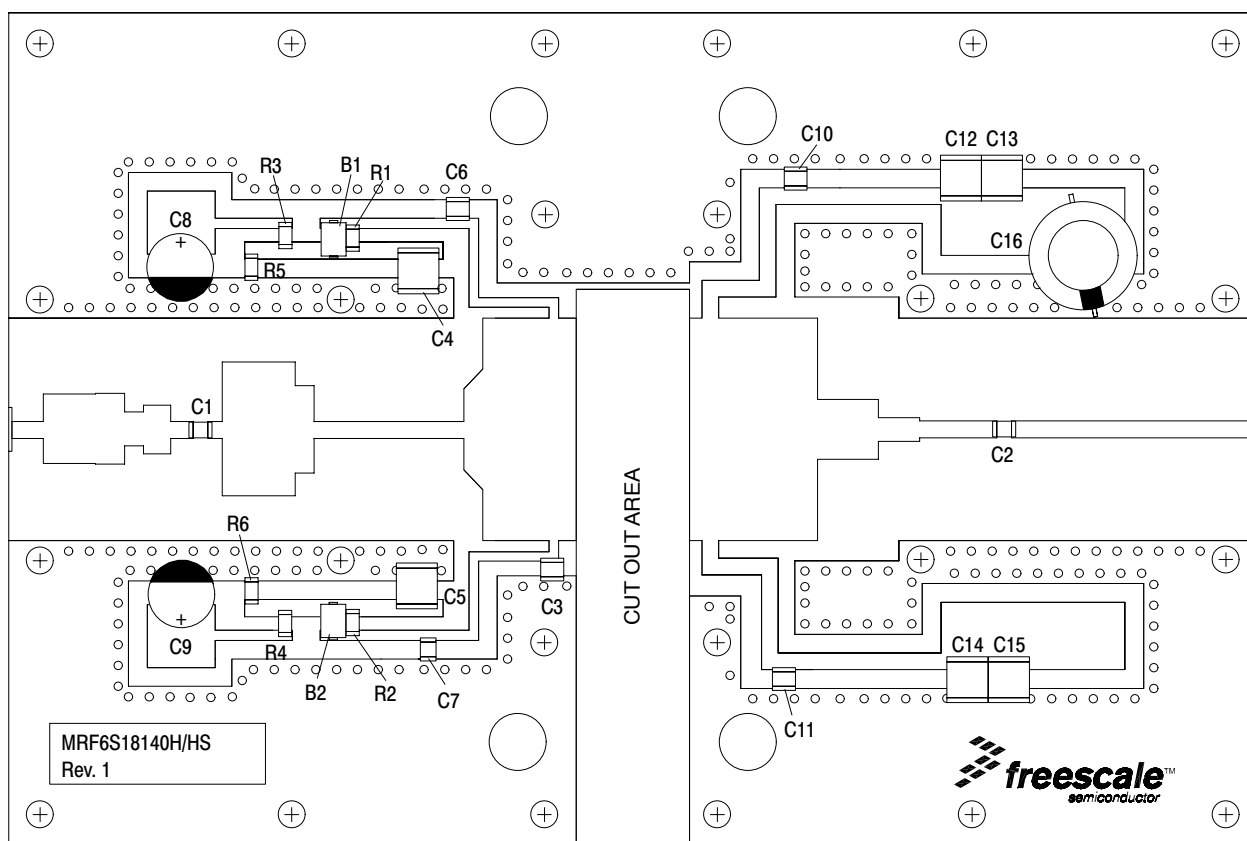


Figure 2. MRF6S18140HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

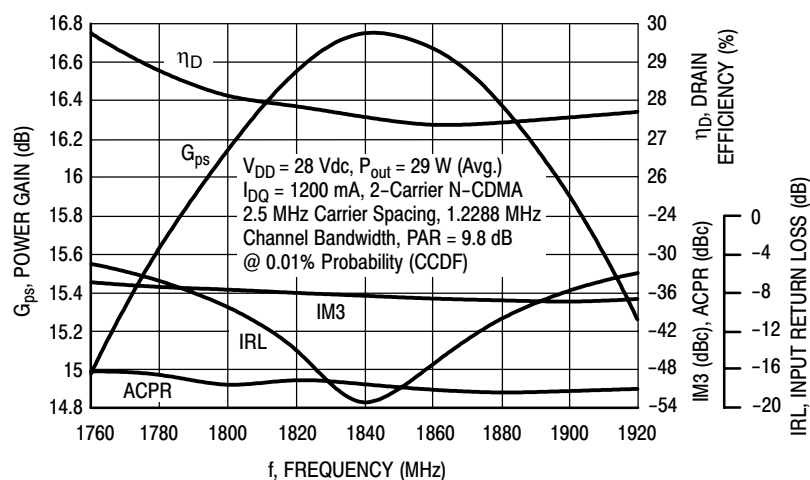


Figure 3. 2-Carrier N-CDMA Broadband Performance @ $P_{out} = 29$ Watts Avg.

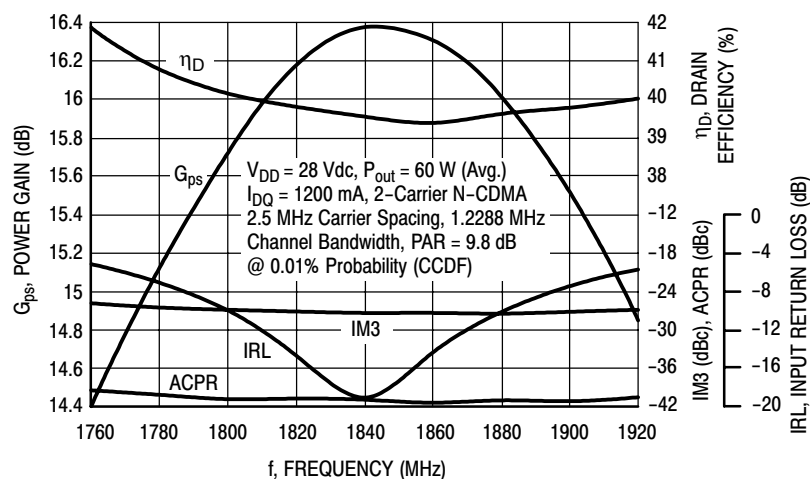


Figure 4. 2-Carrier N-CDMA Broadband Performance @ $P_{out} = 60$ Watts Avg.

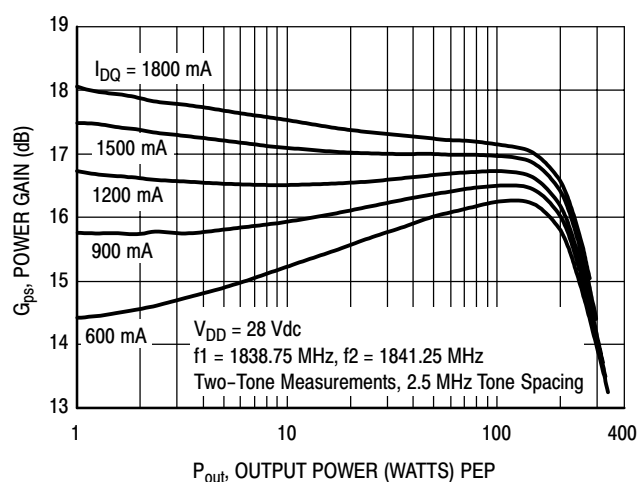


Figure 5. Two-Tone Power Gain versus Output Power

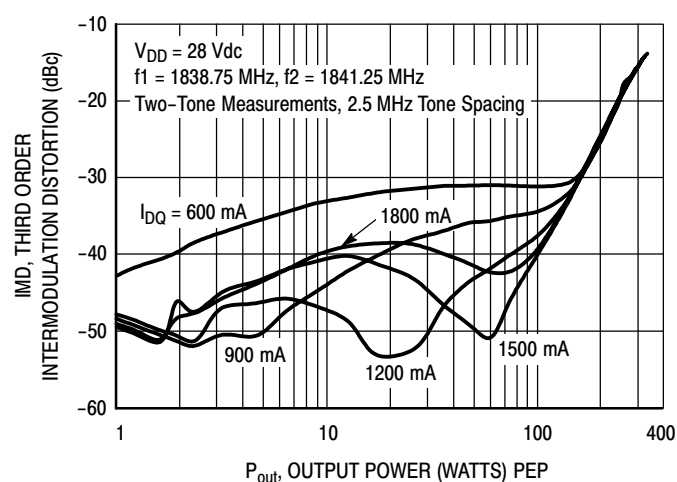


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

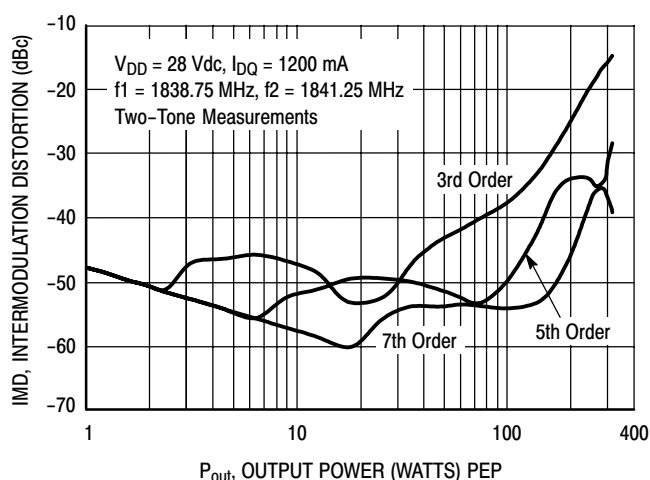


Figure 7. Intermodulation Distortion Products versus Output Power

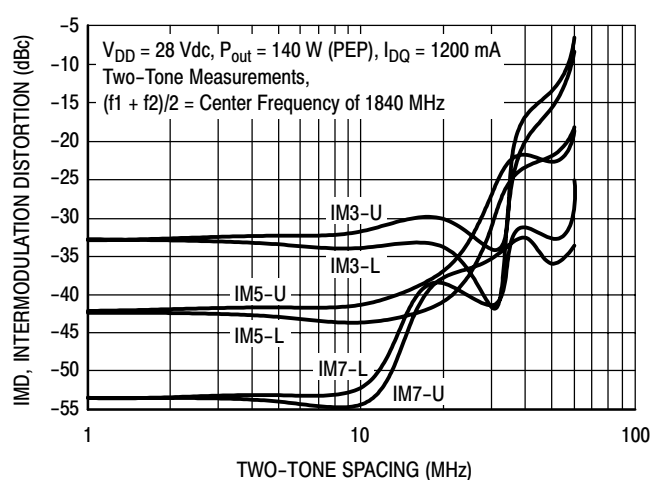


Figure 8. Intermodulation Distortion Products versus Tone Spacing

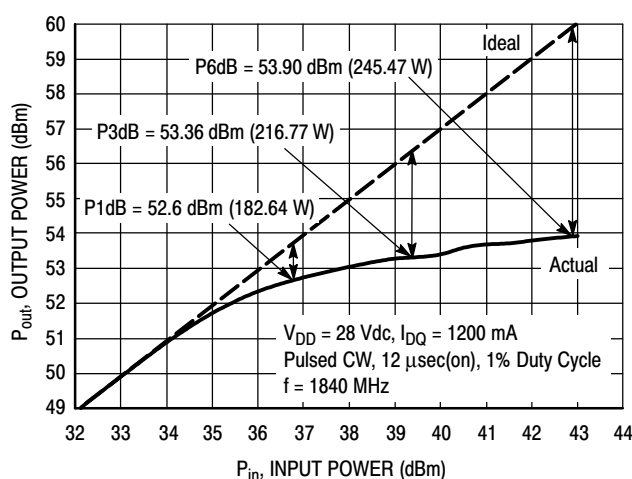


Figure 9. Pulsed CW Output Power versus Input Power

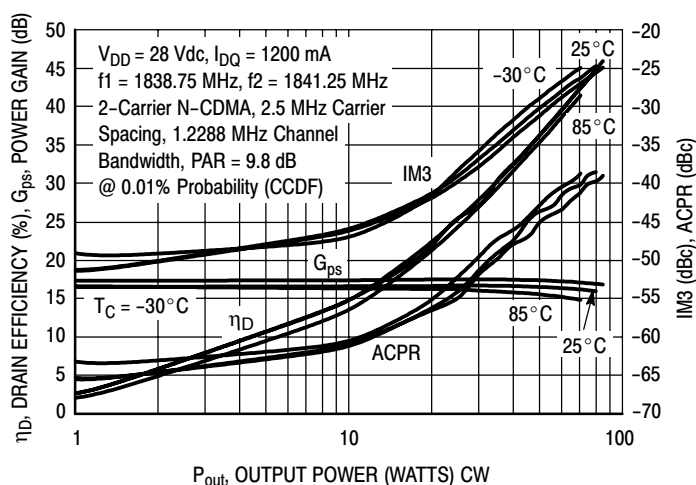


Figure 10. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

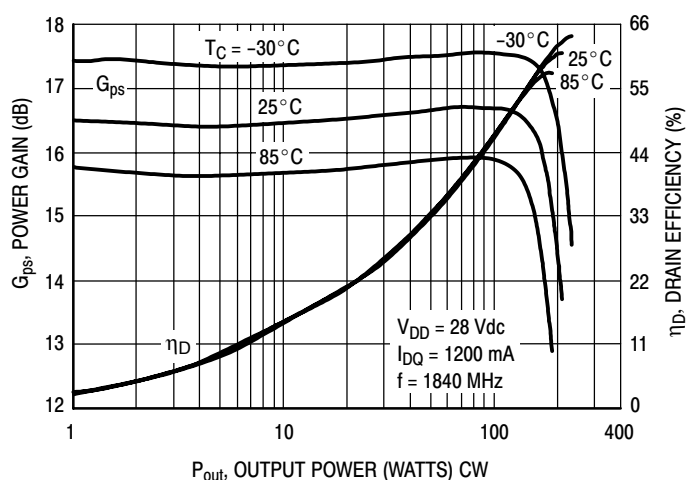


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

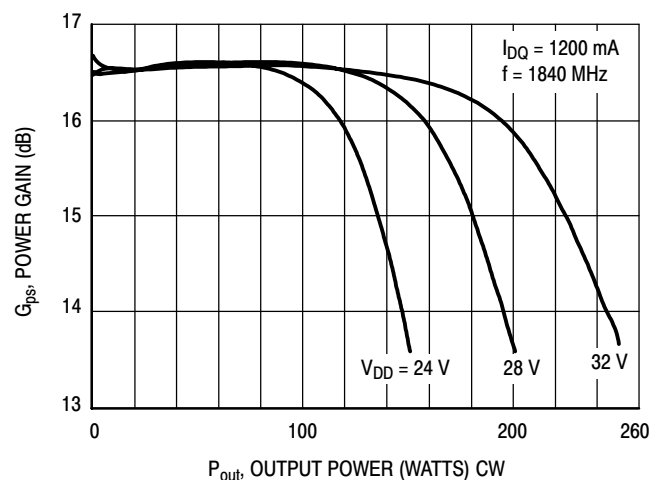
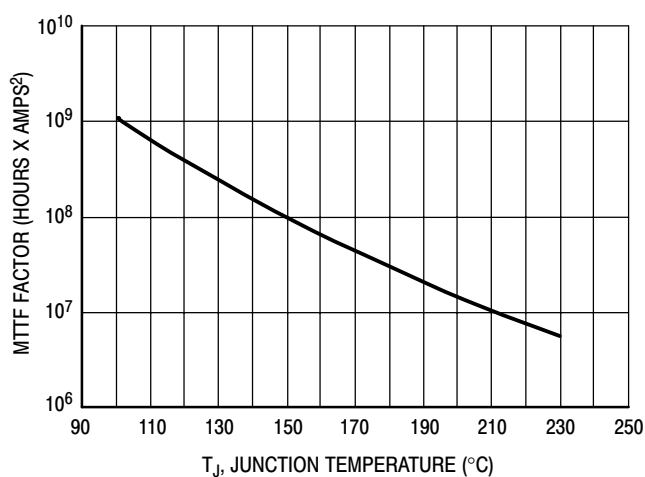


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 13. MTTF Factor versus Junction Temperature

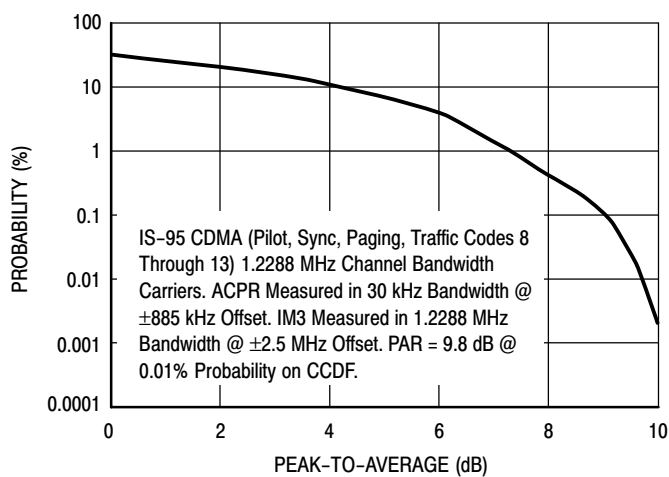


Figure 14. 2-Carrier CCDF N-CDMA

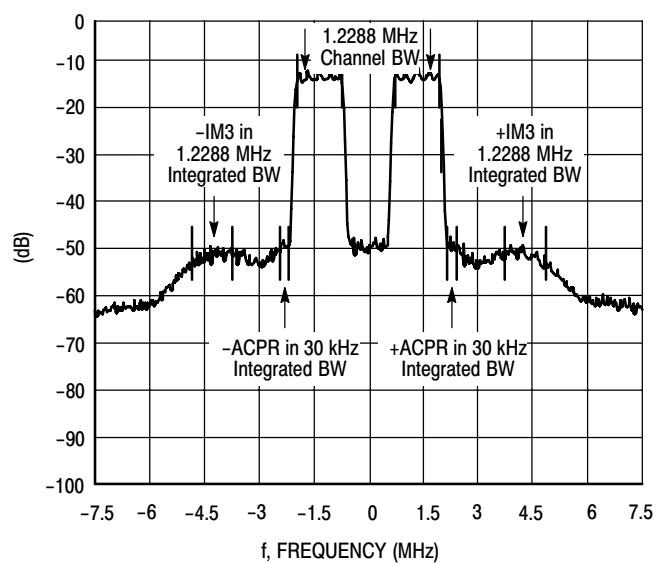
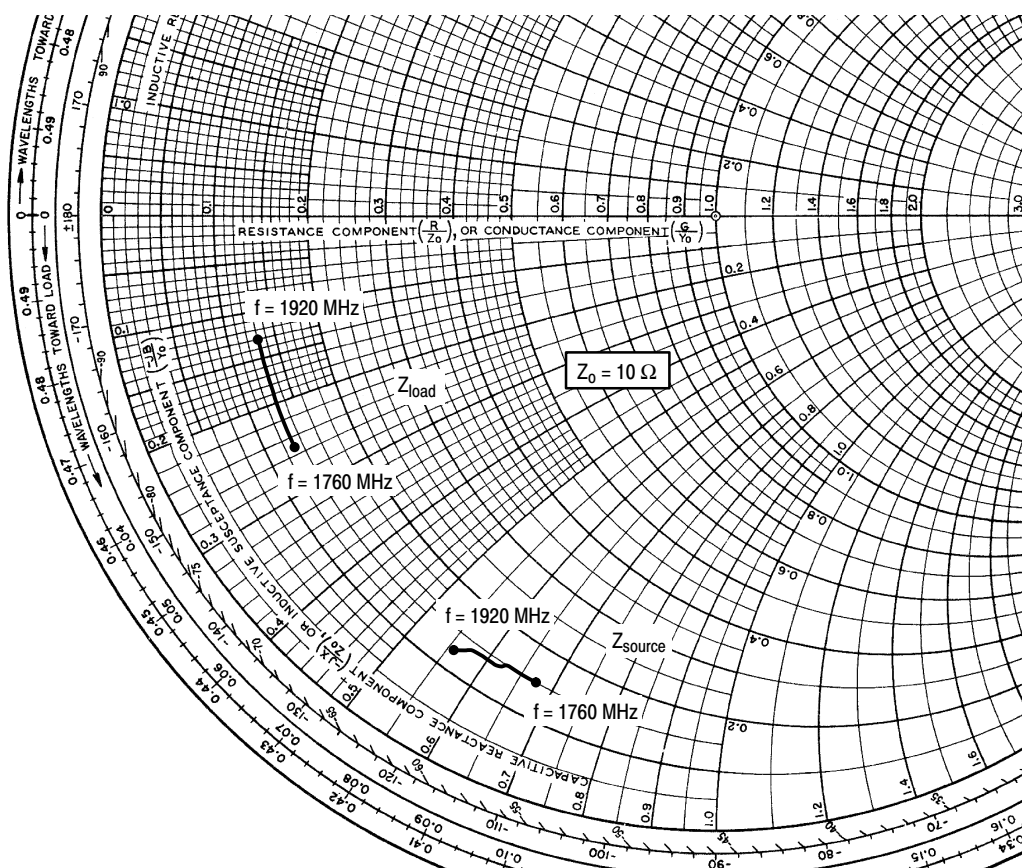


Figure 15. 2-Carrier N-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1200 \text{ mA}$, $P_{out} = 29 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1760	$1.454 - j6.703$	$1.344 - j2.479$
1780	$1.465 - j6.511$	$1.338 - j2.299$
1800	$1.467 - j6.336$	$1.333 - j2.129$
1820	$1.448 - j6.193$	$1.325 - j1.966$
1840	$1.440 - j6.049$	$1.308 - j1.801$
1860	$1.414 - j5.938$	$1.301 - j1.687$
1880	$1.377 - j5.827$	$1.303 - j1.550$
1900	$1.311 - j5.710$	$1.301 - j1.419$
1920	$1.231 - j5.583$	$1.289 - j1.303$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

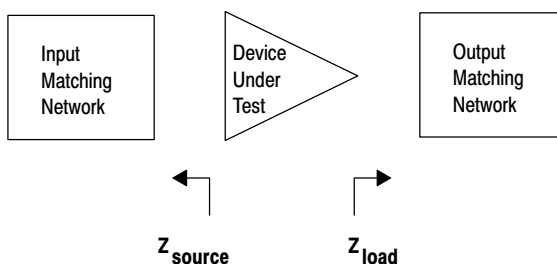
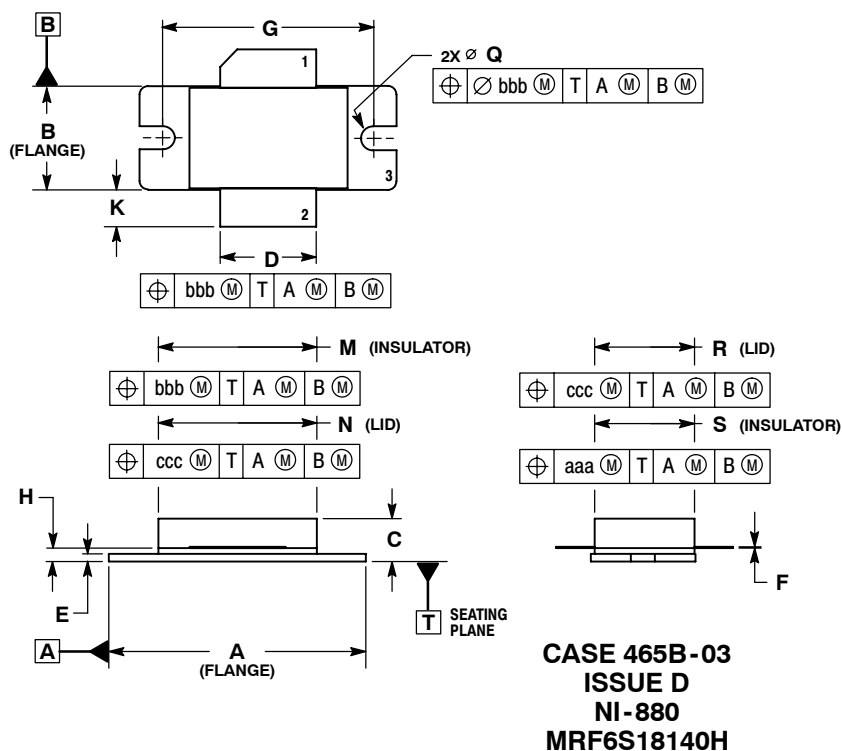


Figure 16. Series Equivalent Source and Load Impedance

MRF6S18140HR3 MRF6S18140HSR3

PACKAGE DIMENSIONS



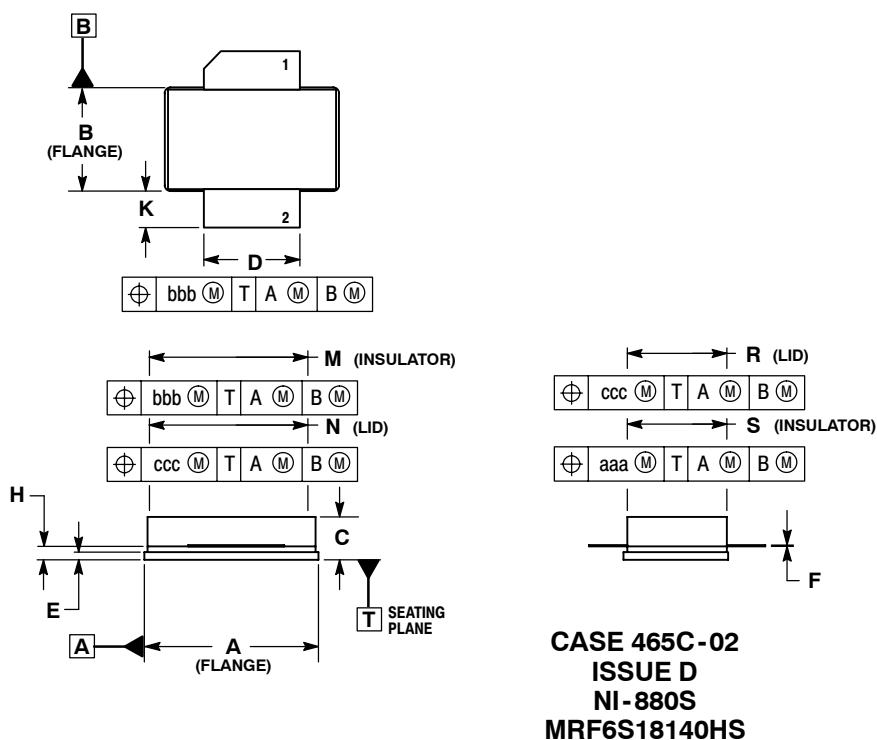
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. DELETED

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100	BSC	27.94	BSC
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	$\varnothing$.118	$\varnothing$.138	$\varnothing$ 3.00	$\varnothing$ 3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007	REF	0.178	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007	REF	0.178	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Date	Revision Number	Description
Sept. 2006	0	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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