HD66132T

(240-Channel HI-FAS Segment Driver for Dot-Matrix Graphic LCD Display)

HITACHI

Rev 0.6
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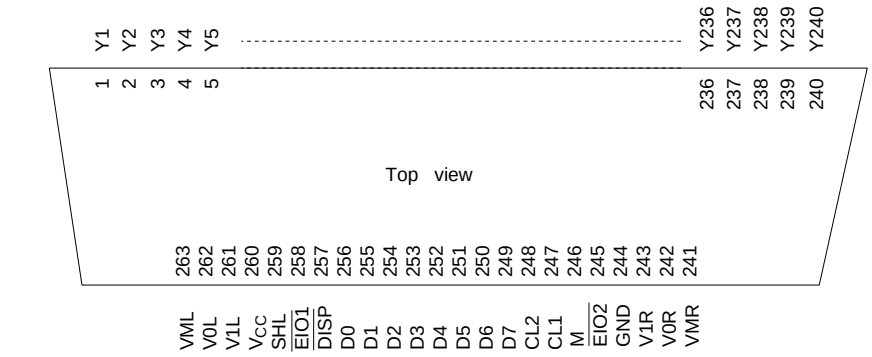
Description

The HD66132T is a 240-channel segment driver, which drives a dot matrix liquid crystal graphic system with HI-FAS (high-frequency-amplitude selection). The HD66132T operates with low voltages of 5-V LCD drive voltage and 3.3-V logic drive voltage, and therefore, its low current consumption characteristics of liquid crystal cells can be effectively used. The HD66132T, packaged in a fine-pitch slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area.

Features

- HI-FAS drive method
- Duty cycle: Up to 1/300
- LCD drive voltage: 5.5V max
- 240 LCD drive circuits
- Operating voltage: 3.5 to 5.5V
- Eight data bits
- Shift clock speed
  - 25 MHz max/3V
  - 40 MHz max/5V
- Display off function
- Slim TCP
- Output lead pitch: 70 to 93 µm
- User area: 5.5 to 6.66 mm
- Chip enable signal automatic generation
- Standby function

Pin Arrangement



Note: This figure does not specify the tape carrier package dimension.

Figure 1 Pin Arrangement

Block Diagram

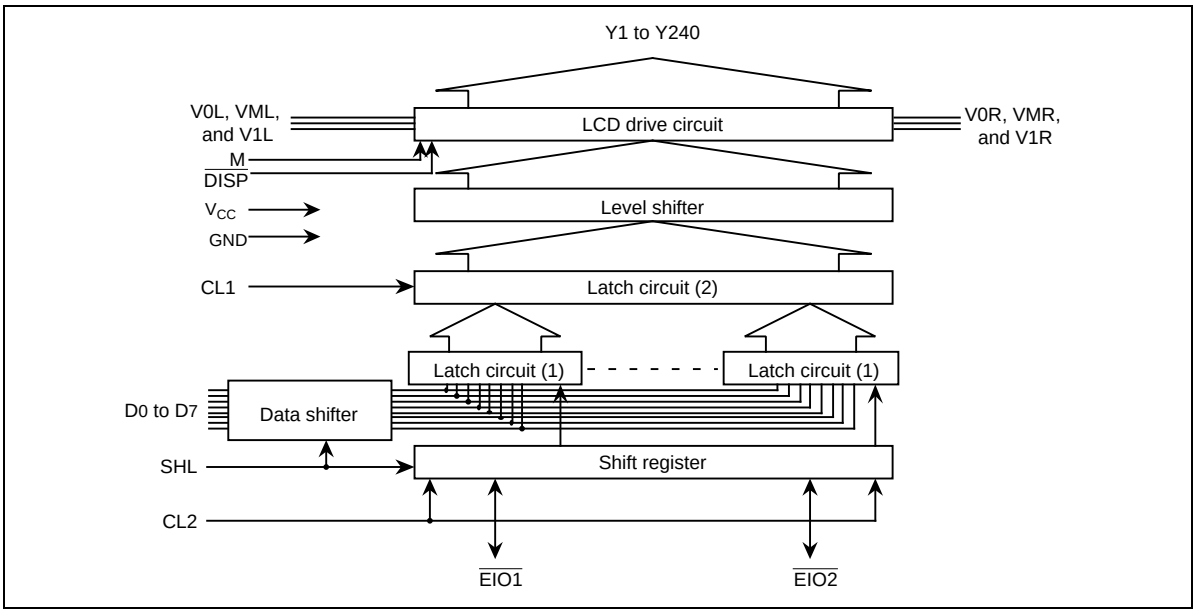


Figure 2 Block Diagram

Block Functions

LCD Drive Circuit

The 240-bit LCD drive circuit generates three voltage levels VH, VL, and VM, which drive the LCD panel. One of these three levels is output to the corresponding Y pin, depending on the $\overline{DISP}$ signal and the combination of the M signal and the data in latch circuit (2).

Level Shifter

The level shifter changes logic control signals into LCD drive signals.

Latch Circuit (2)

240-bit latch circuit (2) latches data input from latch circuit (1), and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit (1)

240-bit latch circuit (1) latches 8-bit parallel data input via the D0 to D7 pins, and outputs the latched data to latch circuit 2, both at the timing generated by the shift register.

Shift Register

The 30-bit shift register generates and outputs data latch signals for latch circuit (1) at the falling edge of each clock 2 (CL2) pulse.

Data Shifter

The data shifter shifts the destinations of data output, when necessary.

Pin Function

Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Power supply	V_{CC} GND	260 244	V_{CC} GND	—	V_{CC}–GND: Logic power supply
	V0L, V0R VML, VMR V1L, V1R	262, 242 263, 241 261, 243	V0L, V0R VML, VMR V1L, V1R	Input	LCD drive level voltage. See Figure 3.
Control signal	CL1	247	Clock 1	Input	Display data latch signal. The LCD drive signal corresponding to display data is output at the falling edge of this signal.
	CL2	248	Clock 2	Input	Display data latch signal. Display data is latched at the falling edge of this signal.
	M	246	M	Input	Changes the LCD drive outputs to AC.
	D0 to D7	256 to 249	Data0 to Data7	Input	When display data is 1 (V_{CC} level), the LCD drive output level is selection level and the liquid crystal display is on, and when 0 (GND level), they are non-selection level and off, respectively.
	SHL	259	Shift left	Input	A control signal to switch the data output destination. See the section of Switching Data Output Destination.
	$\overline{EIO1}$	258	Enable I/O 1	Input/ output	If SHL is V_{CC} level, $\overline{EIO2}$ inputs the chip enable signal and $\overline{EIO1}$ outputs the chip enable signal, and if it is GND level, vice versa Enable input: The chip enable input pin of the first HD66132T must be fixed to GND level, and the rest of chip enable input pins must be connected to the chip enable output pins of he previous HD66132T Enable output: The chip enable output pin must be connected to the chip enable input pin of the next HD66132T.
	$\overline{EIO2}$	245	Enable I/O 2	Input/ output	
	$\overline{DISP}$	257	Disp off	Input	A low $\overline{DISP}$ level sets LCD drive outputs Y1 to Y240 to VM level.
LCD drive output	Y1 to Y240	1 to 240	Y1 to Y240	Output	Either of two levels V0 and V1 is output according to the combination of the M signal and display data when the $\overline{DISP}$ pin is set at V_{CC}. See Figure 4.

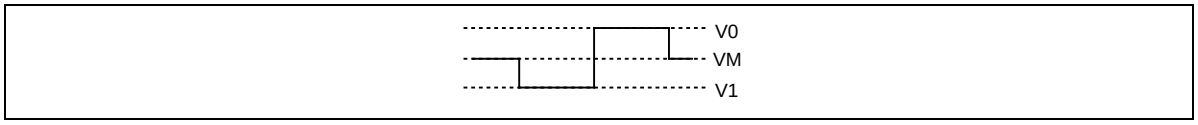


Figure 3 LCD Drive Level Voltage

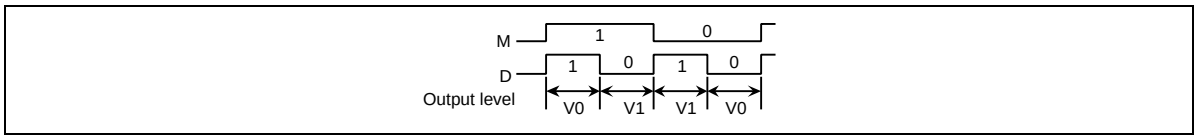


Figure 4 Selection of LCD Drive Output Level

Switching Data Output Destination

The output destination of data latched by the SHL signal is switched (left or right). At this time, input and output of enable signal pins can also be switched. See Figure 5.

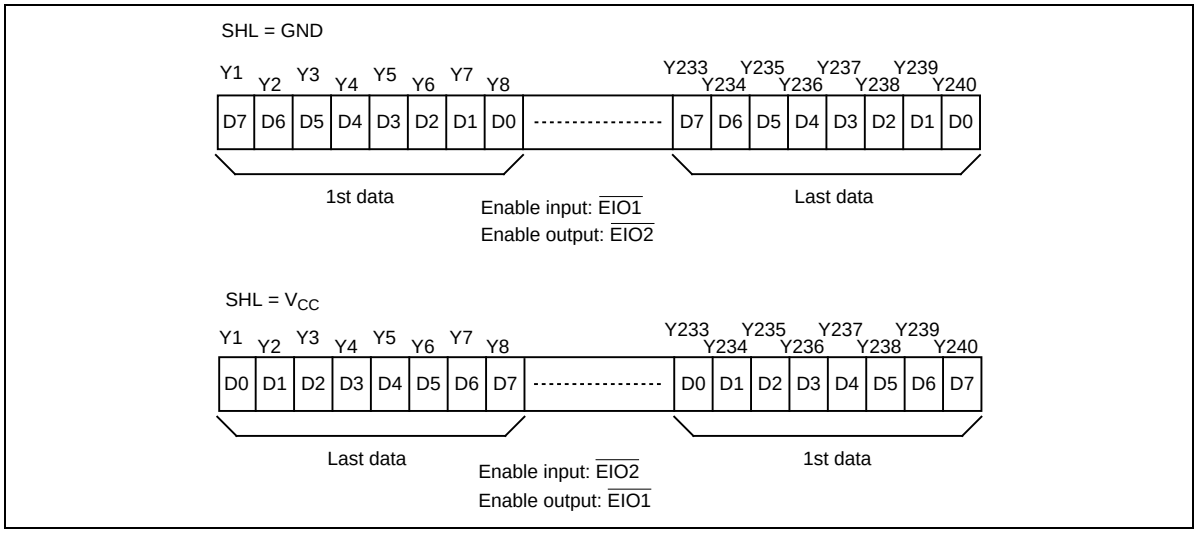


Figure 5 Data Output Destination

Operation Timing

Figure 6 shows 8-bit data latch timing when SHL = GND, that is, the $\overline{EIO1}$ pin is a chip enable input and $\overline{EIO2}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EIO1}$ pin is a chip enable output and $\overline{EIO2}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{EIO1}$ pin, the HD66132T is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data.

It simultaneously latches eight bits of data at the falling edge of each CL2 pulse. When it has latched 232 bits of data, it sets the $\overline{EIO2}$ signal low. When it has latched 240 bits of data, it automatically stops and enters standby state, initiating the next HD66132T, as long as its $\overline{EIO2}$ pin is connected to the $\overline{EIO1}$ pin of the next HD66132T.

The HD66132Ts output one line of data from the Y1 to Y240 pins at the falling edge of each CL1 pulse. Data d1 is output from Y1, and d240 from Y240 when SHL = GND, and d1 is output from Y240, and d240 from Y1 when SHL = V_{CC}.

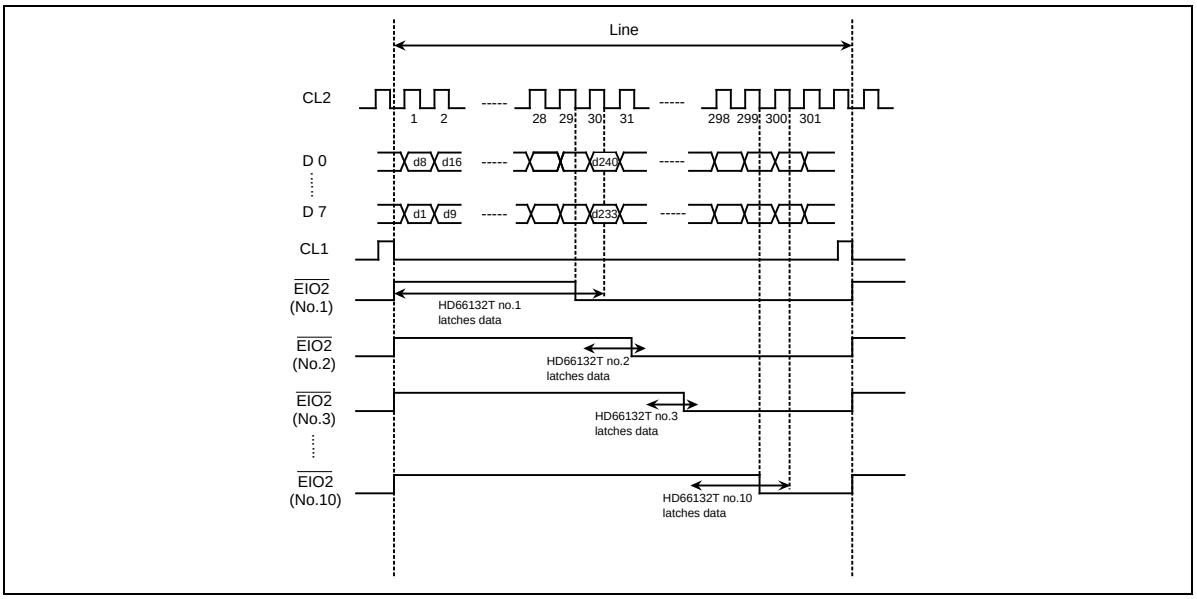


Figure 6 Data Latch Timing

Application Example

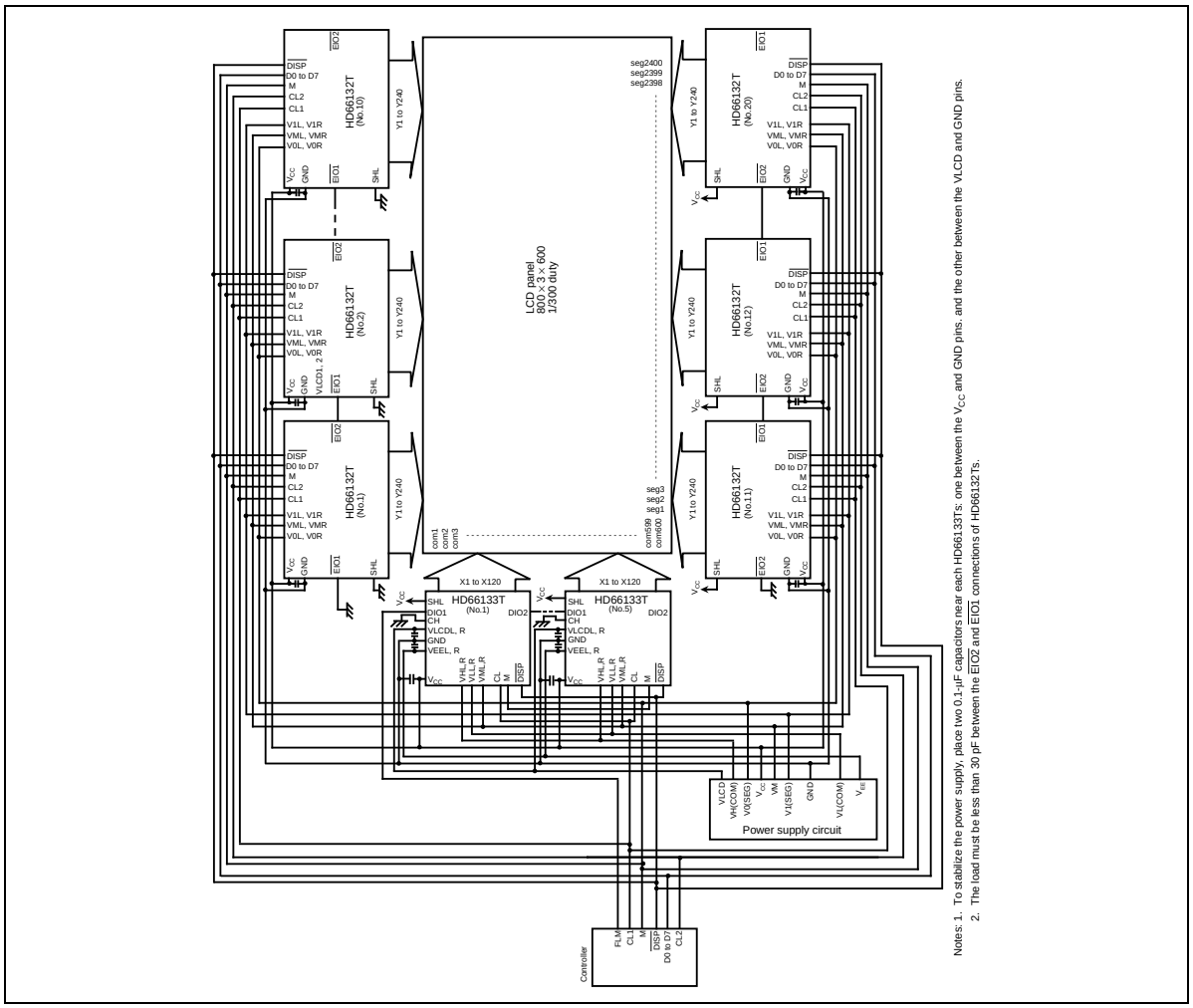


Figure 7 Application Example

Absolute Maximum Ratings[*1]

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	2 and 5
	LCD drive circuit	VLCD	–0.3 to +7.0	V	2 and 5
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	2 and 3
Input voltage (2)		VT2	–0.3 to V0 + 0.3	V	2 and 4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

2. The reference point is GND (0V).
3. Applies to logic circuit input pins.
4. Applies to the VML, VMR, VIL, and VIR pins
5. Power should be applied to V_{CC}–GND first, and then GND–V0, and should be cut off in GND–V0 first, and then GND–V_{CC}.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.7 to 4.5V, V0–GND = 3.5 to 5.5V, and Ta = –20 to +75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	VIH	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, and D0 to D7	0.7 × V_{CC}	—	V_{CC}	V		
Input low level voltage	VIL		0	—	0.3 × V_{CC}	V		
Output high level voltage	VOH	$\overline{EIO1}$ and $\overline{EIO2}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	VOL	$\overline{EIO1}$ and $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj ON resistance	R_{ON}	Y1 to Y240, V0L, and V0R	—	0.5	1.0	kΩ	I_{ON} = 150 µA	1
		Y1 to Y240, VML, and VMR	—	1.0	2.0	kΩ		
		Y1 to Y240, V1L, and V1R	—	0.5	1.0	kΩ		
Input leakage current (1)	I_{IL1}	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, and D0 to D7	–5	—	5	µA	VIN = V_{CC}–GND	
Input leakage current (2)	I_{IL2}	VML, VMR, V1L, and V1R	–100	—	25	µA	VIN = V0–GND	
Current consumption (1)	I_{CC}	V_{CC}	—	—	TBD	mA	V_{CC} = 3.0 V f_{CL2} = 25 MHz f_{CL1} = 100 kHz f_M = 75 Hz	2
Current consumption (2)	I_{V0}	V0L and V0R	—	—	TBD	mA		
Current consumption (3)	I_{ST}	V_{CC}	—	—	TBD	mA		2 and 3

DC Characteristics 2 (V_{CC} = 2.7 to 4.5V, V0–GND = 3.5 to 5.5V, and Ta = –20 to +75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	VIH	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, and D0 to D7	0.7 × V_{CC}	—	V_{CC}	V		
Input low level voltage	VIL		0	—	0.3 × V_{CC}	V		
Output high level voltage	VOH	$\overline{EIO1}$ and $\overline{EIO2}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	VOL	$\overline{EIO1}$ and $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj ON resistance	R_{ON}	Y1 to Y240, V0L, and V0R	—	0.5	1.0	kΩ	I_{ON} = 150 µA	1
		Y1 to Y240, VML, and VMR	—	1.0	.	kΩ		
		Y1 to Y240, V1L, and V1R	—	0.5	1.0	kΩ		
Input leakage current (1)	I_{IL1}	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, and D0 to D7	–5	—	5	µA	VIN = V_{CC} –GND	
Input leakage current (2)	I_{IL2}	VML, VMR, V0L, and V0R	–100	—	100	µA	VIN = V0–GND	
Current consumption (1)	I_{CC}	V_{CC}	—	—	TBD	mA	V_{CC} = 5.0V f_{CL2} = 40 MHz f_{CL1} = 160 kHz f_M = 75 Hz	2
Current consumption (2)	I_{V0}	V0L and V0R	—	—	TBD	mA		
Current consumption (3)	I_{ST}	V_{CC}	—	—	TBD	mA		2 and 3

Notes: 1 Indicates the resistance between one of the pins Y1–Y240 and one of the voltage supply pins, when load current is applied to the Y pin; defined under the following conditions:

V0–GND = 6V

VM = (VLCD–GND)/2

V1 = GND + 1

V1 should be near the GND level, and the VM should be near the middle voltage between V1 and V0. 1 should be within the range of ΔV = 3 V0, which is the range within which RON, the LCD drive circuit's output impedance, is stable. See Figure 8.

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, VIH and VIL must be held at V_{CC} and GND, respectively.
3. Standby current.

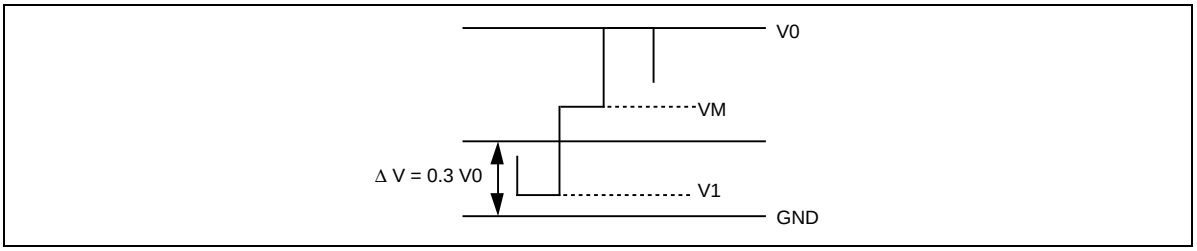


Figure 8 Relationship between Driver Output Waveforms and Each Level Voltage

AC Characteristics 1 (V_{CC} = 2.7 to 4.5V, V0–GND = 3.5 to 5.5V, and Ta = –20 to +75 °C, unless otherwise stated)[*1]

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	40	—	ns	
Clock high level width (1)	t_{CWH2}	CL2	15	—	ns	
Clock low level width (1)	t_{CWL2}	CL2	15	—	ns	
Clock high level width (2)	t_{CWH1}	CL1	25	—	ns	
Clock setup time	t_{SCL}	CL1 and CL2	100	—	ns	
Clock hold time	t_{HCL}	CL1 and CL2	100	—	ns	
Clock rise time	t_r	CL1 and CL2	—	30	ns	2
Clock fall time	t_f	CL1 and CL2	—	30	ns	2
Data setup time	t_{DS}	D0 to D7, and CL2	10	—	ns	
Data hold time	t_{DH}	D0 to D7, and CL2	10	—	ns	
M phase difference	t_{CM}	M	—	300	ns	
Output delay time (1)	t_{pd1}	CL1, and Y1 to Y240	—	500	ns	
Output delay time (2)	t_{pd2}	M, and Y1 to Y240	—	500	ns	

Notes: 1. The load must be less than 30 pF between $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66132Ts.

2. Clock rise time (t_r) and clock fall time (t_f) must satisfy the following condition:
   t_r and $t_f < (t_{CYC} – t_{CWH2} – t_{CWL2})/2$ (1)
   t_r and $t_f \leq 30$ ns

AC Characteristics 2 (V_{CC} = 4.5 to 5.5V, V0–GND = 4.5 to 5.5V, and Ta = –20 to +75 °C, unless otherwise stated)[*1]

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	25	—	ns	
Clock high level width (1)	t_{CWH2}	CL2	10	—	ns	
Clock low level width (1)	t_{CWL2}	CL2	10	—	ns	
Clock high level width (2)	t_{CWH1}	CL1	25	—	ns	
Clock setup time	t_{SCL}	CL1 and CL2	100	—	ns	
Clock hold time	t_{HCL}	CL1 and CL2	100	—	ns	
Clock rise time	t_r	CL1 and CL2	—	20	ns	2
Clock fall time	t_f	CL1 and CL2	—	20	ns	2
Data setup time	t_{DS}	D0 to D7, and CL2	6	—	ns	
Data hold time	t_{DH}	D0 to D7, and CL2	6	—	ns	
M phase difference	t_{CM}	M	—	300	ns	
Output delay time (1)	t_{pd1}	CL1, and Y1 to Y240	—	500	ns	
Output delay time (2)	t_{pd2}	M, and Y1 to Y240	—	500	ns	

Notes: 1. The load must be less than 30 pF between $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66132Ts.

2. Clock rise time (t_r) and clock fall time (t_f) must satisfy the following condition:
   t_r and $t_f < (t_{CYC} – t_{CWH2} – t_{CWL2})/2$
   t_r and $t_f \leq 20$ ns

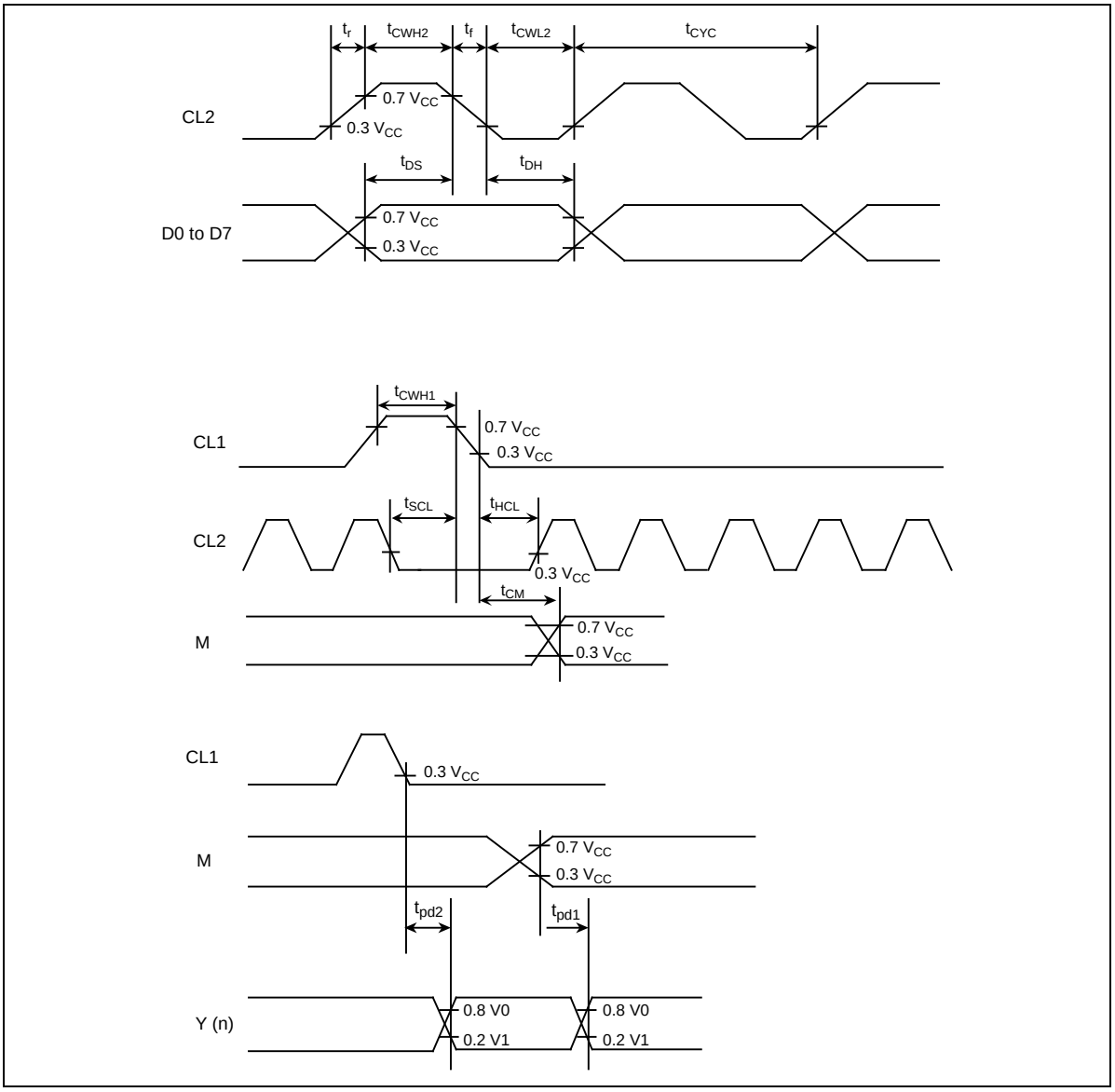


Figure 9 AC Characteristics