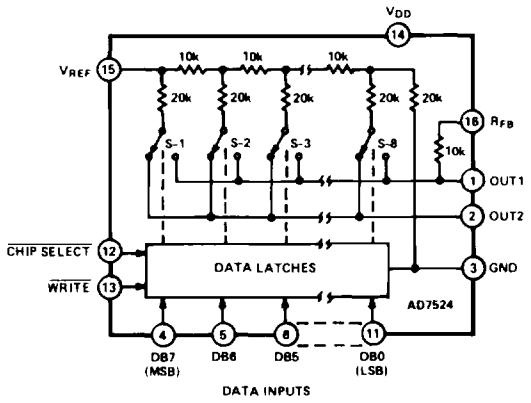
CMOS 8-Bit Buffered Multiplying DAC

AD7524

FEATURES
- Microprocessor Compatible (6800, 8085, Z80, etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- Endpoint Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

APPLICATIONS
- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

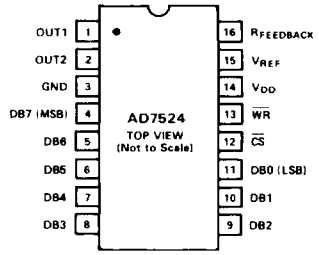
Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5 V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5 V to +15 V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Nonlinearity (V_{DD} = +15 V)	Package Option[2]
AD7524JN	40°C to +85°C	±1/2 LSB	N-16
AD7524KN	40°C to +85°C	±1/4 LSB	N-16
AD7524LN	–40°C to +85°C	±1/8 LSB	N-16
AD7524JP	–40°C to +85°C	±1/2 LSB	P-20A
AD7524KP	–40°C to +85°C	±1/4 LSB	P-20A
AD7524LP	40°C to +85°C	±1/8 LSB	P-20A
AD7524JR	40°C to +85°C	±1/2 LSB	R-16A
AD7524AQ	–40°C to +85°C	±1/2 LSB	Q-16
AD7524BQ	–40°C to +85°C	±1/4 LSB	Q-16
AD7524CQ	–40°C to +85°C	±1/8 LSB	Q-16
AD7524SQ	–55°C to +125°C	±1/2 LSB	Q-16
AD7524TQ	–55°C to +125°C	±1/4 LSB	Q-16
AD7524UQ	55°C to +125°C	±1/8 LSB	Q-16
AD7524SE	55°C to +125°C	±1/2 LSB	E-20A
AD7524TE	55°C to +125°C	±1/4 LSB	E-20A
AD7524UE	55°C to +125°C	±1/8 LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7524—SPECIFICATIONS (V_{REF} = +10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise noted)

Parameter	Limit, T_A = +25°C V_{DD} = +5 V	Limit, T_A = +25°C V_{DD} = +15 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = 5 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = +15 V	Units	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC Measured from +25°C to T_{MIN} or from +25°C to T_{MAX}
DC Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100 Ω, C_{EXT} = 13 pF; $\overline{WR}$, $\overline{CS}$ = 0 V; DB0–DB7 = 0 V to V_{DD} to 0 V.
AC Feedthrough[4]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10 V, 100 kHz Sine Wave; DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R_{IN} (Pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (Pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	30	30	30	30	pF max	
C_{OUT1} (Pin 1)	30	30	30	30	pF max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement						
V_{IL}	+0.8	+1.5	+0.5	+1.5	V max	
Input Current						
I_{IN}	±1	±1	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0 V
WR, CS	20	20	20	20	pF max	V_{IN} = 0 V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[3]						See Timing Diagram
t_{CS}						$t_{WR} = t_{CS}$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	µA max	All Digital Inputs 0 V or V_{DD}

NOTES

[1]Temperature ranges as follows: J, K, L versions: –40°C to +85°C.
A, B, C versions: –40°C to +85°C.
S, T, U versions: –55°C to +125°C.

[2]Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.

[3]Guaranteed not tested.

[4]DAC thin-film resistor temperature coefficient is approximately –300 ppm/°C.

[5]AC parameter, sample tested at +25°C to ensure conformance to specification.

Specifications subject to change without notice.