REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, change t_H on page 6. Editorial changes throughout.	1988 NOV 10	M.A. Frye

REV																								
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REV																								
SHEET																								
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A					A		A								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 18 NOVEMBER 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, QUAD BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-87707
A	67268	

SHEET 1 OF 17

DESC FORM 193
SEP 87

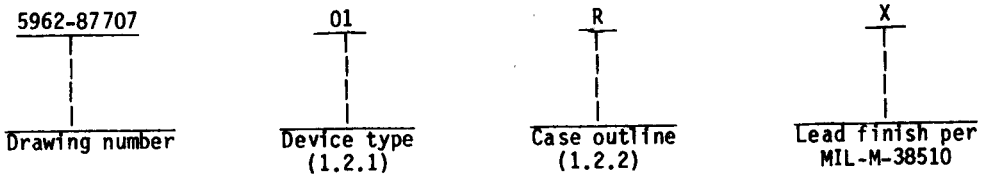
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1005

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example.



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2907	Quad bus transceiver with interface logic and 2.0 V input receiver threshold

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation P_D (1/)	1.1 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}): Cases R, S, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C
DC input current	-30 mA to 5.0 mA
DC output current into bus	200 mA
DC output current into outputs (except bus)	30 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
BUS INPUT/OUTPUT PARAMETERS							
Output low voltage bus	V_{OL}	V_{CC} = 4.5 V $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 40 mA	1,2,3		0.5	V
			I_{OL} = 70 mA			0.7	V
			I_{OL} = 100 mA			0.8	V
Input high voltage (receiver)	V_{TH}	Bus enable = 2.4 V 1/		1,2,3	2.4		V
Input low voltage (receiver)	V_{TL}	Bus enable = 2.4 V 1/		1,2,3		1.5	V
Bus leakage current	I_O	V_{CC} = 5.5 V	V_O = 0.4 V	1,2,3		-50	µA
			V_O = 4.5 V			200	µA
Bus leakage current (power off)	I_{OFF}	V_{CC} = 0 V, V_{OUT} = 4.5 V		1,2,3		100	µA
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_N = -18 mA		1,2,3		-1.2	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
DC PARAMETERS							
Output high voltage receiver	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.0 mA V_{IN} = V_{IL} or V_{IH}		1,2,3	2.4		V
Output high voltage parity	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -660 µA V_{IN} = V_{IL} or V_{IH}		1,2,3	2.5		V
Output low voltage (except bus)	V_{OL}	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH} $\overline{BE}$ = 2.4 V	I_{OL} = 4.0 mA	1,2,3		0.4	V
			I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 12.0 mA			0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA		1,2,3		-1.2	V
Input high current	I_{IH}	V_{CC} = 5.5 V	V_{IN} = 2.7 V	1,2,3		20	µA
Input low current	I_{IL}	V_{CC} = 5.5 V	V_{IN} = 0.4 V	1,2,3		-0.36	mA
Input reverse current	I_I	V_{CC} = 5.5 V	V_{IN} = 5.5 V	1,2,3		100	µA
Output short circuit current	I_{OS}	V_{CC} = 5.5 V	2/	1,2,3	-12	-65	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V; $\overline{BE}$ = $\overline{OE}$ = 3.0 V All other inputs = GND		1,2,3		110	mA
Off-state output current (receiver outputs)	I_O	V_{CC} = 5.5 V	V_O = 2.4 V	1,2,3		20	µA
			V_O = 0.4 V			-20	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
AC PARAMETERS						
Propagation delay driver clock (DRCP) to bus	t_{PLH}	C_L = 50 pF R_{L2} = 50 ohm See figure 4	9,10,11		40	ns
Propagation delay driver clock (DRCP) to bus	t_{PHL}	C_L = 50 pF R_{L2} = 50 ohm See figure 4	9,10,11		40	ns
Bus enable to bus	t_{PLH}	C_L = 50 pF R_{L2} = 50 ohm See figure 4	9,10,11		26	ns
Bus enable to bus	t_{PHL}	C_L = 50 pF R_{L2} = 50 ohm See figure 4	9,10,11		26	ns
A data inputs setup	t_S	See figure 4	9,10,11	18		ns
A data inputs hold	t_H	See figure 4	9,10,11	10		ns
Clock pulse width (High)	t_{PWH}	See figure 4	9,10,11	28		ns
Propagation delay bus to receiver output (latch enabled)	t_{PLH}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		37	ns
Propagation delay bus to receiver output (latch enabled)	t_{PHL}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		37	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay latch enable to receiver output	t_{PLH}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		37	ns
Propagation delay latch enable to receiver output	t_{PHL}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		37	ns
Bus to latch enable	t_S	See figure 4	9,10,11	21		ns
Bus to latch enable	t_H	See figure 4	9,10,11	7		ns
Propagation delay A data to odd parity out (driver enabled)	t_{PLH}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns
Propagation delay A data to odd parity out (driver enabled)	t_{PHL}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns
Propagation delay bus to odd parity out (driver inhibit)	t_{PLH}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns
Propagation delay bus to odd parity out (driver inhibit)	t_{PHL}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns

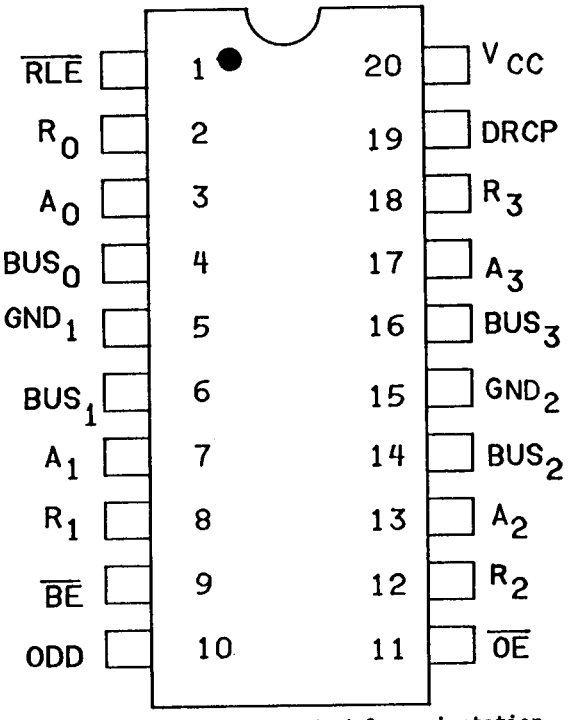
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay latch enable to odd parity output	t_{PLH}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns
Propagation delay latch enable to odd parity output	t_{PHL}	C_L = 15 pF R_{L2} = 2.0 kΩ See figure 4	9,10,11		40	ns
Propagation delay output control to output	t_{PZH}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		28	ns
Propagation delay output control to output	t_{PZL}	C_L = 15 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		28	ns
Propagation delay output control to output	t_{PHZ}	C_L = 5 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		28	ns
Propagation delay output control to output	t_{PLZ}	C_L = 5 pF R_{L1} = 5.0 kΩ R_{L2} = 2.0 kΩ See figure 4	9,10,11		28	ns

1/ Input thresholds are tested during dc testing and done in combination with other dc parameters.
2/ Not more than one output shorted at a time. Duration should not exceed one second.

Case outlines R and S



NOTE: Pin 1 is marked for orientation.

Case outline 2

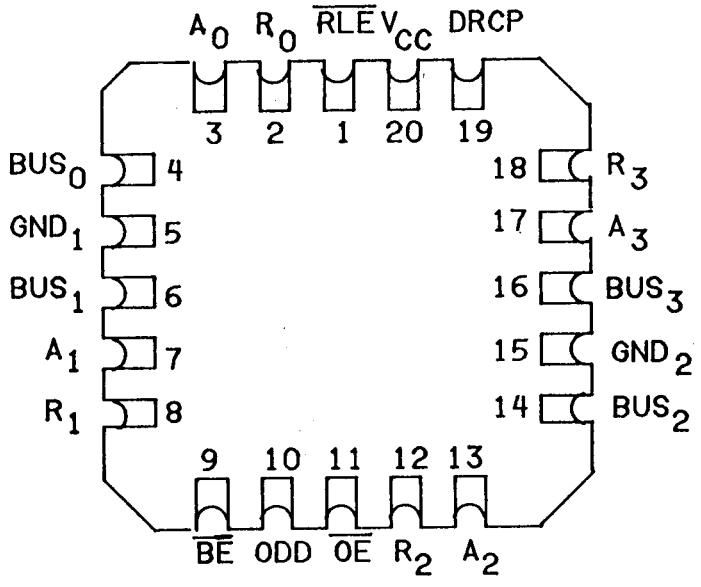


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87707
		REVISION LEVEL	SHEET 9

Inputs					Internal to device		Bus	Output	Function
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X X	X X	H H	L L	L L	X X	L H	L H	H L	Driver output disable and receive data via Bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L H	↑ ↑	X X	X X	X X	L H	X X	X X	X X	Load driver register
X X	L H	X X	X X	X X	NC NC	X X	X X	X X	No driver clock restrictions
X	X	L	X	X	H	X	L	X	Drive Bus

H = HIGH
L = LOW
Z = HIGH impedance
NC = No change
X = Don't care
↑ = LOW to HIGH transition
i = 0, 1, 2, and 3

FIGURE 2. Truth table.

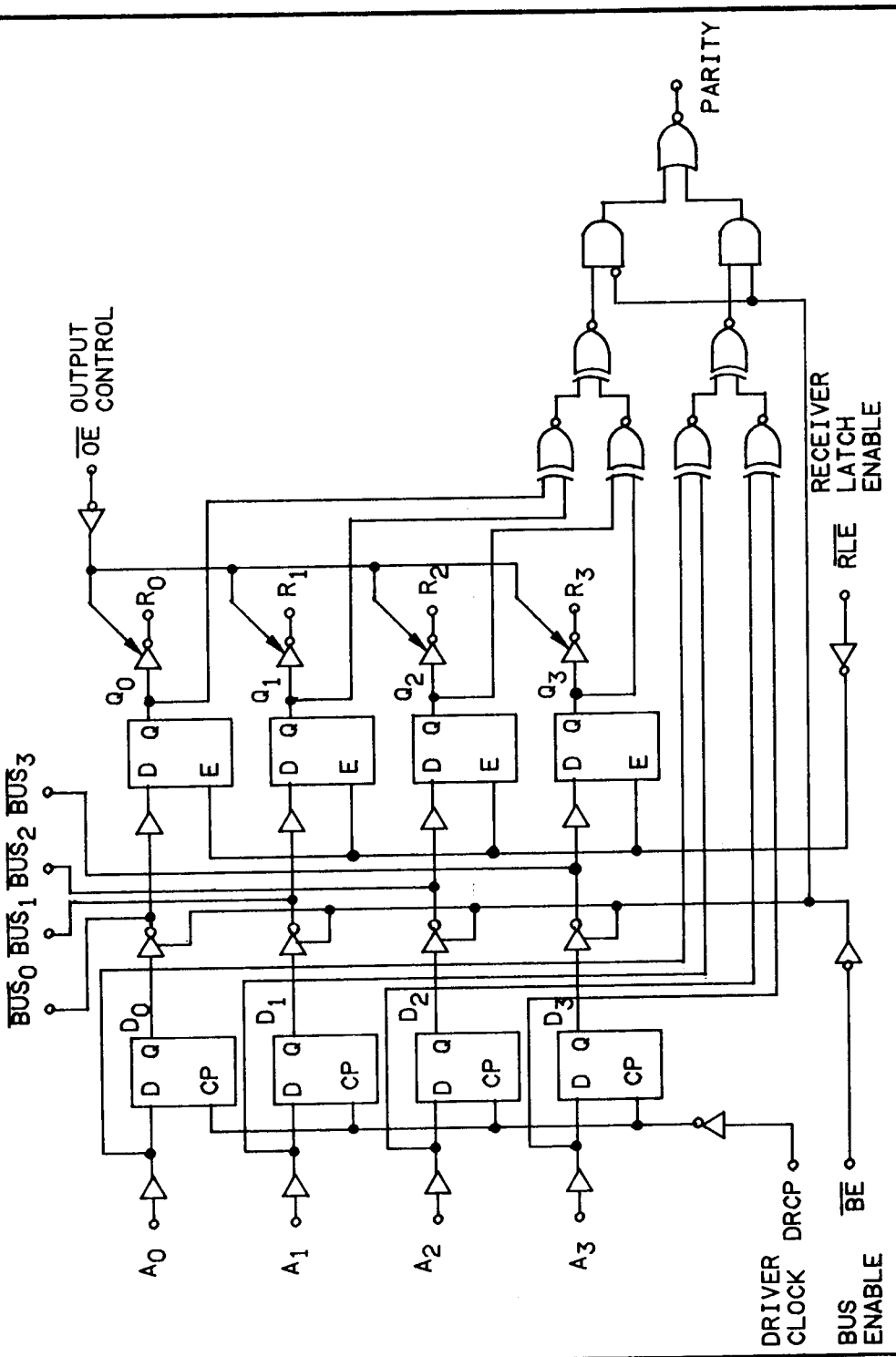
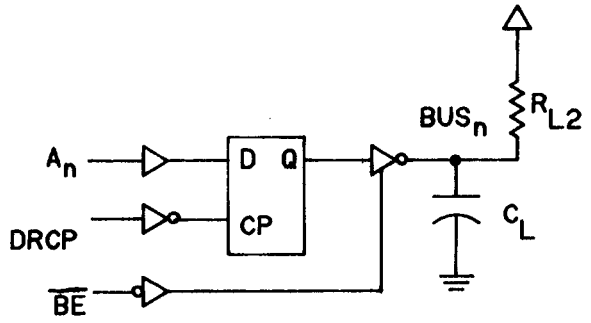
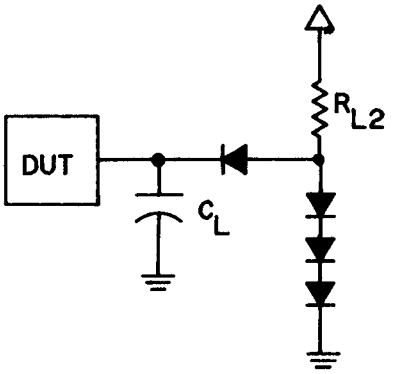


FIGURE 3. Logic diagram.

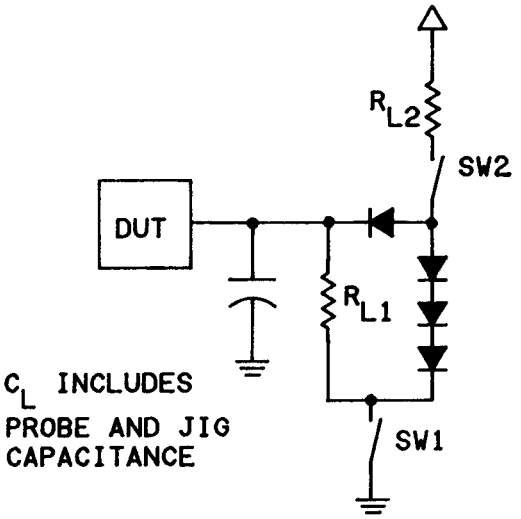
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87707
		REVISION LEVEL	SHEET 11



DRIVER SWITCHING TEST CIRCUIT



LOAD FOR PARITY OUTPUT

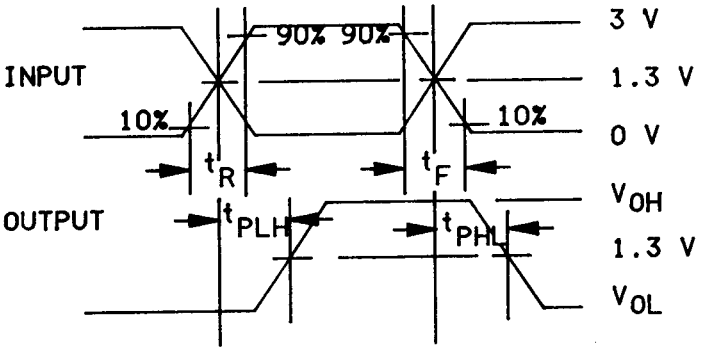


LOAD FOR RECEIVER OUTPUT

FIGURE 4. Switching test circuits and waveforms.

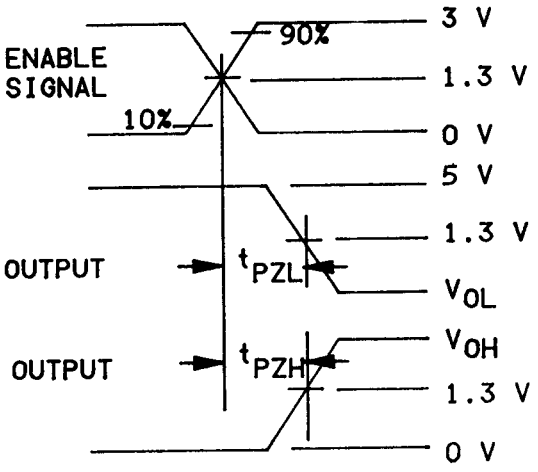
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87707
		REVISION LEVEL	SHEET 12

PROPAGATION DELAY

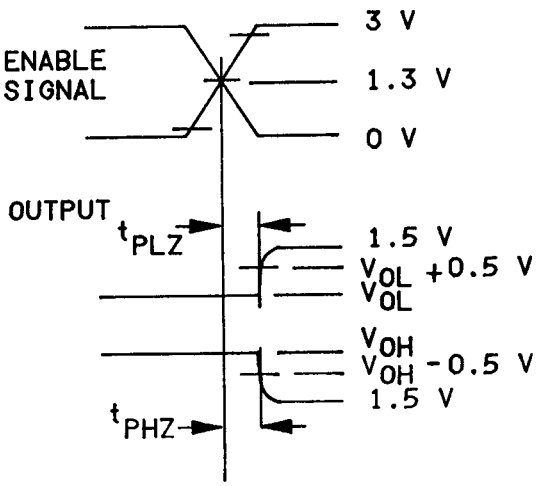


Switch matrix		
Parametar	SW1	SW2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZL}	Open	Closed
t_{PZH}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

ENABLE TIME



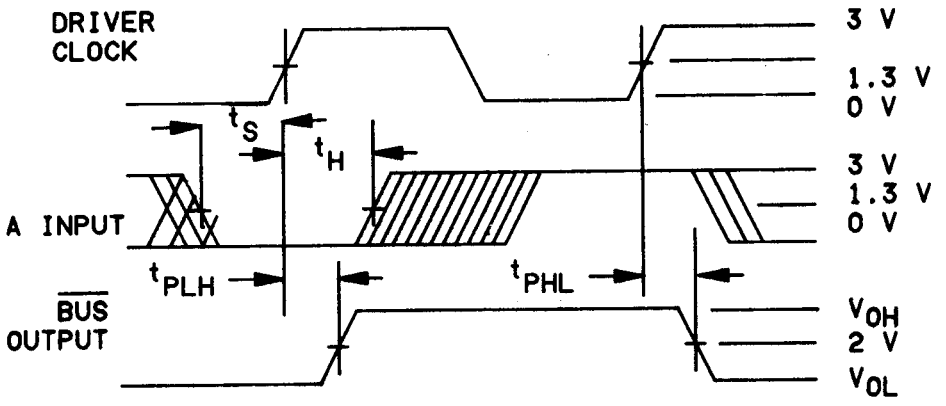
DISABLE TIME



NOTE: Pulse generator for all pulses:
Rate $\leq$ 1.0 MHz; Z_O = 50Ω; $t_R \leq$ 15 ns; $t_F \leq$ 6.0 ns.

FIGURE 4. Switching test circuits and waveforms - Continued.

INPUT SET-UP AND HOLD TIMES



LATCH ENABLE TO RECEIVER OUTPUT

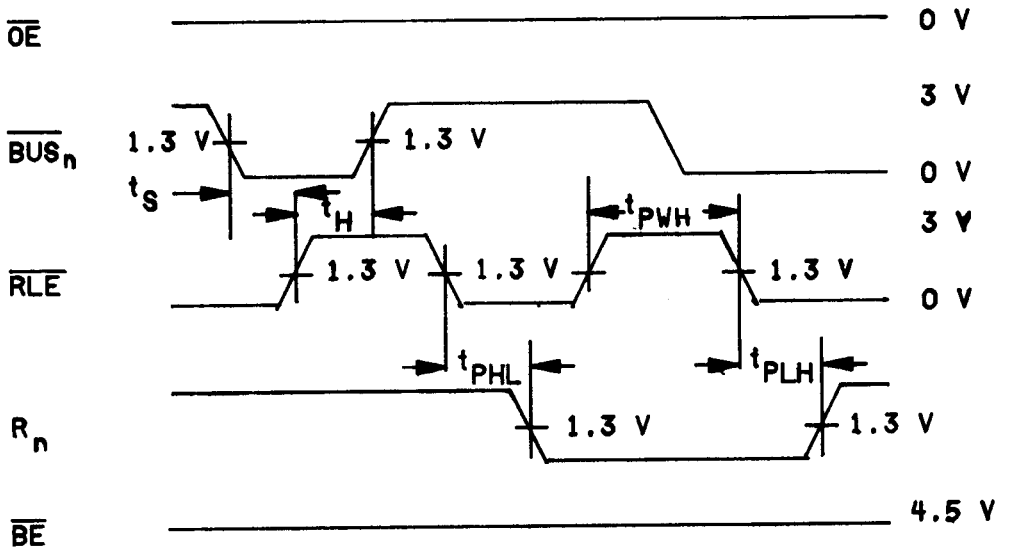


FIGURE 4. Switching test circuits and waveforms - Continued.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A and C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A and C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8770701RX	34335	AM2907/BRA	
5962-8770701SX	34335	AM2907/BSA	
5962-87707012X	34335	AM2907/B2A	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088