Introduction

EG&G Reticon's G Series solid state line scanners are optimized for second-generation solid state image sensor applications. Devices in this series contain 128, 256, 512 or 1024 photodiodes on 25 µm centers (the RL0128G, RL0256G, RL0512G, and RL1024G, respectively). Applications include optical character recognition, pattern recognition, facsimile and noncontact measurement.

Key Features

- On-chip driver and parts of video processing circuit
- Simplicity of use – single-phase TTL clock (open collector TTL or CMOS 5V)
- Several units can be directly cascaded for higher resolution
- Differential output for on-chip noise cancellation
- Charge storage mode operation for high sensitivity
- Standard dual-inline ceramic package with optical window

General Description

The Reticon G series is a family of monolithic self-scanning linear photodiode arrays. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent and multiplex switch for periodic readout via an integrated shift register scanning circuit. The shift register clock driver is also integrated so that only a single-phase TTL clock is required for scanning. A row of dummy diodes is read out differentially with the photodiodes to allow cancellation of multiplex switching transients, and to provide a clean video signal with a minimum of external circuitry. The 512 and 1024 devices are designed for low-cost facsimile applications and can easily be cascaded for extremely high resolution by optically dividing the field of view between two or more devices. The 128 and 256 element devices are well suited for OCR applications. Any of these devices may be used for noncontact measurement and inspection depending on the required resolution. Pinout configurations are shown in Figure 1.

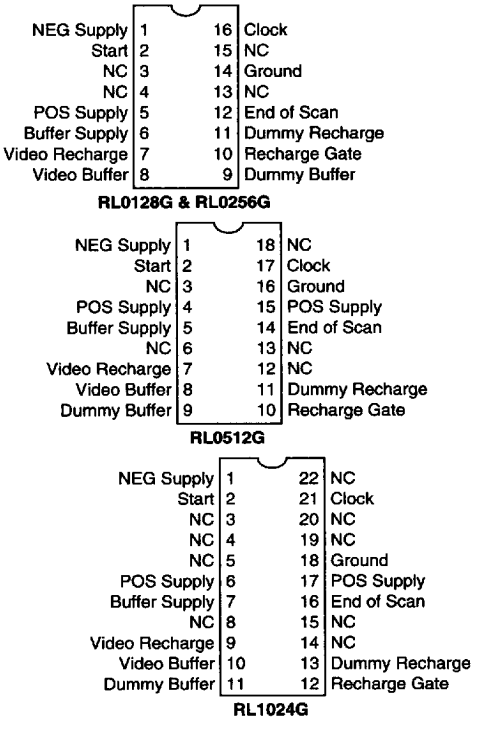

Figure 1. Pinout Configurations

Equivalent Circuit

A greatly simplified equivalent circuit of a G series line scanner is shown in Figure 2 *. Each cell consists of a photodiode and a dummy diode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to video and dummy recharge lines which are common to all the cells. The switches are sequentially closed for one clock period by the shift register scanning circuit, thereby recharging each cell to 5V and storing a charge of approximately 3 pC on its capacitance. The scanning circuit is driven by a single-phase TTL clock with a periodic TTL start pulse introduced to initiate each scan. The cell-to-cell sampling rate is the clock frequency, and the total time between line scans is the interval between start pulses. During this line time, the charge stored on each photodiode is gradually removed by photocurrent. The photocurrent is the product of the diode sensitivity and the light intensity or irradiance. The total charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled and reset once each scan.

* In the schematic diagram of Figure 2, the block labeled "shift register scanning circuit" consists of two two-phase dynamic shift registers and a drive circuit which generates four clock phases and two properly timed start pulses to load the two registers. The individual cells are actually interdigitated with the odd elements being sampled by one register, and the even numbered cells by the other register.

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The part number (RL0128G, etc) indicates the number of diodes in the various devices. The diodes are on 25 µm centers in all cases. The devices are packaged in 16, 18, or 22-pin dual-inline integrated circuit packages with ground and polished optical windows.

In addition to the signal charge, switching transients are capacitively coupled into the video line by multiplex switches. Similar transients are introduced into the dummy line and, therefore, they can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

In many applications, the recharge gate is biased to the negative supply potential and an output signal is obtained simply by differentially amplifying the recharge pulses on the video and dummy recharge lines. However, internal buffer amplifiers are also provided which may be used as part of a sample-and-hold video output circuit.

Sensor Geometry

In G line scanners the light-sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive. Photocurrent generated by light incident between photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry along with an idealized response function which would be obtained by scanning a point source of visible light along the length of the aperture.

The dimensions *a*, *b* and *c* indicated in Figure 3 are as follows: the photodiode width *a* is 15 µm, the center-to-center spacing *b* is 25 µm, and the aperture width *c* is 26 µm.

Sensitivity and Spectral Response

The spectral response of the G series devices is similar to that of other high-quality silicon photodetectors, covering the range from the near UV to the near IR. A glass window is standard; however, an optional quartz window is available. Relative spectral response is shown as a function of wavelength in Figure 4. Note that relatively high sensitivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. As most applications for these devices (OCR, fax, etc.) utilize visible light, the sensitivity and uniformity of response are specified using a source with the spectral distribution shown by the dotted line in Figure 4. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat absorbing filter 1 mm thick.

Since Reticon line scanners operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. A plot of charge output versus exposure is shown in Figure 5 for the light source of Figure 4.

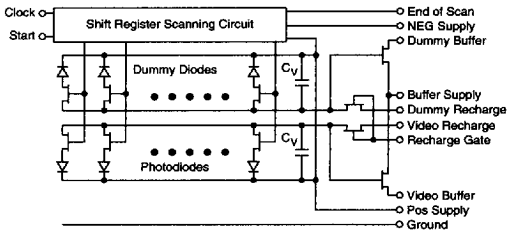

Figure 2. Simplified Equivalent Circuit

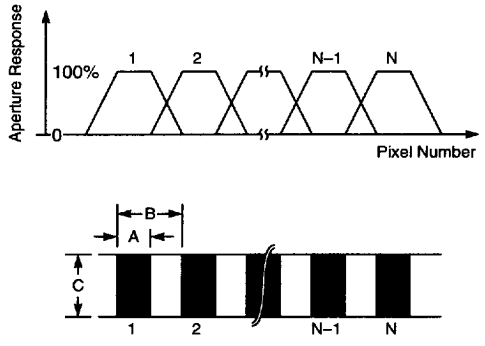

Figure 3. Sensor Geometry and Idealized Aperture Response Function

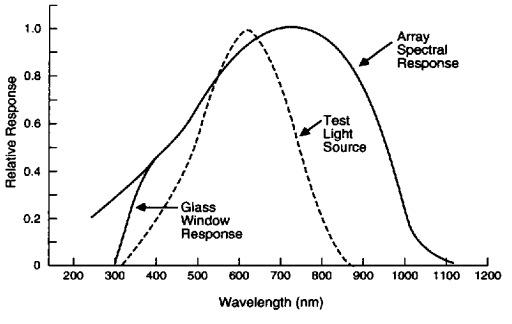

Figure 4. Relative Spectral Response as a Function of Wavelength. Dotted line shows spectral distribution of light source used for sensitivity measurements. Quartz and glass windows have similar response except the glass window will fall off at approximately 300 nm as shown above

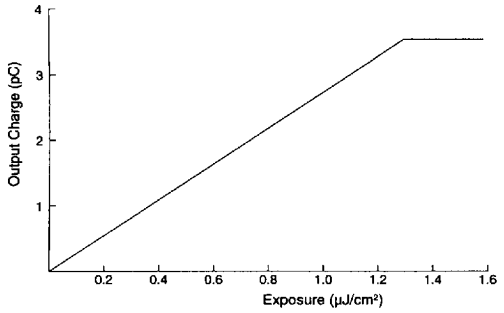

Figure 5. Signal Charge per Cell as a Function of Exposure (Light Intensity x Line Scan Time)

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible). The nonuniformity specifications of the G series are based on the light source of Figure 4.

Dark Response and Dynamic Range

There are three components to the dark output signal from a Reticon line scanner: (1) the integrated dark leakage current, (2) the fixed pattern noise caused by incomplete cancellation of clock switching transients which are capacitively coupled into the video line, and (3) the random pixel noise.

The dark leakage current will vary from element to element but is typically less than 2 pA at room temperature. Assuming this value, leakage current would contribute an output charge of 2 pC with a 1 sec line time or .08 pC with a 40 ms line time. Thus, since the saturation charge is typically 4 pC, dark current will contribute about 2% of the saturated output signal for t_L = 40 ms, 0.2% for t_L = 4 ms, and so on. The dark current is a very strong function of temperature, approximately doubling for every 7°C increase of photodiode temperature. Thus, the maximum allowable line time becomes correspondingly shorter at high temperatures, and longer at low temperatures. An important feature of the G device design is low power dissipation which means that self-heating is negligible. Dark current does not become a limiting factor in the dynamic range unless very long integration times or highly elevated temperatures are used.

The switching noise appears as a fixed pattern which is spatially random except that it may have a slight 1, 2, 3, 4 pattern because alternate diodes are sampled on different phases of an internally-generated, four-phase clock. Fixed pattern noise is largely removed by differential readout; its residual amplitude will typically be 1% of the saturation level.

Pixel noise is the random, nonrepetitive fluctuations which are superimposed on the dark level and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved depends on circuit complexity and layout techniques. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup.

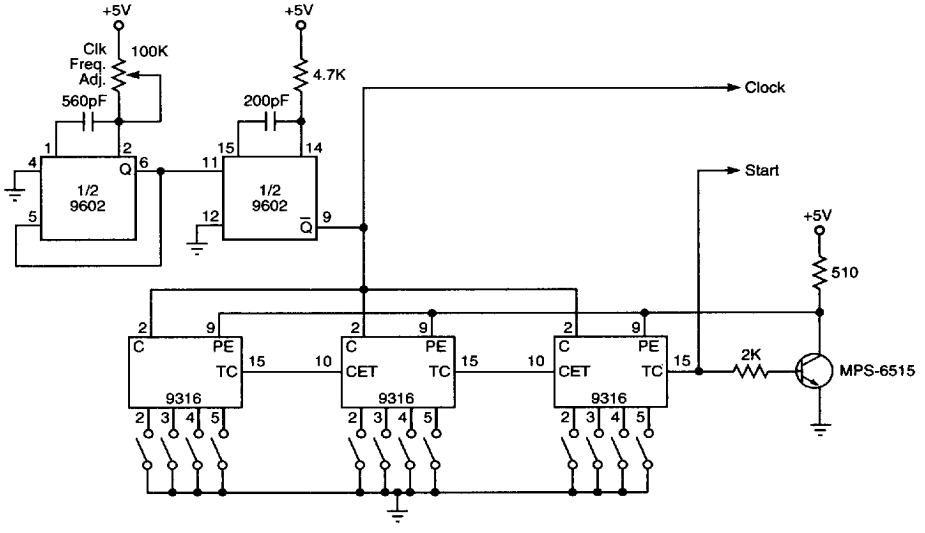

Figure 6. Clock and Counter Circuit Suitable for Generating TTL Clock and Start Pulses. The number of clock periods between start pulses may be set at any value up to 4096 by setting the switches

Drive Requirements

Two power supplies to the array are required—nominally +5 and -10V. The clock and start timing signals may be at TTL level, and may be supplied from other parts of the system or generated by using a simple circuit such as that shown in Figure 6. In this circuit, the start pulse is obtained by counting clock pulses. By setting the appropriate switches, the number of clock periods, n, between start pulses may be set at any desired value greater than or equal to N, the number of elements in the array. However, the total time between start pulses $t_L = n/f_S$ should not exceed approximately 40 ms (at room temperature) to prevent integrated dark current from making a significant contribution to the output charge.

A timing diagram showing the relationship between the clock and start pulses and the video and end-of-line outputs is shown in Figure 7.

Signal Extraction

The video output of the G devices is a train of N charge pulses flowing onto the video recharge line and dummy recharge line capacitances during each scan, with timing as shown in Figure 7. The pulses on the dummy line contain switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a useable voltage level. Two types of amplifier circuits are in common use: (1) a simple differential current amplifier, and (2) a video line integration, sample-and-hold circuit. The former has a pulse output while the latter has a boxcar output waveform.

Current Amplifier

A simple differential current amplifier circuit is shown in Figure 8. The same circuit can be used on all G series devices. In this mode of operation, the recharge gate is biased ON by connecting it to the negative supply and the signal is obtained through the video dummy and recharge lines. The unused buffer amplifiers are biased OFF by connecting all pins to the positive supply. An example of the video output of the circuit of Figure 8 is shown in the oscilloscope photograph of Figure 9.

Integrate, Sample-and-Hold Amplifier

A simple buffer mode operation circuit and its associated timing diagram are shown in Figure 10a and 10b. This alternative signal processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier, and sampled and held. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. The result is a sampled-and-held boxcar video signal such as that shown in Figure 11.

End-of-Scan

An output pulse is provided when the next-to-last element is sampled by the shift register scanning circuit. This end-of-scan output is provided primarily for test purposes. When not in use, it should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan output. In these cases, it is recommended that the voltage excursion on the end-of-scan terminal be minimized by using a circuit such as that shown in Figure 12. This figure shows a common application in which the end-of-scan output of one array is used to generate the start pulse for a second array. The timing is such that the last element of the first array and the first element of the second array are sampled on successive clock pulses.

Circuit Cards

Printed circuit cards containing all required drive and amplifier circuitry for operating G series self-scanning photodiode arrays are available from Reticon. These circuits are highly recommended for first-time array evaluation. In many cases they are also useful for design into final equipment.

Two families of circuit cards are available, corresponding to the two amplifier configurations described earlier. Both circuits are complete except for power supplies and have the flexibility to operate over a wide range of scan rates and integration times.

RC0300 Series. These boards incorporate the clock and counter circuit of Figure 6 and the amplifier circuit of Figure 8. They provide a pulse type output such as that shown in Figure 9 and give good performance at lowest cost. The boards are 3 inches square and have mounting holes in each corner on 2.6-inch centers.

RC0100 Series. These circuits provide an integrated, sampled-and-held boxcar output such as that shown in Figure 11. They are recommended for high-performance applications which require this type of output waveform. Each circuit is divided into two boards—a standard "motherboard", which contains most of the circuitry, and a small "array board", which contains only those components which must be located close to the array. The array board may be plugged directly into the motherboard or can be extended up to 30 inches away via an optional ribbon cable.

The motherboard (RC0100LNB) is 4.5 x 6.4 inches in size and is terminated by a standard 22-pin edge connector. The array boards (RC0104L) are 3 inches square and have mounting holes in each corner on 2.6-inch centers. A different array board is required for each array type.

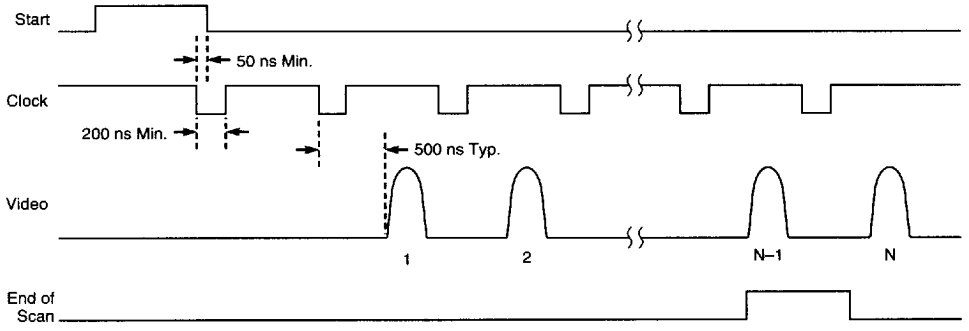

Figure 7. Timing Diagram Showing Relationship of Clock and Start Inputs to Video and End-of-Scan Outputs

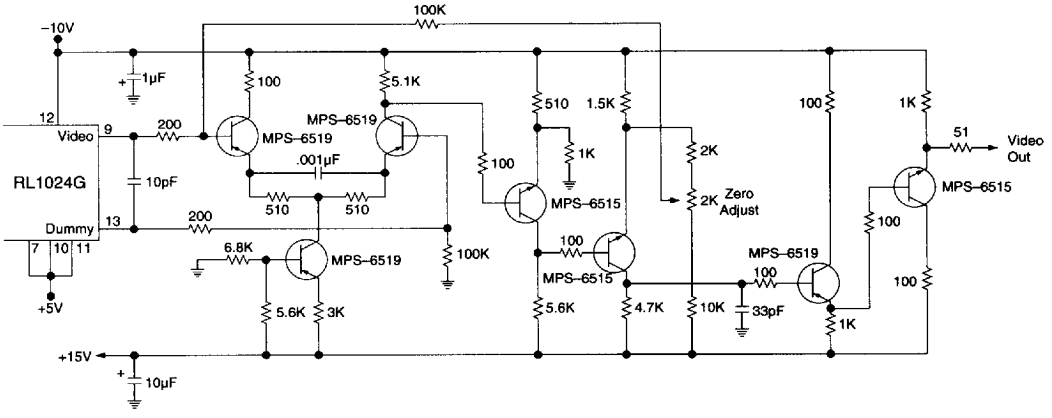

Figure 8. Differential Current Amplifier Circuit for RL1024G

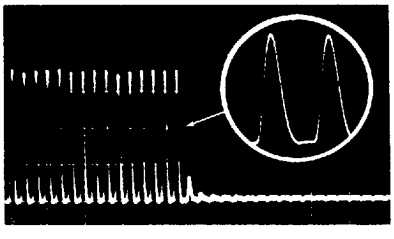

Figure 9. Oscilloscope Photograph Showing Video Output of Circuit of Figure 8

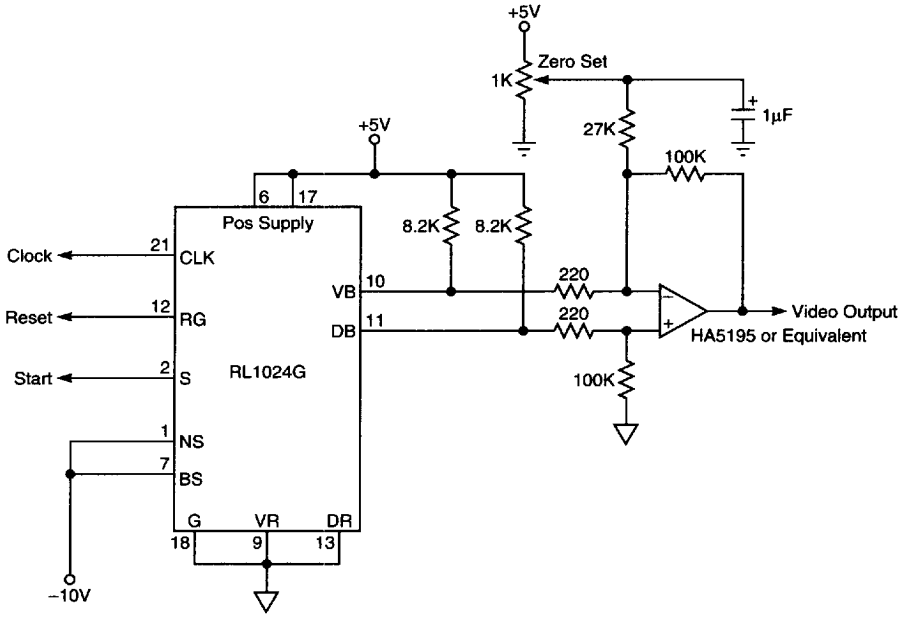

Figure 10a. Buffer Mode Operation Simplified Diagram

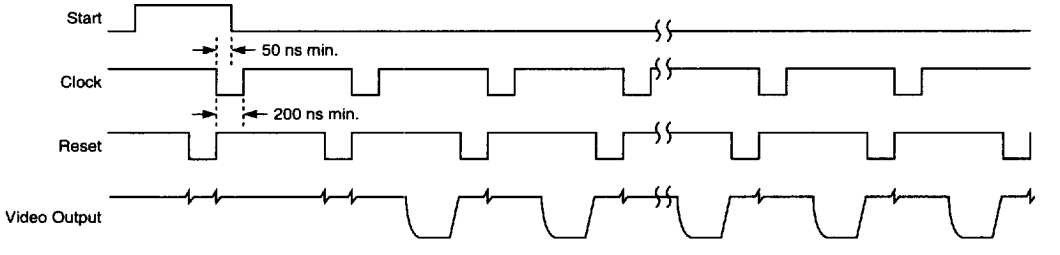

Figure 10b. Buffer Mode Timing Diagram

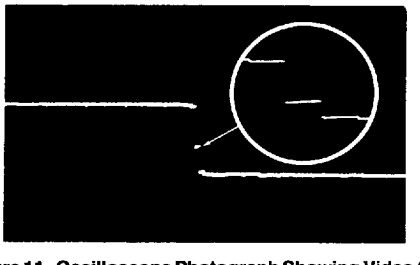

Figure 11. Oscilloscope Photograph Showing Video Output of Integrate, Sample-and-Hold Amplifier

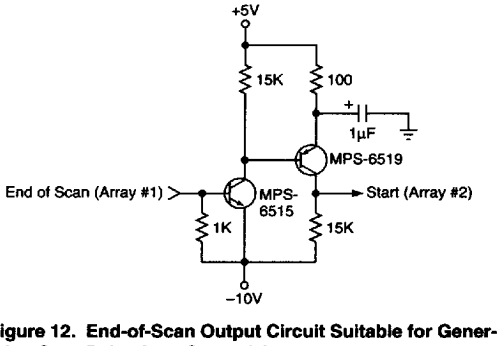

Figure 12. End-of-Scan Output Circuit Suitable for Generating Start Pulse for a Second Array

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Positive supply voltage V_P [1]	+4.5	+5	+5.5	V
Negative supply voltage V_n	-10.5	-10	-9.5	V
Clock voltage low V_{CL}	-10.5	0	+1	V
Clock voltage high V_{CH}	V_P-1	+5	V_P	V
Start voltage low V_{SL}	-10.5	0	+1	V
Start voltage high V_{SH}	V_P-1	+5	V_P	V
Recharge gate voltage low V_{RL}	-10.5	-10	-9.5	V
Recharge gate voltage high V_{RH}	V_P-1	+5	V_P	V
Clock pulse width	0.2	-	-	µs
Start pulse width	See Figure 7			
Clock frequency f_c	-	-	1	MHz
Integration time t_i [3]	-	-	40	ms
Clock input capacitance C_C [2]	-	4	-	pF
Start input capacitance C_S [2]	-	4	-	pF
Video line capacitance C_V [2]				
RL0128G	-	8	-	pF
RL0256G	-	12	-	pF
RL0512G	-	20	-	pF
RL1024G	-	30	-	pF
End-of-scan output resistance	-	5	-	KΩ
DC power dissipation [4]	-	45	-	mW

Test Conditions:

A. Typical supply parameters used
B. Light source of Figure 4
C. Clock frequency = 500 kHz
D. RC0100L series circuit used

Notes:
1 No terminal should ever be allowed to go more positive than V_P
2 Measured with nominal power supply voltages
3 Integration time can be longer if the array is cooled and/or if the application can tolerate a larger percentage of dark signal
4 Mostly due to use of on-chip buffers. When recharge mode is used (buffers biased off), power dissipation is on the order of 1 mW

Table 2. Electro-Optical Characteristics (25°C)

	Min	Typ	Max	Units
Diode center-to-center spacing	-	25	-	µm
Diode aperture width	-	26	-	µm
Photodiode sensitivity [1]	-	2.5	-	pC/µJ/cm^2
Nonuniformity of sensitivity [1]				
RL0128G	-	7	10	±%
RL0256G	-	7	10	±%
RL0512G	-	9	11	±%
RL1024G	-	12	14	±%
Saturation exposure [1]	-	1.8	-	µJ/cm^2
Saturation charge	-	4	-	pC

Note:
1 Measured using light source of Figure 4 neglecting first 2 and last 2 diodes

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

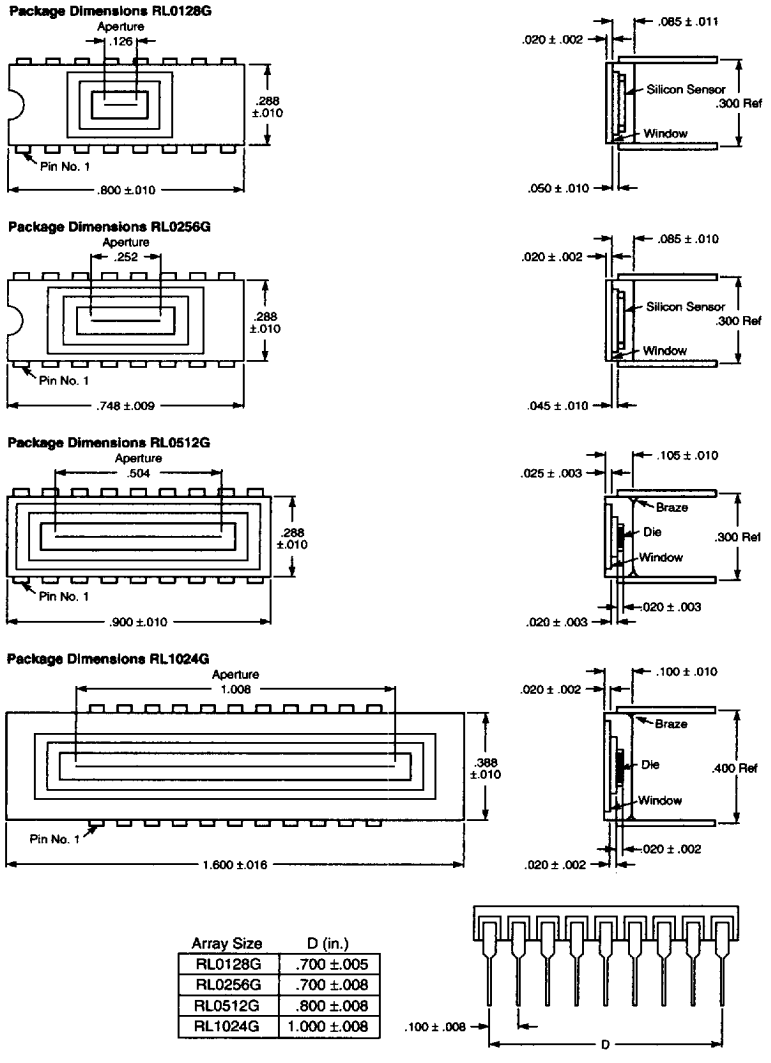

Figure 13. Package Dimensions

Ordering Information *

Ordering No.	Current Amplifier	Evaluation Circuit Integrate, S/H Amplifier
RL0128GAG-011	RC0301LNN	RC0100LNB-011/RC0104LNN-011
RL0256GAG-011	RC0301LNN	RC0100LNB-011/RC0104LNN-011
RL0512GAG-011	RC0302LNN	RC0100LNB-011/RC0105LNN-011
RL1024GAG-011	RC0303LNN	RC0100LNB-011/RC0106LNN-011

* Includes standard devices. For options, consult your local sales offices.

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