# NLSF302

# Quad 2-Input NOR Gate

The NLSF302 is an advanced high speed CMOS 2−input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed: $t_{PD}$ = 3.6 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 2.0 μA (Max) at $T_A$ = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Function Compatible with Other Standard Logic Families
- QFN−16 Package
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model > 200 V
- Chip Complexity: 40 FETs or 10 Equivalent Gates
- Pb−Free Package is Available*

**FUNCTION TABLE**

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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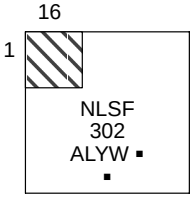
**QFN−16**
**MN SUFFIX**
**CASE 485G**

**MARKING DIAGRAM**




NLSF302 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NLSF302MNR2 | QFN−16 | 3000/Tape & Reel |
| NLSF302MNR2G | QFN−16 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

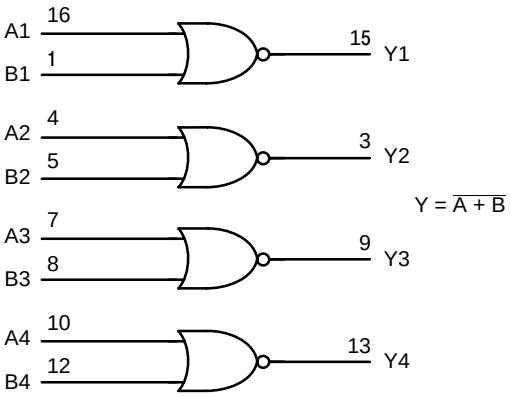



**Figure 1. LOGIC DIAGRAM**

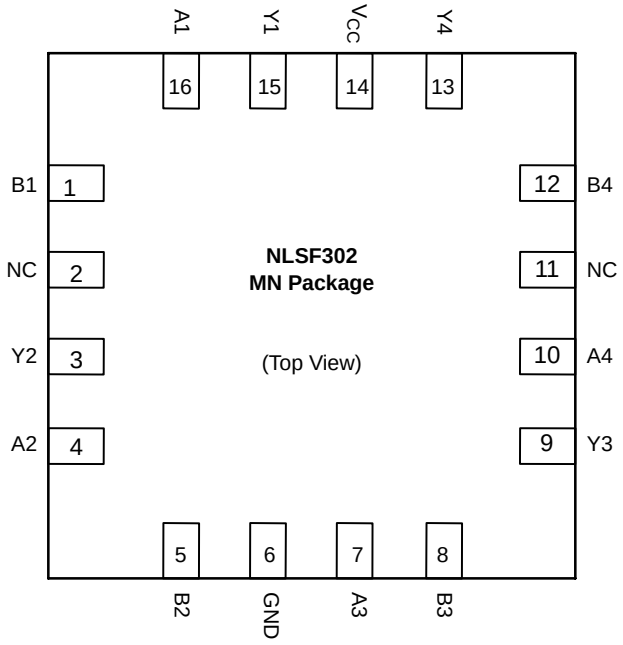



**Figure 2. PIN ASSIGNMENT (QFN−16)**

## MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | – 0.5 to + 7.0 | V |
| DC Input Voltage | $V_{in}$ | – 0.5 to + 7.0 | V |
| DC Output Voltage | $V_{out}$ | – 0.5 to $V_{CC}$ + 0.5 | V |
| Input Diode Current | $I_{IK}$ | − 20 | mA |
| Output Diode Current | $I_{OK}$ | ± 20 | mA |
| DC Output Current, per Pin | $I_{out}$ | ± 25 | mA |
| DC Supply Current, $V_{CC}$ and GND Pins | $I_{CC}$ | ± 50 | mA |
| Power Dissipation in Still Air | $P_D$ | 450 | mW |
| Storage Temperature | $T_{stg}$ | – 65 to + 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| DC Supply Voltage | | $V_{CC}$ | 2.0 | 5.5 | V |
| DC Input Voltage | | $V_{in}$ | 0 | 5.5 | V |
| DC Output Voltage | | $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature | | $T_A$ | −40 | +85 | °C |
| Input Rise and Fall Time | $V_{CC}$ = 3.3 V ± 0.3 V<br>$V_{CC}$ =5.0 V ± 0.5 V | $t_r$, $t_f$ | 0<br>0 | 100<br>20 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Parameter | Test Conditions | Symbol | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = − 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| Minimum High−Level Input Voltage | | $V_{IH}$ | 2.0<br>3.0 to 5.5 | 1.50<br>$V_{CC}$ x 0.7 | | | 1.50<br>$V_{CC}$ x 0.7 | | V |
| Maximum Low−Level Input Voltage | | $V_{IL}$ | 2.0<br>3.0 to 5.5 | | | 0.50<br>$V_{CC}$ x 0.3 | | 0.50<br>$V_{CC}$ x 0.3 | V |
| Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −50 μA | $V_{OH}$ | 2.0<br>3.0<br>4.5 | 1.9<br>2.9<br>4.4 | 2.0<br>3.0<br>4.5 | | 1.9<br>2.9<br>4.4 | | V |
| | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA | | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | |
| Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | $V_{OL}$ | 2.0<br>3.0<br>4.5 | | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V |
| | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | |
| Maximum Input Leakage Current | $V_{in}$ = 5.5 V or GND | $I_{in}$ | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| Maximum Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | $I_{CC}$ | 5.5 | | | 2.0 | | 20.0 | μA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0ns)

| Parameter | Test Conditions | Symbol | $T_A$ = 25°C | | | $T_A$ = − 40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| Maximum Propagation Delay, Input A or B to Output Y | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF<br>$C_L$ = 50 pF | $t_{PLH}$, $t_{PHL}$ | | 5.6<br>8.1 | 7.9<br>11.4 | 1.0<br>1.0 | 9.5<br>13.0 | ns |
| | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF<br>$C_L$ = 50 pF | | | 3.6<br>5.1 | 5.5<br>7.5 | 1.0<br>1.0 | 6.5<br>8.5 | |
| Maximum Input Capacitance | | $C_{in}$ | | 4 | 10 | | 10 | pF |
| Power Dissipation Capacitance (Note 1) | | $C_{PD}$ | Typical @ 25°C, $V_{CC}$ = 5.0 V<br>15 | | | | | pF |

1. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## NOISE CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0 ns, $C_L$ = 50 pF, $V_{CC}$ = 5.0V)

| Characteristic | Symbol | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| Quiet Output Maximum Dynamic $V_{OL}$ | $V_{OLP}$ | 0.3 | 0.8 | V |
| Quiet Output Minimum Dynamic $V_{OL}$ | $V_{OLV}$ | − 0.3 | − 0.8 | V |
| Minimum High Level Dynamic Input Voltage | $V_{IHD}$ | | 3.5 | V |
| Maximum Low Level Dynamic Input Voltage | $V_{ILD}$ | | 1.5 | V |

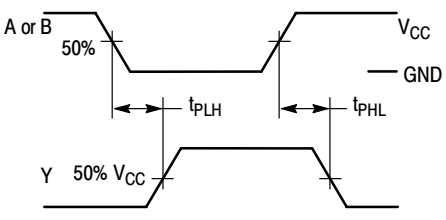
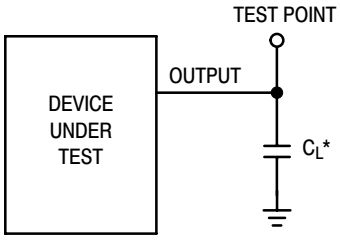



**Figure 3. Switching Waveforms**




*Includes all probe and jig capacitance

**Figure 4. Test Circuit**

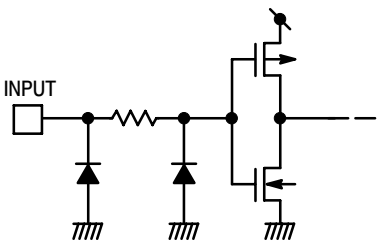
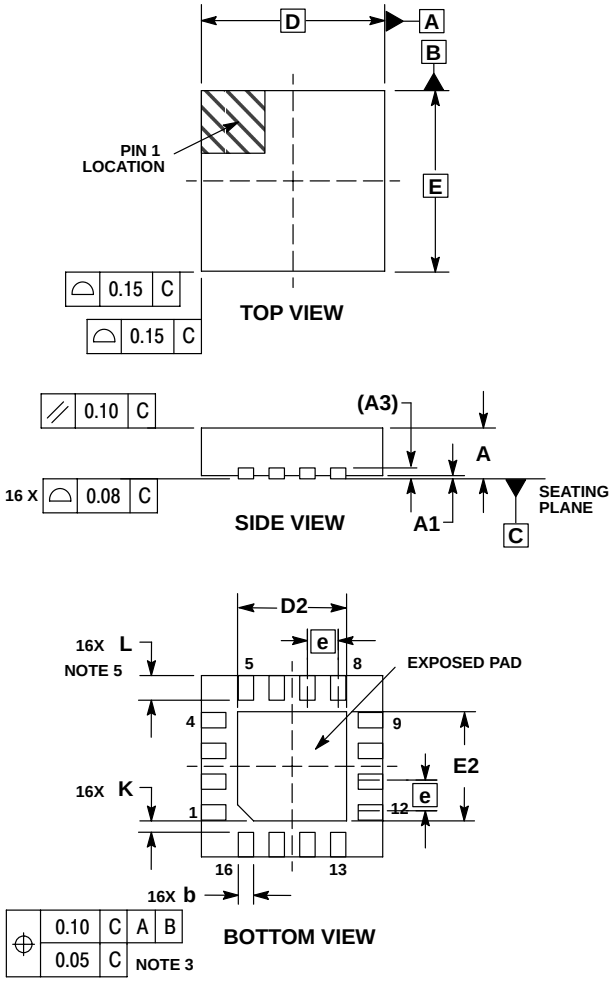



**Figure 5. Input Equivalent Circuit**

# NLSF302

## PACKAGE DIMENSIONS

**16 PIN QFN**
CASE 485G−01
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. $L_{max}$ CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.65 | 1.85 |
| E | 3.00 BSC | |
| E2 | 1.65 | 1.85 |
| e | 0.50 BSC | |
| K | 0.18 TYP | |
| L | 0.30 | 0.50 |



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**NLSF302/D**