National Semiconductor

DS8911/DS8913 AM/FM/TV Sound Up-Conversion Frequency Synthesizer

General Description

The DS8911 is a digital Phase-Locked Loop (PLL) frequency synthesizer intended for use as a Local Oscillator (LO) in electronically tuned radios. The device is used in conjunction with a serial data controller, a loop filter, some varactor diodes and several passive elements to provide the local oscillator function for both AM and FM tuning.

The conventional superheterodyne AM receiver utilizes a low IF or down conversion tuning approach whereby the IF is chosen to be below the frequencies to be received. The DS8911 PLL on the other hand, utilizes an up-conversion technique in the AM mode whereby the first IF frequency is chosen to be well above the RF frequency range to be tuned. This approach eliminates the need for tuned circuits in the AM frontend since the image, half IF, and other spurious responses occur far beyond the range of frequencies to be tuned. Sufficient selectivity and second IF image protection is provided by a crystal filter at the output of the first mixer.

A significant cost savings can be realized utilizing this up-conversion approach to tuning. Removal of the AM tuned circuits eliminates the cost of expensive matched varactor diodes and reduces the amount of labor required for alignment down from 6 adjustments to 2. Additional cost savings are realized because up-conversion enables both the AM and FM bands to be tuned using a single Voltage Controlled Oscillator (VCO) operating between 98 and 120 MHz. (The 2 to 1 LO tuning range found in conventional AM down-version radios is reduced to a 10% tuning range; 9.94 MHz to 11.02 MHz).

Up-conversion AM tuning is accomplished by first dividing the VCO signal down by a modulus 10 to obtain the LO signal. This LO in turn is mixed on chip with the RF signal to obtain a first IF at the MIXER output pins. This first IF after crystal filtering is mixed (externally) with a reference frequency provided by the PLL to obtain a 450 kHz second IF

frequency. The DS8911 derives the 450 kHz second IF by mixing an 11.55 MHz first IF with a 12.00 MHz reference frequency.

FM and WB (weather band) tuning is done using the conventional down conversion approach. Here the VCO signal is buffered to produce the LO signal and then mixed on chip with the RF signal to obtain an IF frequency at the MIXER output pins. This IF frequency is typically chosen to be 10.7 MHz although placement at 11.50 MHz can further enhance AM mode performance and minimize IF circuitry.

The PLL provides phase comparator reference frequencies of 10, 12.5, 25, and 100 kHz. The tuning resolutions resulting from these reference frequencies are determined by dividing the reference by the premix modulus. Table II shows the tuning resolutions possible.

The DS8911 contains the following logic elements: a voltage controlled oscillator, a reference oscillator, a 14-bit programmable dual-modulus counter, a premix divider chain, a premix divider, a phase comparator, a charge pump, an operational amplifier, and control circuitry for latched serial data entry.

The DS8913 includes all the above logic elements except that it requires a 10 MHz reference frequency instead of 12 MHz.

Features

■ Direct synthesis of LW, MW, SW, FM, and WB frequencies
■ Serial data entry for simplified processor control
■ 10, 12.5, 25, and 100 kHz reference frequencies
■ 8 possible tuning resolutions (see Table II)
■ An op amp with high impedance inputs for loop filtering
■ Programmable mixer with high dynamic range

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Connection Diagram

Plastic Chip Carrier
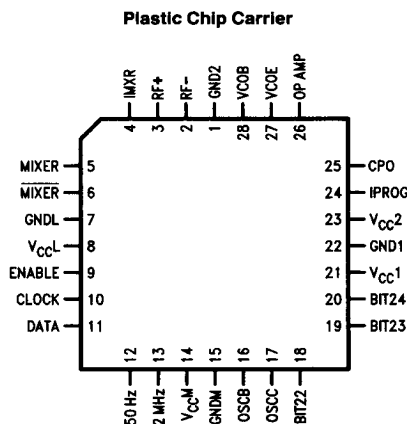
TL/F/7398–8

Top View

Order Number DS8911V/DS8913V
See NS Package Number V28A

Pin Descriptions

V_{CC1}: The V_{CC1} pin provides a 5V supply source for all circuitry except the reference divider chain, op amp and mixer sections of the die.

V_{CC2}: The V_{CC2} pin provides a 12V supply source for the Op amp.

V_{CCL}: The V_{CCL} pin provides an isolated 5V supply source for the premix divider and mixer functions.

V_{CCM}: The V_{CCM} pin provides a 5V supply source for the reference oscillator and divider chain down through the 50 Hz output, thus enabling low standby current for time-of-day clock applications.

GND1, GND2, GNDL and GNDM: Provide isolated circuit ground for the various sections of the device.

DATA and CLOCK: The DATA and CLOCK inputs are for serial data entry from a controller. They are CMOS inputs with TTL logic thresholds. The 24-bit data stream is loaded into the PLL on the positive transition of the CLOCK. The first 14 bits of the data stream select PLL divide code in binary form MSB first. The 15th through 24th bits select the premix modulus, the reference frequency, the bit output status, and the test/operate modes as shown in Tables I through V.

ENABLE: The ENABLE input is a CMOS input with a TTL logic threshold. The ENABLE input enables data when at a logic "one" and latches data on the transition to a logic "zero".

BIT Outputs: The open-collector BIT outputs provide either the status of shift register bits 22, 23, and 24 or enable access to key internal circuit test nodes. The mode for the bit outputs is controlled by shift register bits 20 and 21. In operation, the bit outputs are intended to drive radio functions such as gain, mute, and AM/FM status. These outputs can also be used to program the loop gain by connection of an external resistor to IPROG. Bit 24 output can also be used as a 300 millisecond timer under control of shift register bit 19. During service testing, these pins can be used for the purpose of either monitoring or driving internal logic points as indicated in the TEST MODES description under Table V.

VCOb and VCOe: The Voltage Controlled Oscillator inputs drive the 14-bit programmable counter and the premix divider. These inputs are the base and emitter leads of a transistor which require connection of a coil, varactor, and several capacitors to function as a Colpitts oscillator. The VCO is designed to operate up to 225 MHz. The VCO's minimum operating frequency may be limited by the choice of reference frequency and the 961 minimum modulus constraint of the 31/32 dual modulus counter.

RF + and RF −: The Radio Frequency inputs are fed differentially into the mixer.

IMXR: The bias current for the mixer is programmed by connection of an external resistor to this pin. The total mixer output current equals 4 times the current entering this pin.

MIXER and $\overline{\text{MIXER}}$: The MIXER outputs are the collectors of the double balanced pair mixer transistors. They are intended to operate at voltages greater than V_{CC1}.

OSCb and OSCc: The Reference Oscillator inputs are part of an on-chip Pierce oscillator designed to work in conjunction with 2 capacitors and a crystal resonator. The DS8911 requires a 12 MHz crystal to derive the reference frequencies shown in Table II. The DS8913 requires 10 MHz crystal.

The 12 MHz OSC signal is also used externally as the 2nd AM LO to obtain a 450 kHz 2nd IF frequency in the AM mode.

2 MHz: The 2 MHz output is provided to drive a controller's clock input.

50 Hz: The 50 Hz output is provided as a time reference for radios with time-of-day clocks.

IPROG: The IPROG pin enables the charge pump to be programmed from 0.25 mA to 1.0 mA by connection of an external resistor to ground.

CPO: The Charge Pump Output circuit sources current if the VCO frequency is high and sinks current if the VCO frequency is low. The CPO is wired directly to the negative input of the loop filter op amp.

OP AMP: The OP AMP output is provided for loop filtering. The op amp has high impedance PMOS gate inputs and is wired as a transconductance amplifier/filter. The op amp's positive input is internally referenced while its negative input is common with the CPO output.

Reference Tables

TABLE I

Bit 15	Premix Modulus
0	÷ 1
1	÷ 10

TABLE II

Bit		Reference Frequency	Tuning Resolution	
16	17		÷ 1 Premix	÷ 10 Premix
0	0	10 kHz	10 kHz	1 kHz
0	1	12.5 kHz	12.5 kHz	1.25 kHz
1	0	25 kHz	25 kHz	2.5 kHz
1	1	100 kHz	100 kHz	10 kHz

TABLE III

Bit 18	Mode
0	Normal Operation*
1	Production Test Mode Only

*The user should always load Bit 18 low.

TABLE IV

Bit 19	Timer
0	Bit 24 Status
1	Bit 24 for 300 ms

TIMER OPERATION

The timer function is provided for use as a retriggerable "one shot" to enable muting for approximately 300 milliseconds after station changes. The timer is enabled at bit 24's output if the normal operating mode is selected (shift register bits 20 and 21 = "LOW") and shift register bit 19 data is latched as a "HI". The timer's output state will invert immediately upon latching bit 19 "HI" and remain inverted for approximately 300 milliseconds. If the user readdresses the device with bit 19 data "LOW" before the timer finishes its

cycle the timer's BIT 24 output will finish out the 300 ms pulse. Readdressing the device with bit 19 "HI" before the timer finishes its cycle will extend the BIT 24 output pulse width by 300 ms. Addressing should be performed immediately after the 50 Hz output transitions "HI". BIT 24's output state is not guaranteed during the first 300 ms after V_{CC1} power up as a result of a timer reset in progress.

TABLE V

Bit		FUNCTION OF PINS 3, 4, & 5
20	21	
0	0	Status of Bits 22-24
0	1	Test mode 1
1	0	Test mode 2
1	1	Test mode 3

TEST MODE OPERATION

Test Mode 1: Enables the BIT output pins to edge trigger the phase comparator inputs and monitor an internal lock detector. BIT 22 negative edge triggers the reference divider input of the phase comparator if the reference divider state is low. BIT 23 provides the open collector ORing of the phase comparator's pump up and down outputs. BIT 24 negative edge triggers the N counter input of the phase comparator if the N counter state is preconditioned low.

Test Mode 2: Enables the BIT outputs to clock the programmable N counter, monitor its output, and force either its load or count condition. BIT 22 provides the N counter output which negative edge triggers the phase comparator and which appears low one N counter clock pulse before it reloads. BIT 23 positive edge triggers the N counter's clock input if the prescaler's output is preconditioned HI. BIT 24 clears the N counter output so that loading will occur on the next N counter clock edge.

Test Mode 3: Enables the BIT outputs to clock the 50 Hz and 10 kHz reference dividers and monitor the reference divider input to the phase comparator. BIT 22 positive edge clocks the 10 kHz reference divider chain if the 10 kHz output is preconditioned HI. BIT 23 positive edge clocks the 50 Hz divider chain. BIT 24 is the reference divider negative edge trigger input to the phase comparator.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CCM}	7V
V_{CC1}	7V
V_{CC2}	15V
Input Voltage	7V
Output Voltage	
Logic	7V
Op Amp and Mixer Outputs	15V
ESD Sensitivity	1000V

Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CCM}	3.5	5.5	V
V_{CC1}	4.5	5.5	V
V_{CC2}	7.0	12.0	V
Temperature, T_A	-40	$+85$	°C
Mixer I_{BIAS} (Mixer + $\overline{Mixer}$ Current)	1	20	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage				2.0			V
V_{IL}	Logic "0" Input Voltage						0.8	V
I_{IH}	Logic "1" Input Current		$V_{IN} = 5.5V$				10	μA
I_I	Logic "1" Input Current		Data, Clock and Enable Inputs, $V_{IN} = 7V$				100	μA
I_{IL}	Logic "0" Input Current		Data, Clock and Enable Inputs, $V_{IN} = 0V$				-10	μA
V_{OH}	Logic "1" Output Voltage	2 MHz	$I_{OH} = -20\ \mu A$		$V_{CCM} - 0.3$			V
			$I_{OH} = -400\ \mu A$		$V_{CCM} - 2$			V
		Op Amp	$I_{OH} = -1.0\ mA$		$V_{CC2} - 1.5$			V
V_{OL}	Logic "0" Output Voltage	2 MHz	$I_{OL} = 20\ \mu A$				0.3	V
			$I_{OL} = 400\ \mu A$				0.4	V
		50 Hz	$I_{OL} = 250\ \mu A$				0.3	V
		Bit Outputs	$I_{OL} = 1\ mA$				0.3	V
		Op Amp	$I_{OL} = 1.0\ mA$				1.5	V
V_{BIAS}	Op Amp Input VΔ		Op Amp I/O Shorted, $V_{CC1} = 5.5V$, $V_{CC2} = 12V$, CPO = TRI-STATE®, Op Amp I_{OH} vs. I_{OL} Applied				200	mV
I_{CEX}	High Level Output Current	Bit Outputs	$V_{CC1} = 4.5V$, $V_O = 8.8V$				100	μA
		50 Hz	$V_{CCM} = 3.5V$, $V_O = 5.5V$				10	μA
		Mixers	$V_{CCL} = V_{CC1} = 4.5V$, $V_O = 12V$				100	μA
I_{CPO}	Charge Pump Program Current		$0.25\ mA < I_{CPO} < 1.0\ mA$ $2\ I_{PROG} = V_{CC1}/R_{PROG}$, Measured I_{PROG} to CPO	Pump-up	-30	$2\ I_{PROG}$	$+30$	%
				Pump-down	-30	$2\ I_{PROG}$	$+30$	%
				TRI-STATE		0	100	nA
I_{CCM}	V_{CCM} Supply Current (Static)		$V_{CCM} = 5.5V$, OSCC = High			0.5	1.0	mA
$I_{CC1} + I_{CCL}$	$V_{CC1} + V_{CCL}$ Supply Current		$V_{CC} = 5.5V$, Bits Hi, I_{MXR} and I_{PROG} Open			25	35	mA
I_{CC2}	V_{CC2} Supply Current		$V_{CC2} = 12V$			1.5	2.5	mA
Mixer I_{BIAS}	Mixer + $\overline{Mixer}$ Current (Note 4)		$V_{CC1} = V_{CCL} = 5.5V$, Mixer = $\overline{Mixer} = 12V$		-25	$4\ I_{MXR}$	$+25$	%
RF_{IN}	Mixer Input Max Signal Level		Mixer $I_{BIAS} = 20\ mA$ $RF+$ or $RF-$ Signal Level			300		mVrms

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the $-40°C$ to $+85°C$ temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Note 4: Total mixer output current (Mixer + $\overline{Mixer}$) $\cong$ 4 times the current into the I_{MXR} pin.

AC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	20%–80% Rise Time			200		ns
t_f	80%–20% Fall Time			200		ns
DATA$_{SU}$	Data Setup Time		100			ns
DATA$_H$	Data Hold Time	V_{CC1} = 4.5V to 5.5V	100			ns
EN$_{SU}$	Enable Setup Time		100			ns
EN$_H$	Enable Hold Time		100			ns
EN$_{PW+}$	Enable Positive Pulse Width		200			ns
CLK$_{PW+}$	Clock Positive Pulse Width		200			ns
CLK$_{PW-}$	Clock Negative Pulse Width		200			ns
VCO f_{max}	VCO Max Frequency	See Typical Wiring Diagram	20		225	MHz
OSC f_{max}	Reference Oscillator Max Frequency	V_{CCM} = 3.5V		12		MHz

Timing Diagram
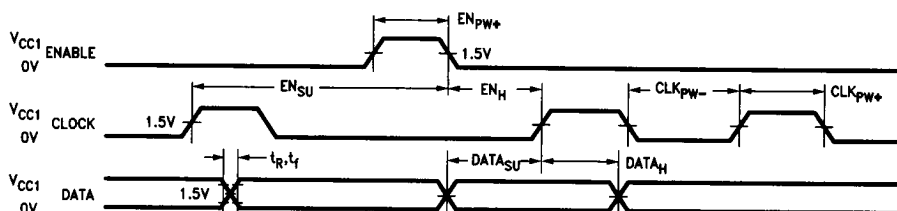
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MICROWIRE™ Bus Format

TL/F/7398–19

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	11.55/.450	.145−.290	112.4−114.1	10	10	1	22−23
MW	11.55/.450	.515−1.61	99.4−110.2	10	10, 12.5, 25, 100	1, 1.25, 2.5, 10	21−23
SW	11.55/.450	5.94−6.2	53.5 to 56.1	10	10, 12.5, 25	1, 1.25, 2.5	28−30
FM	10.7	87.4−108.1	98.1−118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109−130
WB	10.7	162.4−162.6	151−152	1	12.5, 25	12.5, 25	140−142
TV$_1$	10.7	59.75−87.75	70.45−98.45	1	25	25	81−109
TV$_2$	10.7	179.75−215.75	169.1−205.1	1	25	25	158−194

TABLE VI. DS8911 Tuning Characteristics

Input and Output Schematics

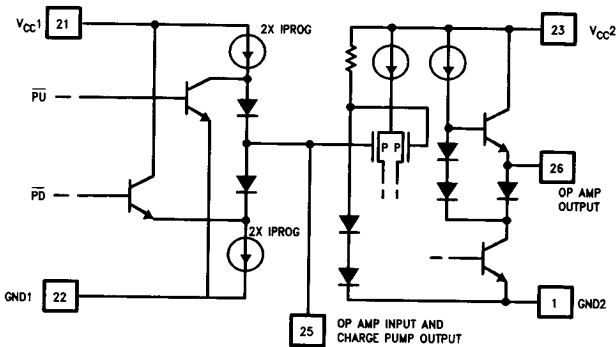$$R = \frac{4\,(V - 0.8)}{MIXER\ I_{BIAS}} - 200\,\Omega$$

I_{MXR} RESISTOR CALCULATION
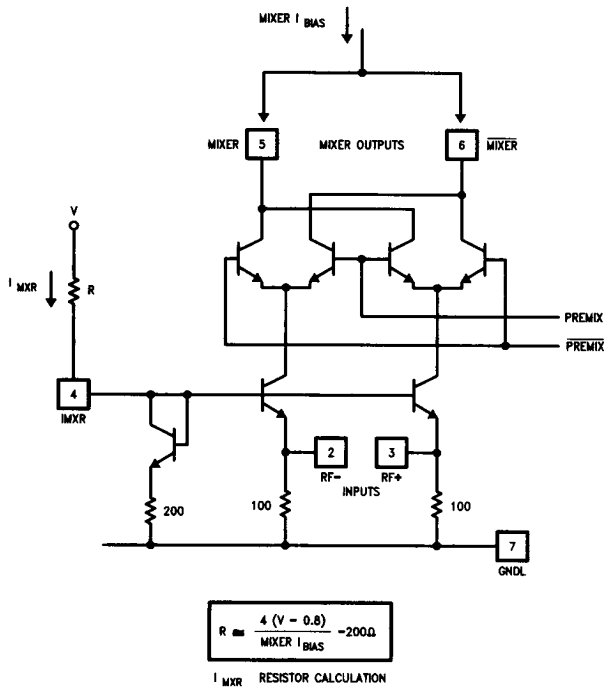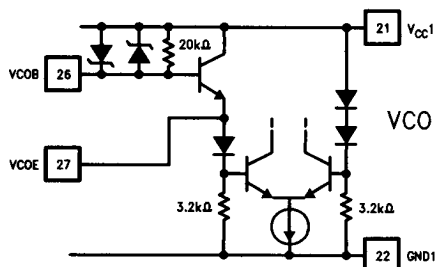
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TL/F/7398−12

Input and Output Schematics (Continued)

50Hz OUTPUT BUFFER

2 MHz OUTPUT BUFFER

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CRYSTAL OSCILLATOR

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INPUT BUFFERS (ONE OF THREE)

PIN 9 ENABLE
PIN 10 CLOCK
PIN 11 DATA

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TEST INPUTS

(SAME SCHEMATIC AS ENABLE, CLOCK AND DATA BUFFERS)

BIT OUTPUTS (ONE OF THREE)

PIN 18 BIT 22
PIN 19 BIT 23
PIN 20 BIT 24

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TL/F/7398–17

TL/F/7398–18

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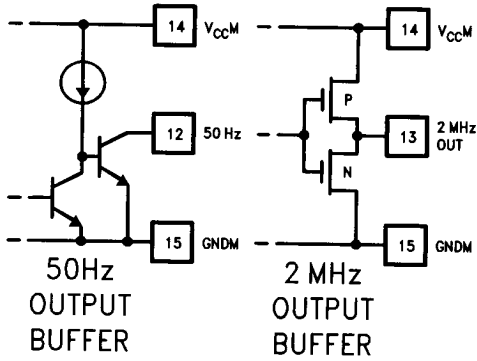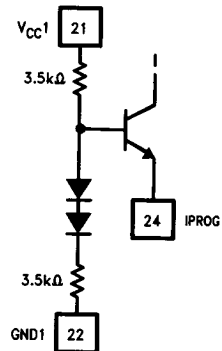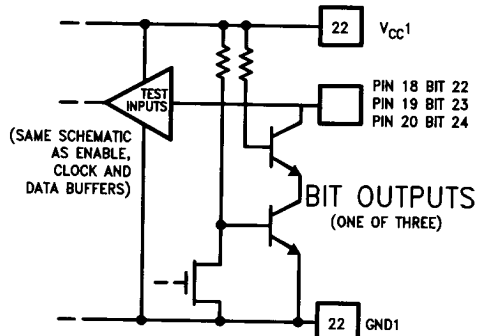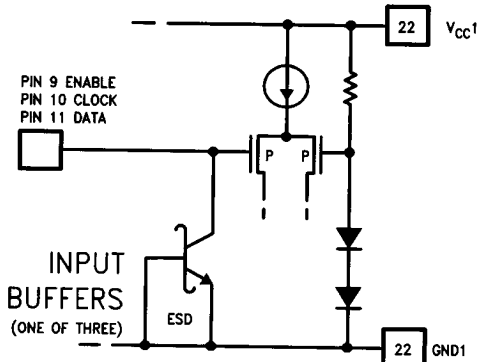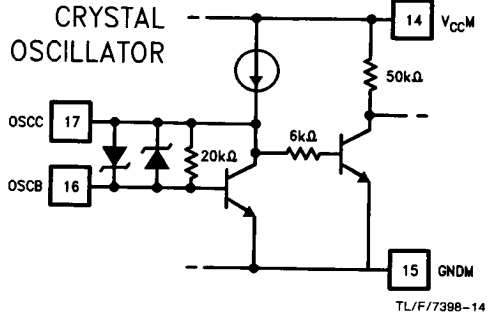
Logic Diagram
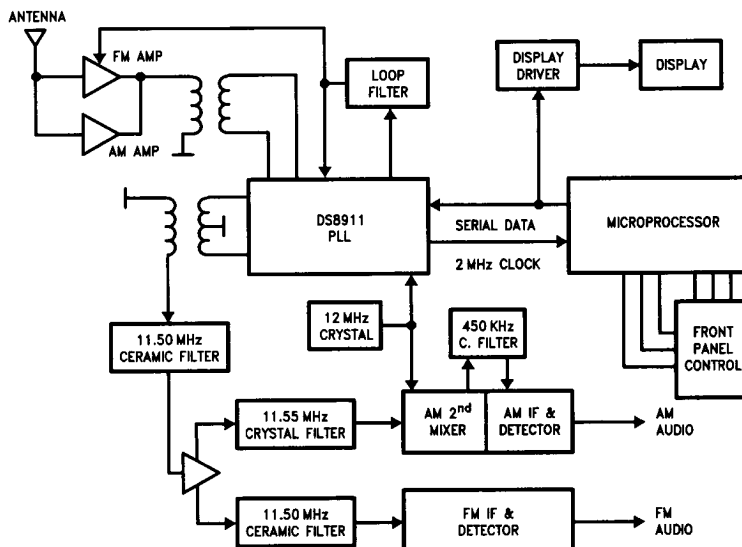
DS8911/DS8913 PLL Synthesizer
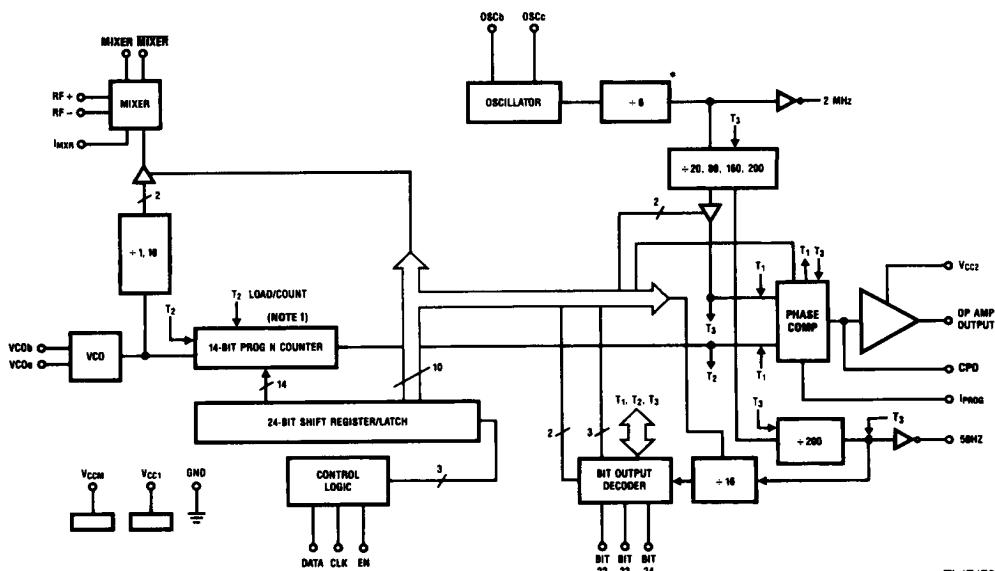
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Note 1: The 14 bit programmable N counter is a dual modulus counter with 31/32 prescaler. The minimum continuous modulus of the N counter is 961. (There are a limited number of valid modulus codes below 961.)
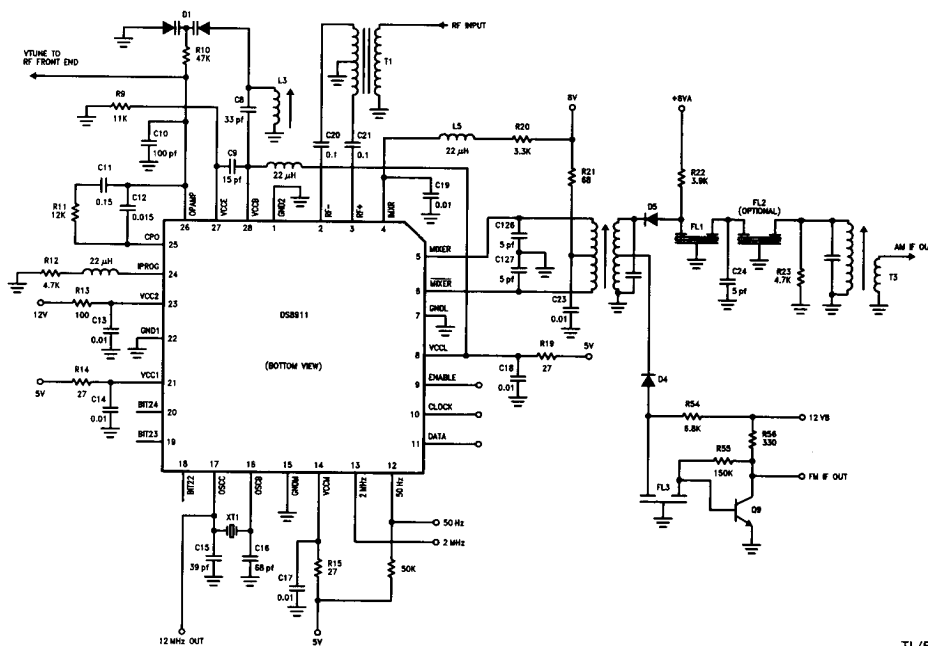
*The DS8913 has ÷ 5

Typical Application Diagram
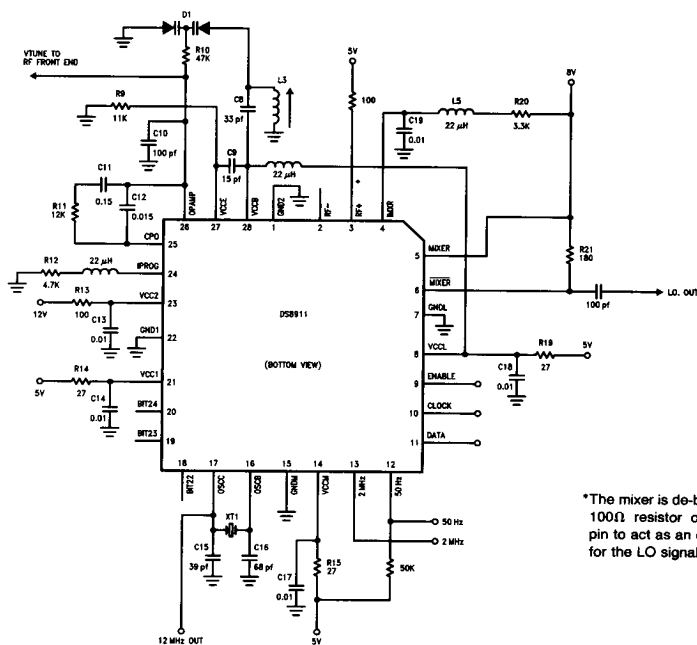
AM/FM ETR Radio Application

TL/F/7398–5

Wiring Diagrams

Configuration Using PLL and First Mixer Functions

TL/F/7398-20

Configuration Using PLL with LO Bypassing Mixer

*The mixer is de-biased by the 100Ω resistor on the RF+ pin to act as an output buffer for the LO signal.

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