100761

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add case outline Y. Change to military drawing format. Change A.C. parameters TAVDV, TRLDV, TLHLL, TAVLL. Change drawing CAGE to 67268. Editorial changes throughout.	23 OCT 87	

CURRENT CAGE CODE 67268

REV																											
PAGE																											
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A										
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16										

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
18 November 1985

AMSC N/A

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SIZE: A

CODE IDENT. NO.: 14933

REV: A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, N-CHANNEL, 16-BIT MICROCONTROLLER, SILICON GATE, MONOLITHIC

DWG NO. 85063

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5962-E580

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DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

85063	01	Z	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish (3.3)

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	8097	NMOS 16-bit Microcontroller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C, MIL-M-38510 and as follows:

Outline letter	Case outline
Y	Figure 1, 68-lead ceramic quad pack
Z	P-AC, 68-pin hermetic grid array package

#196 PGA, 68 PIN, 11 x 11

1.3 Absolute maximum ratings.

Supply voltage	7.0 V dc maximum
Operating voltage range	-0.3 V dc to +7.0 V dc
Case temperature under bias 1/	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Voltage from any pin to V_{SS} or ANGND	-0.3 V dc to 7.0 V dc
Average output current (any pin)	10 mA maximum
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Maximum junction temperature	+200°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Y	5°C/W
Case Z	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Case temperature under bias (T_C) 1/	-55°C ≤ T_C ≤ +125°C
Digital supply voltage (V_{CC})	4.50 V dc ≤ V_{CC} ≤ 5.50 V dc
Analog supply voltage (V_{REF})	4.5 V_{CC} -0.3 ≤ V_{REF} ≤ 5.5 V_{CC} +0.3 V
Oscillator frequency (f_{OSC})	6.0 MHz ≤ f_{OSC} ≤ 12 MHz
Power down supply voltage (V_{PD})	4.50 V ≤ V_{PD} ≤ 5.5 V
Resolution 2/	±.001 V_{REF} 3/
Accuracy 2/	±.004 V_{REF}
Differential nonlinearity 2/	±.002 V_{REF} maximum 3/
Integral nonlinearity 2/	±.004 V_{REF} maximum 3/
Channel-to-channel matching	±1 LSB 4/
Crosstalk (dc to 100 kHz)	-60 dB maximum 4/

1/ Case temperature is "instant on".
2/ Testing is done at V_{REF} = 5.120 V.
3/ Guaranteed but not tested.
4/ Not tested or guaranteed.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtain from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Block diagram. The block diagram shall be as specified on figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage (except $\overline{\text{RESET}}$)	V_{IL}		1, 2, 3	-0.3 1/	+0.8	V
Input low voltage, $\overline{\text{RESET}}$	V_{IL1}		1, 2, 3	-0.3 1/	+0.7	V
Input high voltage (except $\overline{\text{RESET}}$, NMI, XTAL1)	V_{IH}		1, 2, 3	2.0	V_{CC} +0.5 1/	V
Input high voltage, $\overline{\text{RESET}}$, NMI, XTAL1	V_{IH1}		1, 2, 3	2.4	V_{CC} +0.5 1/	V
Output low voltage	V_{OL}	2/	1, 2, 3		0.5	V
Output high voltage	V_{OH}	3/	1, 2, 3	2.4		V
V_{CC} supply current	I_{CC}	All outputs disconnected	1, 2, 3		200	mA
V_{PD} supply current	I_{PD}	Normal operation and power-down	1, 2, 3		1	mA
V_{REF} supply current	I_{REF}	All bits	1, 2, 3		10	mA
Input leakage current to all pins of HSI, P0, P3, P4, and to P2.1	I_{LI}	V_{IN} = 0 to V_{CC} 4/	1, 2, 3		±10	µA
Input high current to $\overline{\text{EA}}$	I_{IH}	V_{IH} = 2.4 V	1, 2, 3		100	µA
Input low current to all pins of P1, and to P2.6, P2.7	I_{IL}	V_{IL} = 0.45 V	1, 2, 3		-100	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits		Unit
				Min	Max	
Input low current to $\overline{\text{RESET}}$	I_{IL1}	V_{IL} = 0.45 V	1, 2, 3		-2	mA
Input low current P2.2, P2.3, P2.4, READY	I_{IL2}	V_{IL} = 0.45 V	1, 2, 3		-50	µA
Pin capacitance (any pin to V_{SS})	C_S	fTEST = 1.0 MHz See 4.3.1c	4		10	pF
Oscillator frequency	FXTAL	Oscillator frequency = 12 MHz Load capacitance on output pins = 80 pF	9, 10, 11	6.0	12.0	MHz
1/Oscillator frequency	TOSC	See figure 3		83	166	ns
CLKOUT period 5/, 8/	TCHCH			3Tosc-30	3Tosc+30	ns
CLKOUT high time	TCHCL			Tosc-20	Tosc+20	ns
CLKOUT low to ALE high	TCLLH			-30	+30	ns
ALE low to CLKOUT high	TLLCH			Tosc-20	Tosc+40	ns
ALE pulse width	TLHLL			Tosc-30	Tosc+20	ns
Address valid to end of ALE	TAVLL			Tosc-60		ns
End of ALE to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ active	TLLRL			Tosc-20		ns
End of ALE to address invalid 8/	TLLAX			Tosc-20		ns
$\overline{\text{WR}}$ pulse width	TWLWH			2Tosc-35		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Output data valid to end of $\overline{WR}$	TQVWX	Oscillator frequency = 12 MHz Load capacitance on output pins = 80 pF See figure 3	9, 10, 11	2Tosc-60		ns
Output data hold after $\overline{WR}$ 8/	TWXQX			Tosc-25		ns
End of $\overline{WR}$ to next ALE	TWXLH			2Tosc-30		ns
$\overline{RD}$ pulse width	TRLRH			3Tosc-30		ns
End of $\overline{RD}$ to next ALE	TRHLH			Tosc-30		ns
READY hold after CLKOUT edge 6/	TCLYX			0		ns
End of ALE to READY setup 6/	TLLYV			-Tosc 1/	2Tosc-60	ns
Non-ready time 6/	TYLYH				1,000	ns
Address valid to input data valid 6/	TAVDV				5Tosc-100	ns
$\overline{RD}$ active to input data valid 1/ 6/	TRLDV				3Tosc-70	ns
End of $\overline{RD}$ to input data float 6/	TRXDZ			0	Tosc-20	ns
End of ALE to READY 6/	TLLYH			2Tosc+60 1/	4Tosc-60 7/	ns

1/ Guaranteed but not tested.
2/ I_{OL} = 0.36 mA for all pins of P1, for P2.6 and P2.7, and for all pins of P3 and P4 when used as ports. I_{OL} = 2.0 mA for TXD, RXD (in serial port mode 0), PWM, CLKOUT, ALE, BHE, RD, WR, and all pins of HSO and P3 and P4 when used as external memory bus (AD0-AD15).
3/ I_{OH} = -20 µA for all pins of P1, for P2.6 and P2.7. I_{OH} = -200 µA for TXD, RXD (in serial port mode 0), PWM, CLKOUT, ALE, BHE, WR, and all pins of HSO and P3 and P4 when used as external memory bus (AD0-AD15). P3 and P4, when used as ports, have open-drain outputs.
4/ Analog conversion not in process.
5/ CLKOUT is directly generated as a divide by three of the oscillator. The period will be 3Tosc ±10 ns if Tosc is constant and the rise and fall times on XTAL1 are less than 10 ns.
6/ Other system components must meet these specifications.
7/ If more than one wait state is desired, add "3Tosc" for each additional wait state.
8/ Due to test equipment limitation, actual tested values may differ from those specified, but specified limits are guaranteed.

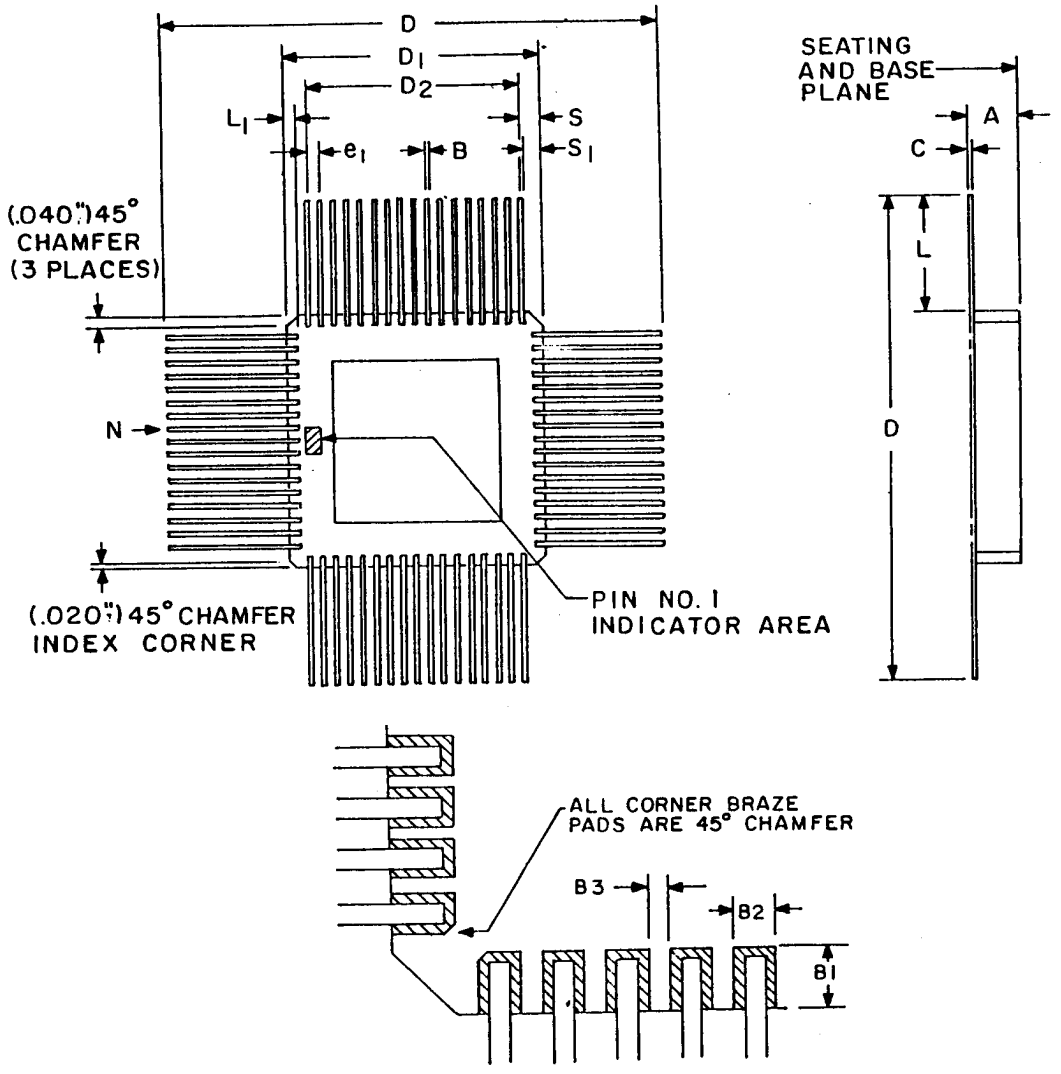

FIGURE 1. Case outline Y.

FLATPACK, 68 PIN, SQ

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Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.080	0.106	2.03	2.69
B	0.016	0.020	0.41	0.51
B_1	0.040	0.060	1.02	1.52
B_2	0.030	0.040	0.76	1.02
B_3	0.005	0.020	0.13	0.51
C	0.008	0.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D_1	0.935	0.970	23.75	24.64
D_2	0.800 BSC		20.32 BSC	
e_1	0.050 BSC		1.27 BSC	
L	0.375	0.450	9.53	11.43
L_1	0.040	0.060	1.02	1.52
N	68		68	
S	0.066	0.087	1.68	2.21
S_1	0.050		1.27	

FIGURE 1. Case outline Y - Continued.

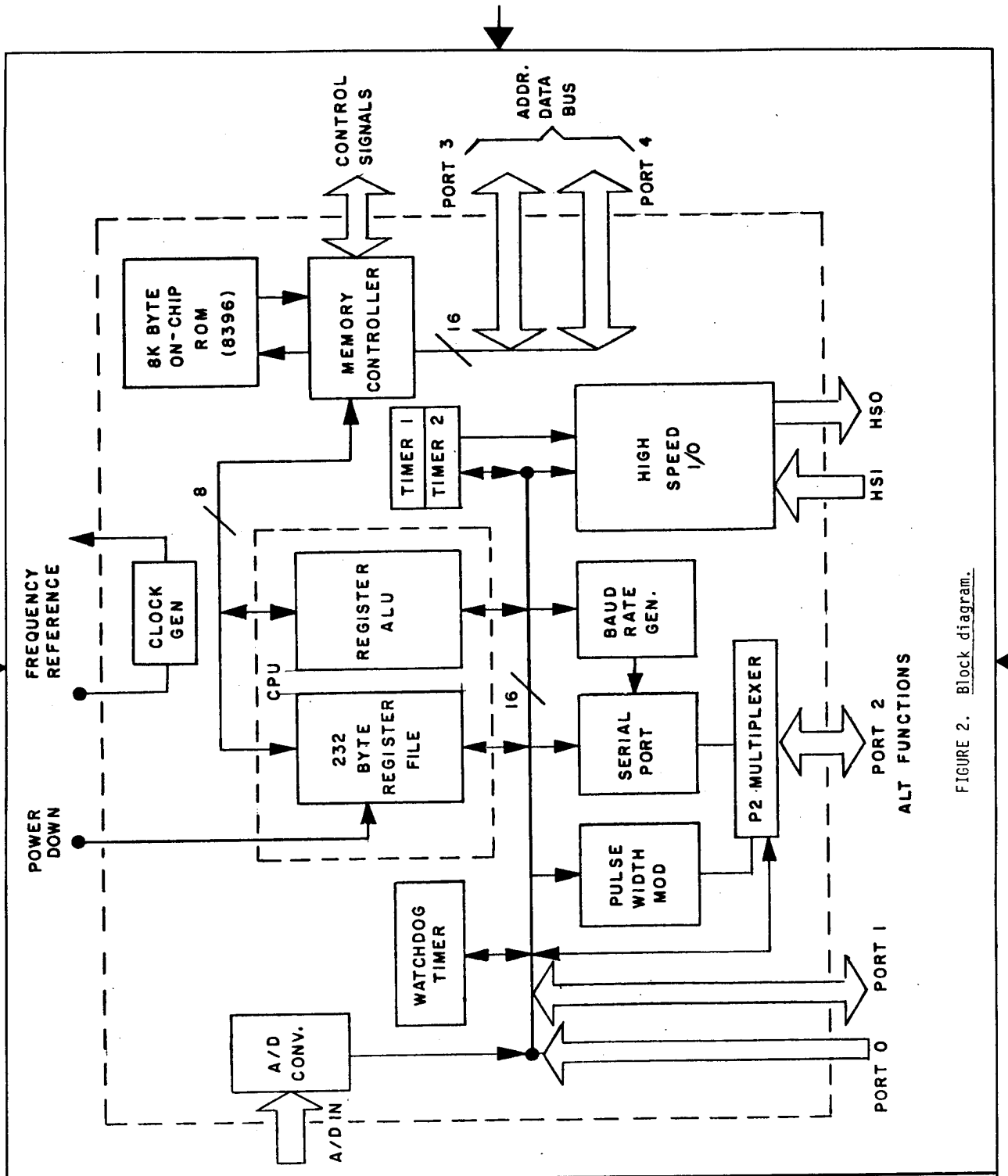

FIGURE 2. Block diagram.

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DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO

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Case Z

PINS FACING UP

	1	3	5	7	9	11	13	15	17	
68	2	4	6	8	10	12	14	16	19	18
66	67								21	20
64	65								23	22
62	63								25	24
60	61								27	26
58	59								29	28
56	57				BOTTOM VIEW				31	30
54	55								33	32
52	53	50	48	46	44	42	40	38	36	34
	51	49	47	45	43	41	39	37	35	

PINS FACING DOWN

	17	15	13	11	9	7	5	3	1	
18	19	16	14	12	10	8	6	4	2	68
20	21								67	66
22	23								65	64
24	25								63	62
26	27								61	60
28	29								59	58
30	31				TOP VIEW				57	56
32	33								55	54
34	36	38	40	42	44	46	48	50	53	52
	35	37	39	41	43	45	47	49	51	

FIGURE 3. Terminal connections.

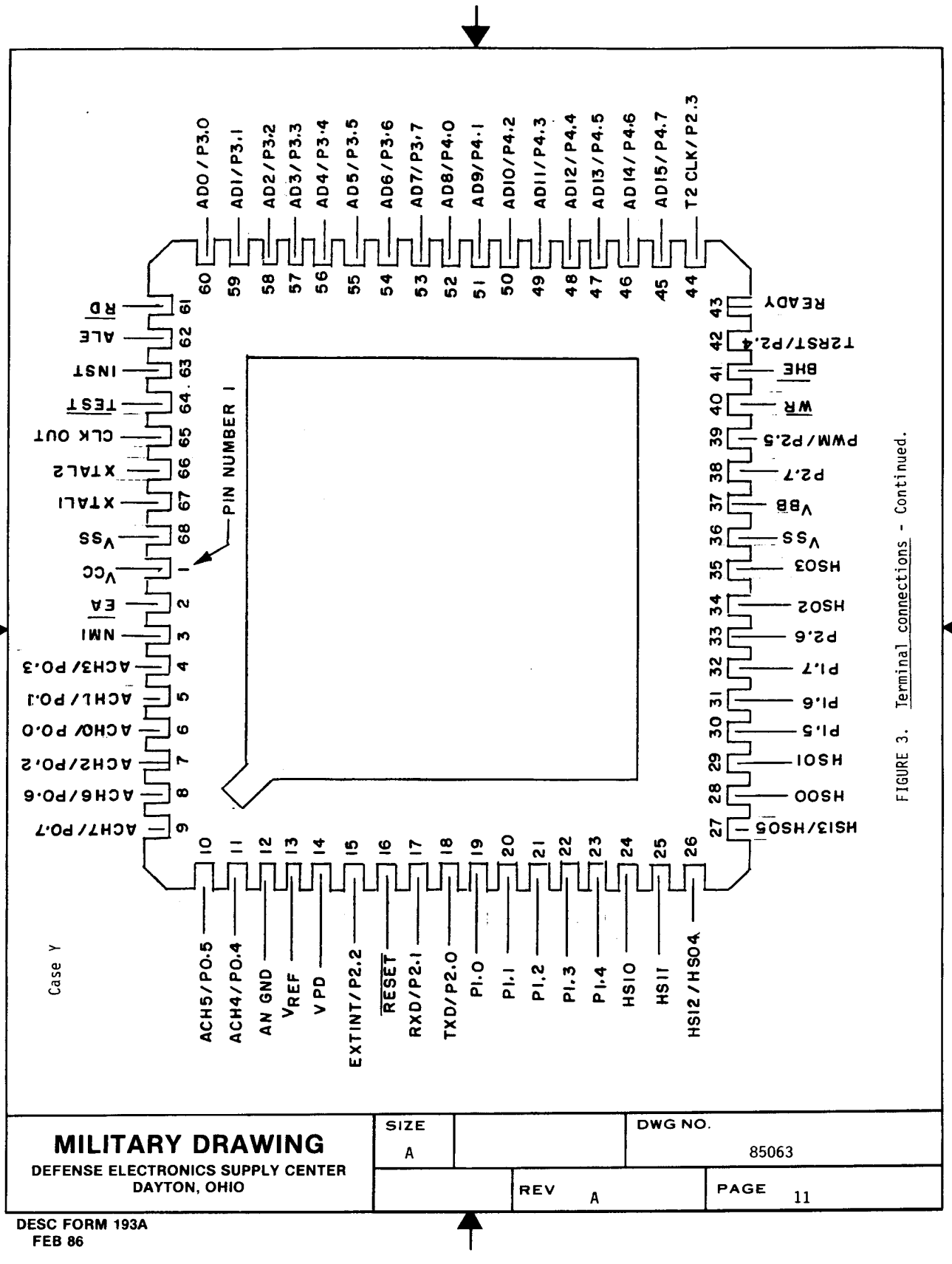

FIGURE 3. Terminal connections - Continued.

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Case Y

Case Z	Case Y	Description	Case Z	Case Y	Description	Case Z	Case Y	Description
1	9	ACH7/P0.7	24	54	AD6/P3.6	47	31	P1.6
2	8	ACH6/P0.6	25	53	AD7/P3.7	48	30	P1.5
3	7	ACH2/P0.2	26	52	AD8/P4.0	49	29	HSO.1
4	6	ACH0/P0.0	27	51	AD9/P4.1	50	28	HSO.0
5	5	ACH1/P0.1	28	50	AD10/P4.2	51	27	HSO.5/HSI.3
6	4	ACH3/P0.3	29	49	AD11/P4.3	52	26	HSO.4/HSI.2
7	3	$\overline{\text{NMI}}$	30	48	AD12/P4.4	53	25	HSI.1
8	2	$\overline{\text{EA}}$	31	47	AD13/P4.5	54	24	HSI.0
9	1	VCC	32	46	AD14/P4.6	55	23	P1.4
10	68	VSS	33	45	AD15/P4.7	56	22	P1.3
11	67	XTAL 1	34	44	T2CLK/P2.3	57	21	P1.2
12	66	XTAL 2	35	43	READY	58	20	P1.1
13	65	CLKOUT	36	42	T2RST/P2.4	59	19	P1.0
14	64	$\overline{\text{TEST}}$	37	41	$\overline{\text{BHE}}$	60	18	TXD/P2.0
15	63	INST	38	40	$\overline{\text{WR}}$	61	17	RXD/P2.1
16	62	ALE	39	39	PWM/P2.5	62	16	$\overline{\text{RESET}}$
17	61	$\overline{\text{RD}}$	40	38	P2.7	63	15	EXTINT/P2.2
18	60	AD0/P3.0	41	37	VBB	64	14	VPD
19	59	AD1/P3.1	42	36	VSS	65	13	VREF
20	58	AD2/P3.2	43	35	HSO.3	66	12	ANGND
21	57	AD3/P3.3	44	34	HSO.2	67	11	ACH4/P0.4
22	56	AD4/P3.4	45	33	P2.6	68	10	ACH5/P0.5
23	55	AD5/P3.5	46	32	P1.7			

FIGURE 3. Terminal connections - Continued.

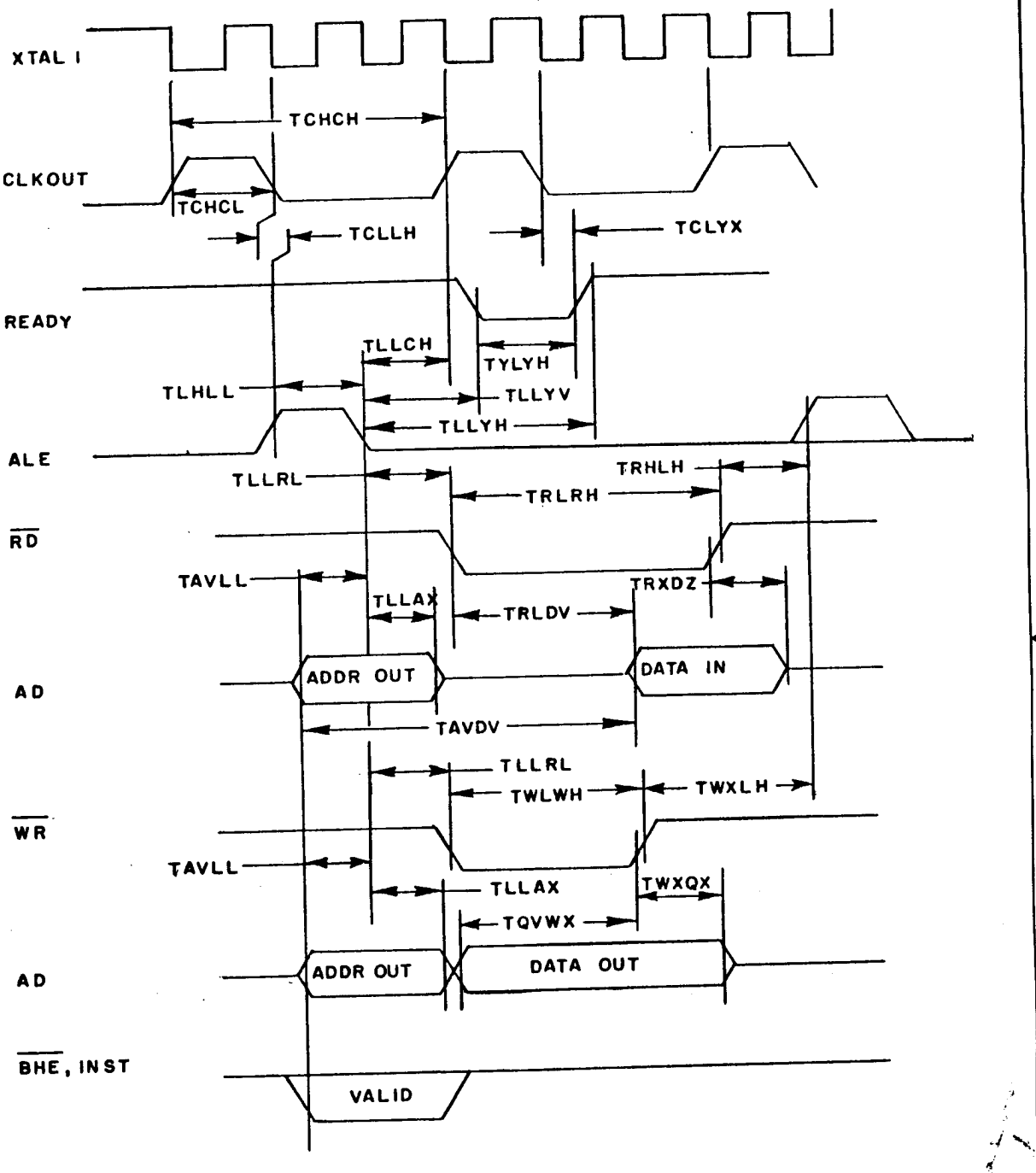

FIGURE 4. Waveform timing diagram.

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3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inpsection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_S measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Initial electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (+125°C only), 10

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8506301ZX	34649	MG8097/B
8506301YX	34649	MQ8097/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Rd. Chandler, AZ 85224