P33PCT139, 139A, 139B
HIGH-SPEED DUAL 1-OF-4 DECODER

ADVANCE INFORMATION

T-67-21-55

FEATURES

- 3.3V ± 0.2V Power Supply
- Center Power and Ground Pins
- Full CMOS Implementation
- Low Power Operation
- Dual 1-Of-4 Decoder with Enable
- I_{OL} = 48mA (commercial) and 32mA (military)
- Low Ground Bounce
- Fully TTL Compatible Input and Output Levels
- Produced with PACE Technology™
- Compact Pinout
  – 16-Pin 300 mil DIP, SOIC

DESCRIPTION

The P33PCT139, P33PCT139A and P33PCT139B are dual 1-of-4 decoders which have two independent decoders, each of which accept two binary weighted inputs (A_0–A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

The P33PCT139 is manufactured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 3.3V supply.

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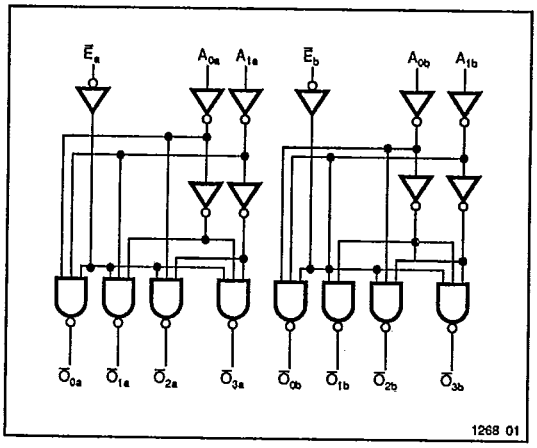
FUNCTIONAL BLOCK DIAGRAM



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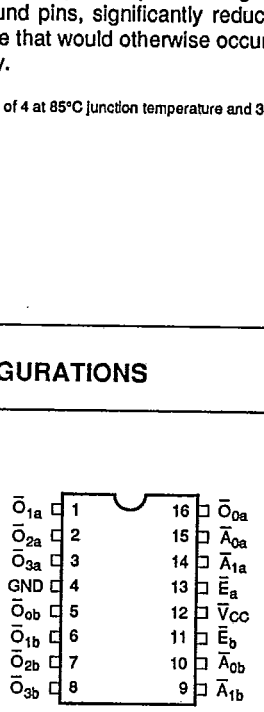
PIN CONFIGURATIONS



DIP (P10, D10) SOIC (S10)

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