FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13603-2E

16-bit Proprietary Microcontroller

CMOS

F²MC-16L MB90610A Series

MB90611A/MB90613A

■ DESCRIPTION

MB90610A series includes 16-bit microcontrollers optimally usable for high-speed real-time data processing in consumer appliances and for system control of printer, CD-ROM, celluar phone, copier, etc. The series uses the *F²MC-16L CPU which is based on the F²MC-16 but with enhanced high-level language and task switching instructions and additional addressing modes.

The internal peripheral resources consist of a 3-channel serial port incorporating a UART function (and supporting I/O expansion serial mode), 8-channel 10-bit A/D converter, 2-channel PPG, 2-channel 16-bit reload timer, 8-channel chip select output, and 8-channel external interrupts.

Also, multiplexed or non-multiplexed operation can be selected for the address/data bus.

*: "F²MC is an abbreviation for "Fujitsu Flexible Microcontroller".

■ FEATURE

- F²MC-16L CPU
- Minimum instruction execution time: 62.5 ns/4 MHz oscillation (Uses PLL clock multiplication), maximum multiplier = 4
- Instruction set optimized for controller applications
  Upward object code compatibility with F²MC-16 (H)
  Wide range of data types (bit/byte/word/long word)
  Improved instruction cycles provide increased speed
  Additional addressing modes: 23 modes
  High code efficiency
  Access methods (bank access/linear pointer)
  Enhanced multiplication and division instructions (signed instructions added)
  High precision operations are enhanced by use of a 32-bit accumulator
  Extended intelligent I/O service (access area extended to 64 Kbytes)
  Maximum memory space: 16 Mbytes

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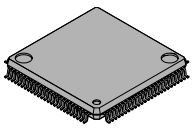
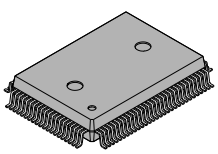
■ PACKAGE

100-pin Plastic LQFP	100-pin Plastic QFP
	
(FPT-100P-M05)	(FPT-100P-M06)

(Continued)

- Enhanced high level language (C)/multitasking support instructions
  Use of a system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
  Stack check function
- Improved execution speed: Four byte instruction queue
- Powerful interrupt function
- Automatic data transfer function (does not use instructions)

Internal peripherals

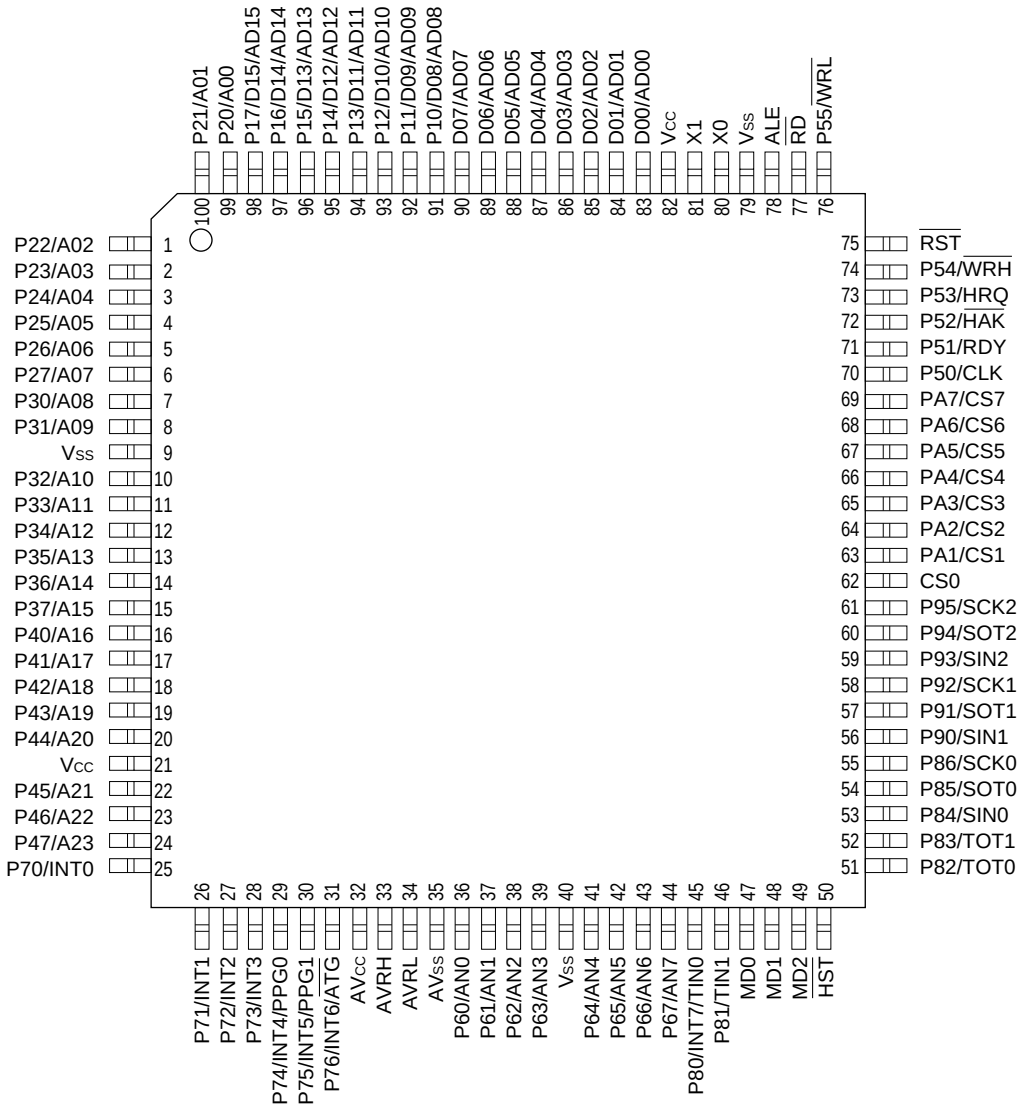
- RAM: 1 Kbyte (MB90611A) 3 Kbytes (MB90613A)
- General purpose ports 8, 16-bit data bus, multiplexed mode : 57 ports max.
  16-bit non-multiplexed mode : 41 ports max.
  8-bit non-multiplexed mode : 49 ports max.
- UART (SCI): 3 channels
  For either asynchronous or clocked serial transfer (I/O expansion serial)
- A/D converter: 8 channels (10-bit)
  8-bit conversion mode also available
- PPG (programmable pulse generator): 2 channels
- 16-bit reload timer: 2 channels
- Chip select output: 8 channels
- External interrupts: 8 channels
- 18-bit timebase timer
  Watchdog timer function
- PLL clock multiplier function
- CPU intermittent operation function
- Various standby modes
- LQFP-100/QFP-100 package
- CMOS technology

■ PRODUCT LINEUP

Part number / Parameter	MB90611A	MB90613A
Classification	Mask ROM	
ROM size	—	
RAM size	1 Kbyte	3 Kbytes
CPU functions	Number of basic instructions : 340 Instruction bit length : 8/16 bits Instruction length : 1 to 7 bytes Data bit length : 1/4/8/16/32 bits Minimum instruction execution time : 62.5 ns/4 MHz (PLL multiplier = 4) Interrupt processing time : 1000 ns/16 MHz (minimum)	
Ports	I/O ports (CMOS/TTL) : 33 (31 CMOS/2 TTL) (N-channel open drain): 8 (16-bit non-multiplex mode) Total : 41	
Packages	FPT-100P-M05 FPT-100P-M06	
UART (SCI)	Three internal UARTs Full-duplex, double-buffered Selectable clock synchronous or asynchronous operation Built-in dedicated baud rate generator	
A/D Converter	10-bit × 8 channels A/D conversion time : 6.13 µs (98 machine cycles/16 MHz machine clock, includes sample and hold time) Triggers : Software, external, or multi-function timer output (RT0) activation can be selected. Activation modes : Single, scan (continuous conversion of multiple channels), continuous (continuous conversion of one channel), and stop (scan mode with synchronized conversion start)	
PPG	2 × 8-bit PPG outputs (1 channel PPG output in 16-bit mode)	
16-Bit Reload Timer	16-bit reload timer operation (selectable toggle output, one-shot output) (Selectable count clock: 0.125 µs, 0.5 µs, or 2.0 µs for a 16 MHz machine cycle) Selectable event count function, 2 internal channels	
Chip select	8 outputs	
External interrupts	8 inputs External interrupt mode (Interrupts can be generated from four different types of request signal)	
PLL Function	Selectable multiplier: 1/2/3/4 (Set a multiplier that does not exceed the assured operation frequency range.)	
Other	—	

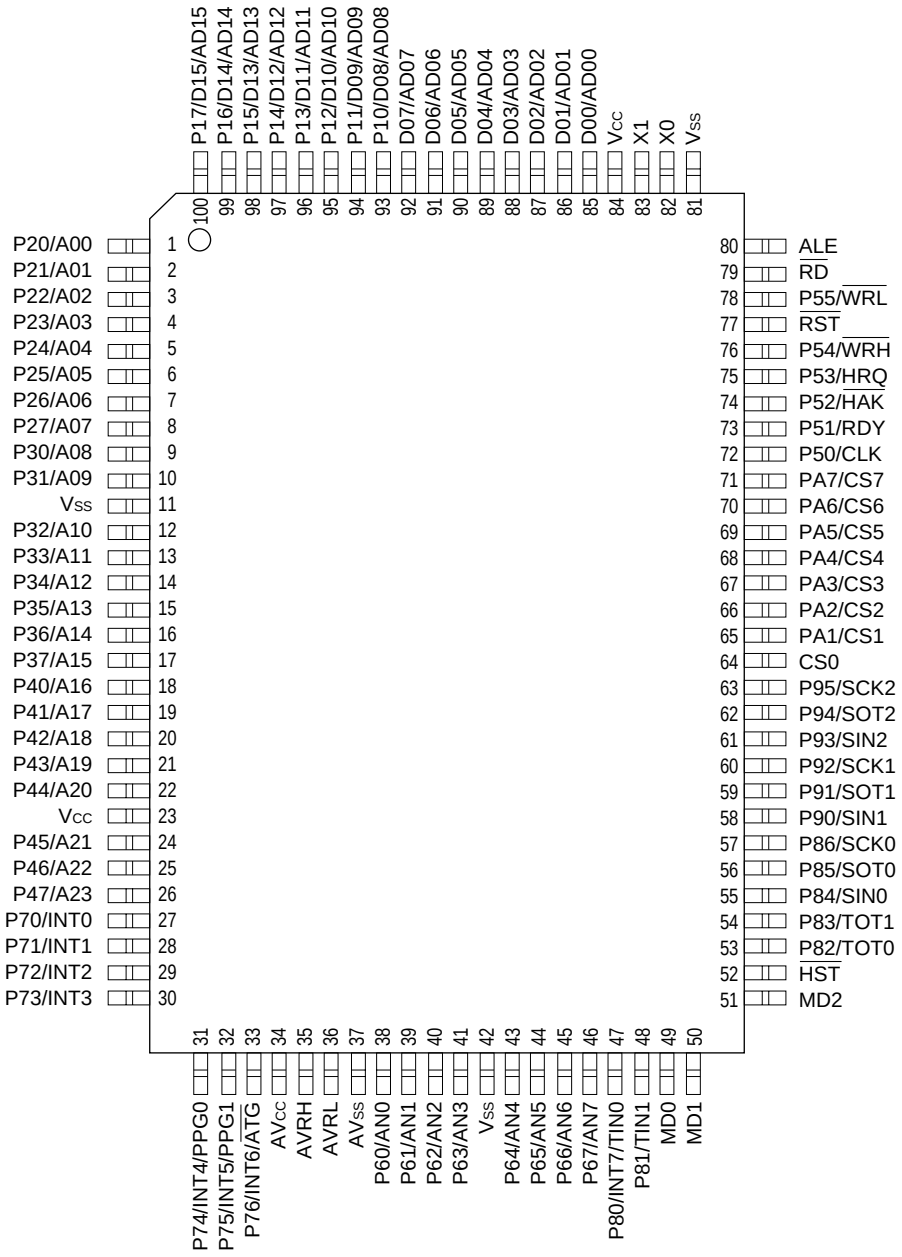
■ PIN ASSIGNMENT

(Top view)



(FPT-100P-M05)

(Top view)



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
80 81	82 83	X0 X1	A (Oscillator)	Crystal oscillator pins
83 to 90	85 to 92	D00 to D07	K (TTL)	In non-multiplex mode, the I/O pins for the lower 8 bits of the external data bus.
		AD00 to AD07		In multiplexed mode, the I/O pins for the lower 8 bits of the external address/data bus.
91 to 98	93 to 100	P10 to P17	K (TTL)	General purpose I/O ports This applies in non-multiplexed mode with an 8-bit external data bus.
		P08 to D15		In non-multiplexed mode, the I/O pins for the upper 8 bits of the external data bus This applies when using a 16-bit external data bus.
		AD08 to AD15		In multiplexed mode, the I/O pins for the upper 8 bits of the external address/data bus.
99 100 1 to 6	1 to 8	P20 to P27	B (CMOS)	General purpose I/O ports This applies in multiplexed mode.
		A00 to A07		In non-multiplexed mode, the output pins for the lower 8 bits of the external address bus.
7 8 10 to 15	9 10 12 to 17	P30 to P37	B (CMOS)	General purpose I/O ports This applies in multiplexed mode.
		A08 to A15		In non-multiplexed mode, the output pins for the upper 8 bits of the external address bus.
16 to 20 22 to 24	18 to 22 24 to 26	P40 to P47	B (CMOS)	General purpose I/O ports This applies when the upper address control register specifies port operation.
		A16 to A23		The output pins for A16 to 23 of the external address bus This applies when the upper address control register specifies address operation.
25 to 28	27 to 30	P70 to P73	H (CMOS/H)	General purpose I/O ports This applies in all cases.
		INT0 to INT3		External interrupt request input pins As the inputs operate continuously when external interrupts are enabled, output to the pins from other functions must be stopped unless done intentionally.

*1: FPT-100P-M05
*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
29 30	31 32	P74, P75	H (CMOS/H)	General purpose I/O ports This applies when the waveform outputs for PPG timers 0 to 1 are disabled.
		INT4, INT5		External interrupt request input pins As the inputs operate continuously when external interrupts are enabled, output to the pins from other functions must be stopped unless done intentionally.
		PPG0, PPG1		Output pins for PPG timers 0 to 1 This applies when the waveform outputs for PPG timers 0 to 1 are enabled.
31	33	P76	H (CMOS/H)	General purpose I/O port This applies in all cases.
		INT6	H (CMOS/H)	External interrupt request input pin As the input operates continuously when the external interrupt is enabled, output to the pin from other functions must be stopped unless done intentionally.
		$\overline{ATG}$		Trigger input pin for the A/D converter As the input operates continuously when the A/D converter inputs are operating, output to the pin from other functions must be stopped unless done intentionally.
32	34	AV_{CC}	Power supply	Power supply for the analog circuits Do not switch this power supply on/off unless a voltage greater than AV_{CC} is applied to V_{CC}.
33	35	AVRH	Power supply	Analog circuit reference voltage input Do not switch the voltage to this pin on/off unless a voltage greater than AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	Analog circuit reference voltage input
35	37	AV_{SS}	Power supply	Ground level for the analog circuits
36 to 39 41 to 44	38 to 41 43 to 46	P60 to P67	C (AD)	Open-drain output ports This applies when port operation is specified in the analog input enable register.
		AN0 to AN7		Analog input pins for the A/D converter This applies when analog input mode operation is specified in the analog input enable register.
45	47	P80	H (CMOS/H)	General purpose I/O port This applies in all cases.
		INT7		External interrupt request input pin As the input operates continuously when the external interrupt is enabled, output to the pin from other functions must be stopped unless done intentionally.
		TIN0		Event input pin for reload timer 0 As the input operates continuously when the reload timer is set to input operation, output to the pin from other functions must be stopped unless done intentionally.

(Continued)

*1: FPT-100P-M05
*2: FPT-100P-M06

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
46	48	P81	D (CMOS/H)	General purpose I/O port This applies in all cases.
		TIN1		Event input pin for reload timer 1 As the input operates continuously when the reload timer is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
47, 48	49, 50	MD0, MD1	E (CMOS/H)	Input pins for specifying an oprating mode Do not connect directly to V_{CC} or V_{SS}.
49	51	MD2	M (CMOS/H)	Input pins for specifying an oprating mode Do not connect directly to V_{CC} or V_{SS}.
50	52	$\overline{HST}$	F (CMOS/H)	Hardware standby input pin
51, 52	53, 54	P82, P83	D (CMOS/H)	General purpose I/O ports This applies when output is disabled for reload timers 0 to 1.
		TOT0, TOT1		Output pins for reload timers 0 to 1 This applies when output is enabled for reload timers 0 to 1.
53	55	P84	D (CMOS/H)	General purpose I/O port This applies in all cases.
		SIN0		Serial data input pin for UART0 As the input operates continuously when UART0 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
54	56	P85	D (CMOS/H)	General purpose I/O port This applies when serial data output is disabled for UART0.
		SOT0		Serial data output pin for UART0 This applies when serial data output is enabled for UART0.
55	57	P86	D (CMOS/H)	General purpose I/O port This applies when the UART0 clock output is disabled.
		SCK0		Clock I/O pin for UART0 This applies when the UART0 clock output is enabled. As the input operates continuously when UART0 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
56	58	P90	D (CMOS/H)	General purpose I/O port This applies in all cases.
		SIN1		Serial data input pin for UART1 As the input operates continuously when UART1 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.

(Continued)

*1: FPT-100P-M05
*2: FPT-100P-M06

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
57	59	P91	D (CMOS/H)	General purpose I/O port This applies when serial data output is disabled for UART1.
		SOT1		Serial data output pin for UART1 This applies when serial data output is enabled for UART1.
58	60	P92	D (CMOS/H)	General purpose I/O port This applies when the UART1 clock output is disabled.
		SCK1		Clock I/O pin for UART1 This applies when the UART1 clock output is enabled. As the input operates continuously when UART1 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
59	61	P93	D (CMOS/H)	General purpose I/O port This applies in all cases.
		SIN2		Serial data input pin for UART2 As the input operates continuously when UART2 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
60	62	P94	D (CMOS/H)	General purpose I/O port This applies when serial data output is disabled for UART2.
		SOT2		Serial data output pin for UART2 This applies when serial data output is enabled for UART2.
61	63	P95	D (CMOS/H)	General purpose I/O port This applies when the UART2 clock output is disabled.
		SCK2		Clock I/O pin for UART2 This applies when the UART2 clock output is enabled. As the input operates continuously when UART2 is set to input operation, output to the pin from other functions must be stopped unless done intentionally.
62	64	CS0	J (CMOS)	Chip select pin for program ROM
63 to 69	65 to 71	PA1 to PA7	I (CMOS)	General purpose I/O ports This applies for pins with chip select output disabled by the chip select control register.
		CS1 to CS7		Output pins for the chip select function This applies for pins with chip select output enabled by the chip select control register.
70	72	P50	I (CMOS)	General purpose I/O port This applies when CLK output is enabled.
		CLK		CLK output pin

*1: FPT-100P-M05
*2: FPT-100P-M06

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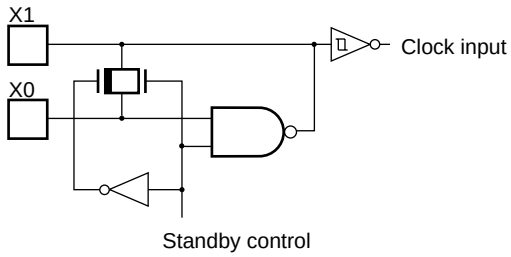
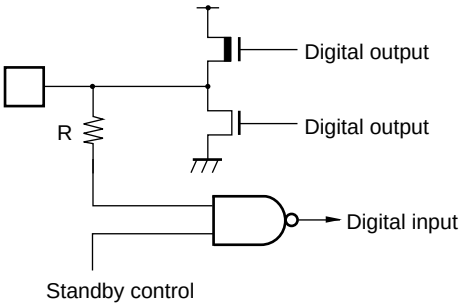
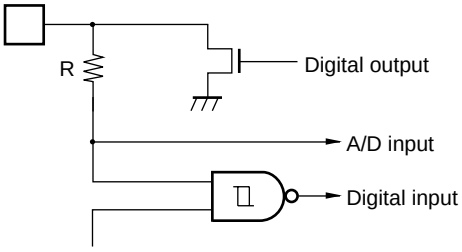
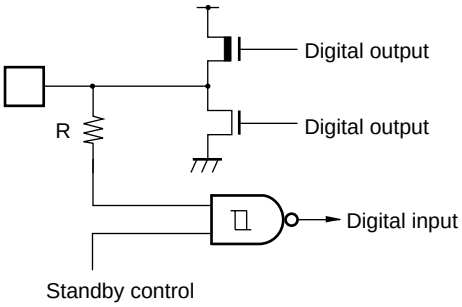
Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
71	73	P51	L (TTL)	General purpose I/O port This applies when the external ready function is disabled.
		RDY		Ready input pin This applies when the external ready function is enabled.
72	74	P52	I (CMOS)	General purpose I/O port This applies when the hold function is disabled.
		$\overline{HAK}$		Hold acknowledge output pin This applies when the hold function is enabled.
73	75	P53	L (TTL)	General purpose I/O port This applies when the hold function is disabled.
		HRQ		Hold request input pin This applies when the hold function is enabled.
74	76	P54	I (CMOS)	General purpose I/O port This applies in 8-bit external bus mode or when output is disabled for the WR pin.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the data bus This applies in 16-bit external bus mode and when output is enabled for the WR pin.
75	77	$\overline{RST}$	G (CMOS/H)	External reset request input pin
76	78	P55	I (CMOS)	General purpose I/O port This applies when output is disabled for the WR pin.
		$\overline{WRL}$		Write strobe output pin for the lower 8 bits of the data bus This applies when output is enabled for the WR pin.
77	79	$\overline{RD}$	J (CMOS)	Read strobe output pin for the data bus
78	80	ALE	J (CMOS)	ALE (address latch enabling) output pin
21, 82	23, 84	V_{CC}	Power supply	Power supply for the digital circuits
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Ground level for the digital circuits

*1: FPT-100P-M05
*2: FPT-100P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Max. 3 to 32 MHz • Oscillator feedback resistance: approximately 1 MΩ
B		• CMOS level I/O With standby control • Pull-up resistor option
C		• N-channel open drain output • CMOS level hysteresis input With AD control • Pull-up resistor option
D		• CMOS level output • CMOS level hysteresis input With standby control • Pull-up resistor option

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

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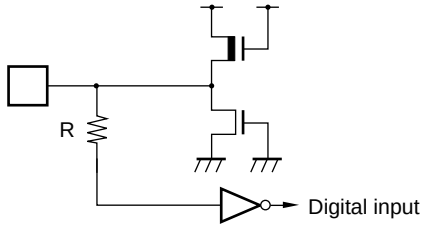
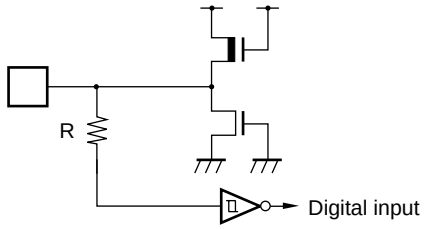
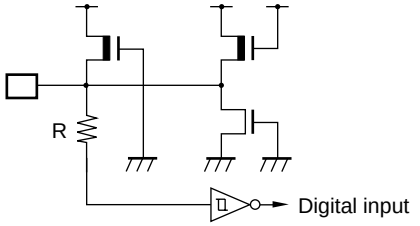
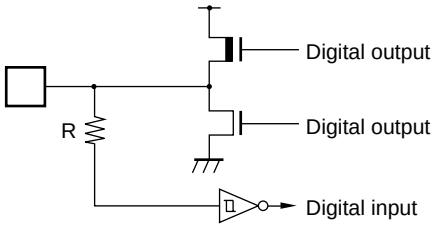
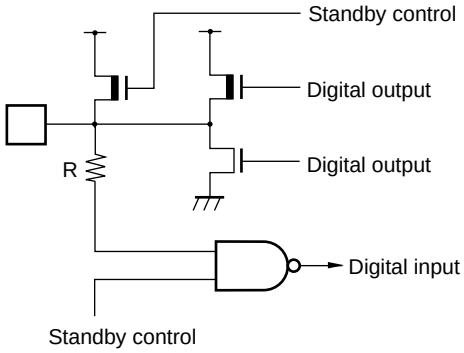
Type	Circuit	Remarks
E		• CMOS level input No standby control • Pull-up resistor option
F		• CMOS level hysteresis input No standby control • Pull-up resistor option
G		• CMOS level hysteresis input No standby control • With pull-up
H		• CMOS level output • CMOS level hysteresis input No standby control • Pull-up resistor option
I		• CMOS level I/O • Pull-up resistor approximately 50 KΩ • Pin goes to high impedance during stop mode.

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

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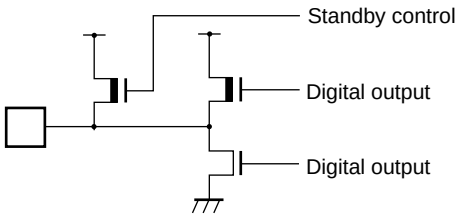
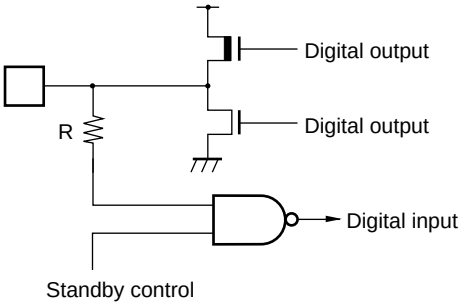
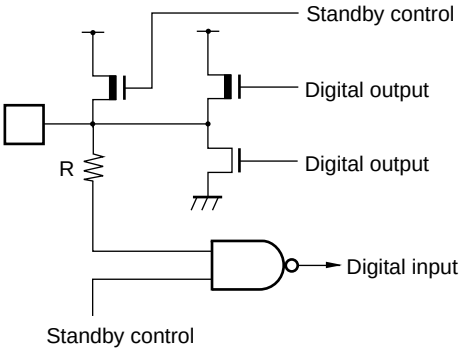
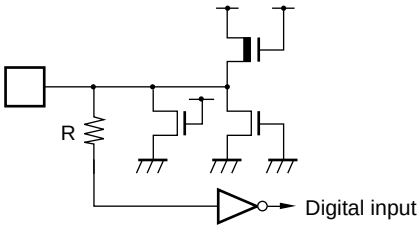
Type	Circuit	Remarks
J		• CMOS level output • Pull-up resistor approximately 50 KΩ • Pin goes to high impedance during stop mode.
K		• CMOS level output • TTL level input With standby control • Pull-up resistor option
L		• CMOS level output • TTL level input • Pull-up resistor approximately 50 KΩ • Pin goes to high impedance during stop mode.
M		• CMOS level input No standby control • Pull-up resistor option

Note: For pins with pull-up resistors, the resistance is disconnected when the pin outputs the “L” level or when in the standby state.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup occurs in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if the voltage applied between V_{CC} and V_{SS} exceeds the rating.
If latchup occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.
For the same reason, also ensure that the analog supply voltage does not exceed the digital supply voltage.

2. Treatment of Unused Pins

Leaving unused input pins unconnected can cause misoperation. Always pull-up or pull-down unused pins.

3. External Reset Input

To reliably reset the controller by inputting an “L” level to the $\overline{RST}$ pin, ensure that the “L” level is applied for at least five machine cycles. Take particular note when using an external clock input.

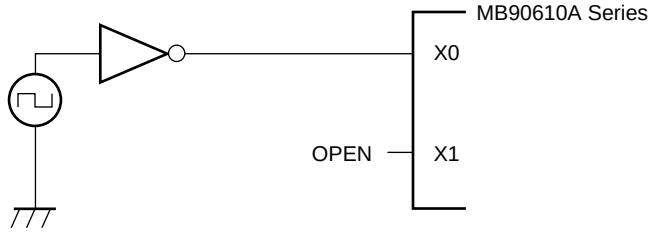
4. V_{CC} and V_{SS} Pins

Ensure that all V_{CC} pins are at the same voltage. The same applies for the V_{SS} pins.

5. Cautions When Using an External Clock

Drive the X0 pin only when using an external clock.

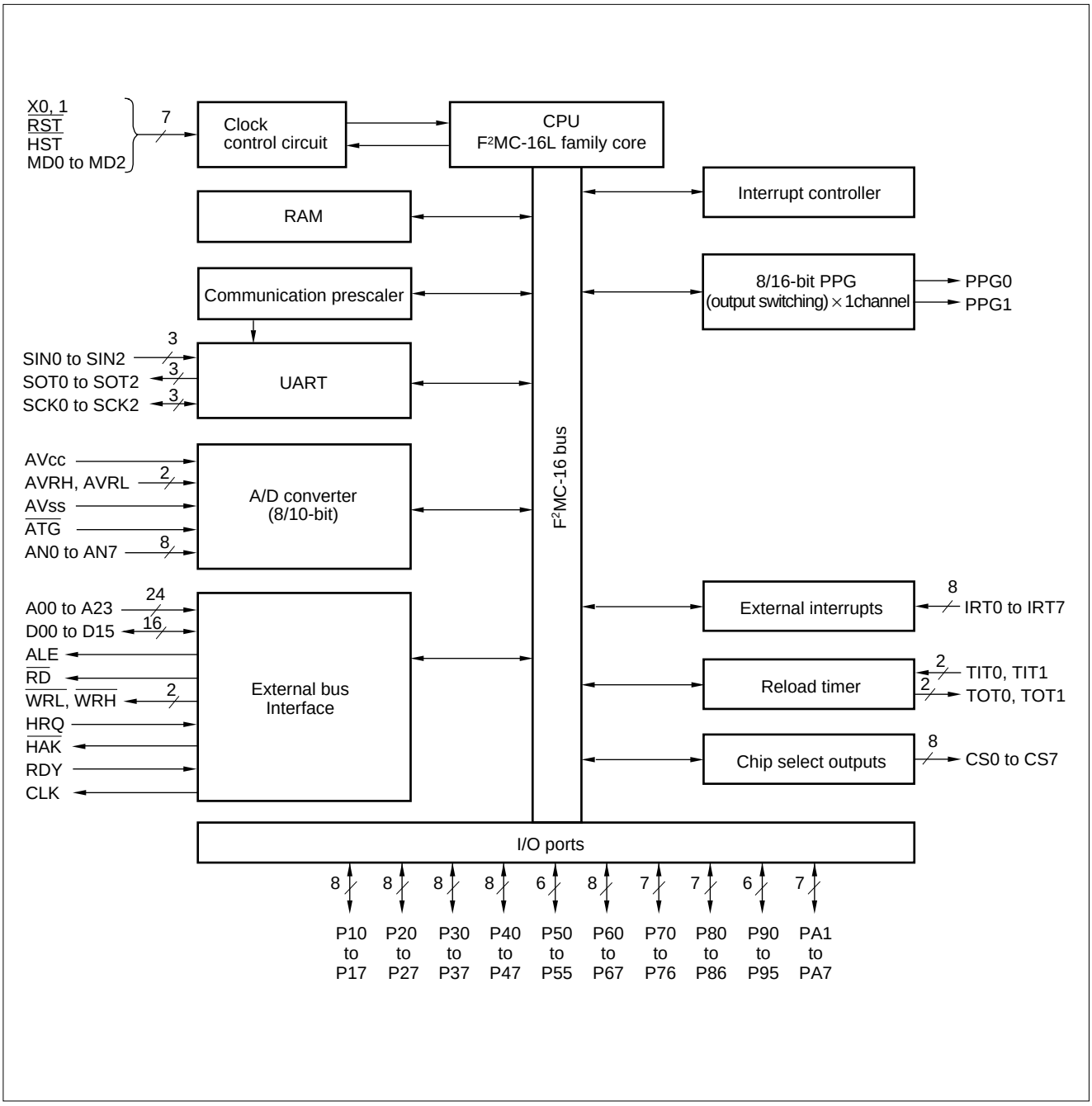
- **Using an External Clock**



6. A/D Converter Power Supply and the Turn-on Sequence for Analog Inputs

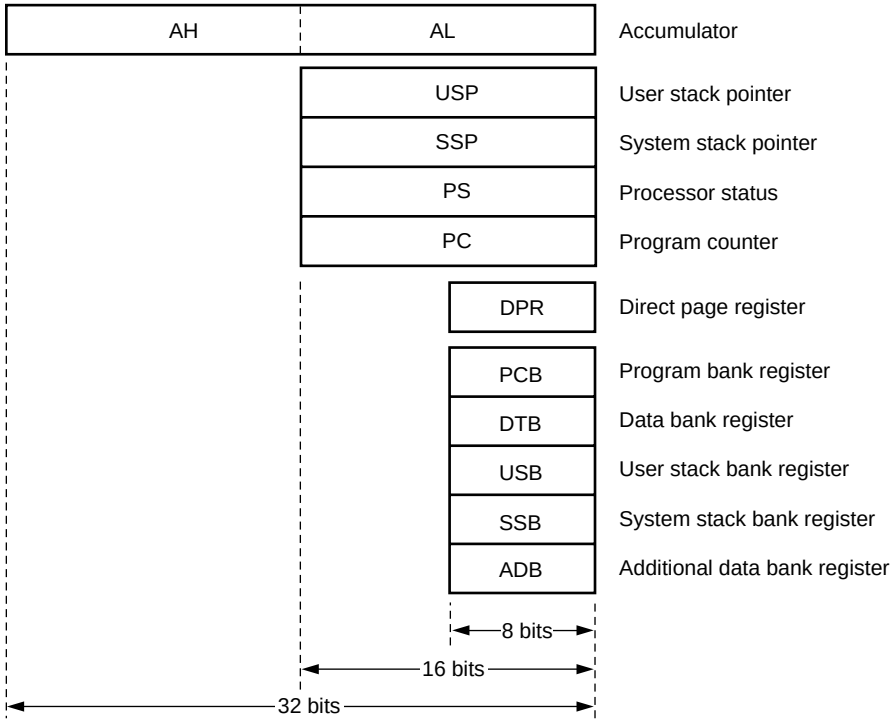
Always cut the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) before disconnecting the digital power supply (V_{CC}).
When turning the power on or off, ensure that AVRH does not exceed AV_{CC}.
Also, when using the analog input pins as input ports, ensure that the input voltage does not exceed AV_{CC}.

■ BLOCK DIAGRAM

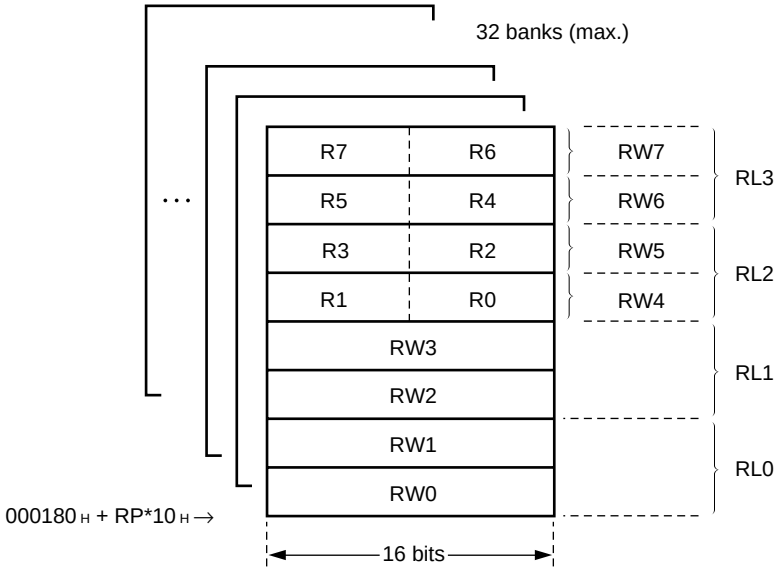


■ F²MC-16L CPU PROGRAMMING MODEL

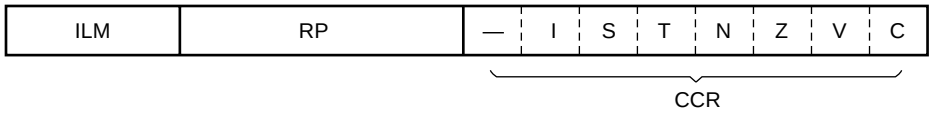
- **Dedicated Registers**



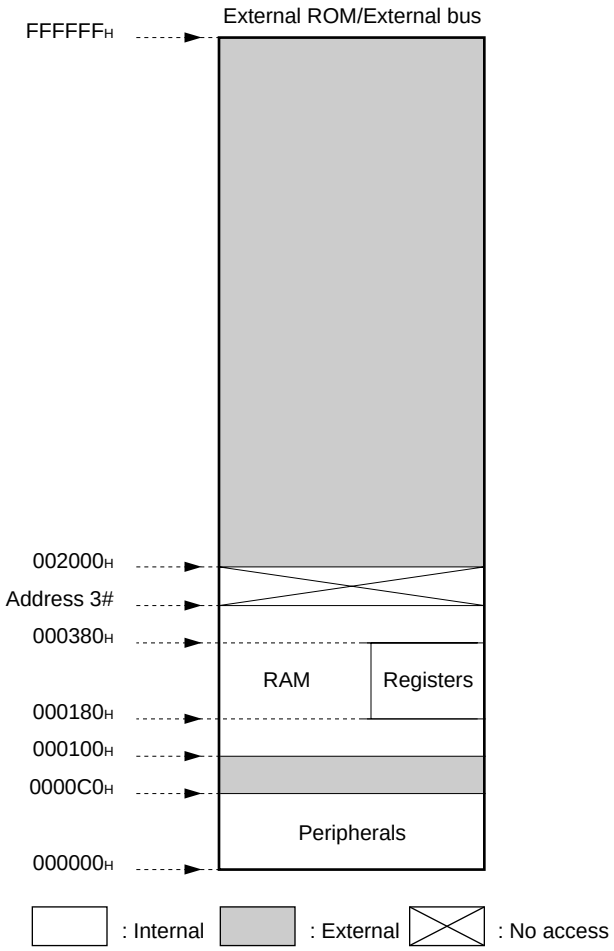
- **General-purpose Registers**



- **Processor States (PS)**



■ MEMORY MAP



Type	Address #3
MB90611A	000500H
MB90613A	000D00H

■ I/O MAP

Address	Register	Name	Access	Resource name	Initial value
000000H	Free	—	*3	—	—
000001H	Port 1 data register	PDR1	R/W*	Port 1*8	XXXXXXXX
000002H	Port 2 data register	PDR2	R/W*	Port 2*7	XXXXXXXX
000003H	Port 3 data register	PDR3	R/W*	Port 3*7	XXXXXXXX
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
000005H	Port 5 data register	PDR5	R/W	Port 5	– – XXXXXX
000006H	Port 6 data register	PDR6	R/W	Port 6	11111111
000007H	Port 7 data register	PDR7	R/W	Port 7	– XXXXXXX
000008H	Port 8 data register	PDR8	R/W	Port 8	– XXXXXXX
000009H	Port 9 data register	PDR9	R/W	Port 9	– – XXXXXX
00000AH	Port A data register	PDRA	R/W	Port A	XXXXXXX –
00000BH to 10H	Vacancy	—	*3	—	—
000011H	Port 1 direction register	DDR1	R/W*	Port 1*8	00000000
000012H	Port 2 direction register	DDR2	R/W*	Port 2*7	00000000
000013H	Port 3 direction register	DDR3	R/W*	Port 3*7	00000000
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000
000015H	Port 5 direction register	DDR5	R/W	Port 5	– – 000000
000016H	Analog input enable register	ADER	R/W	Port 6	11111111
000017H	Port 7 direction register	DDR7	R/W	Port 7	– 0000000
000018H	Port 8 direction register	DDR8	R/W	Port 8	– 0000000
000019H	Port 9 direction register	DDR9	R/W	Port 9	– – 000000
00001AH	Port A direction register	DDRA	R/W	Port A	0000000 –
00001BH to 1FH	Vacancy	—	*3	—	—
000020H	Serial mode register 0	SMR0	R/W!	UART0 (SCI)	00000000
000021H	Serial control register 0	SCR0	R/W!		00000100
000022H	Serial input data register 0/ Serial output data register 0	SIDR0/ SODR0	R/W		XXXXXXXX
000023H	Serial status register 0	SSR0	R/W!		00001 – 00
000024H	Serial mode register 1	SMR1	R/W!	UART1 (SCI)	00000000
000025H	Serial control register 1	SCR1	R/W!		00000100
000026H	Serial input data register 1/ Serial output data register 1	SIDR1/ SODR1	R/W		XXXXXXXX
000027H	Serial status register 1	SSR1	R/W!		00001 – 00

(Continued)

Address	Register	Name	Access	Resource name	Initial value
000028H	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0
000029H	Interrupt/DTP request register	EIRR	R/W		0 0 0 0 0 0 0 0
00002AH	Interrupt level setting register	ELVR	R/W		0 0 0 0 0 0 0 0
00002BH					0 0 0 0 0 0 0 0
00002CH	AD control status register	ADCS	R/W!	A/D converter	0 0 0 0 0 0 0 0
00002DH					0 0 0 0 0 0 0 0
00002EH	AD data register	ADCR	R/W! *4		X X X X X X X X
00002FH					0 0 0 0 0 0 X X
000030H	PPG0 operation mode control register	PPGC0	R/W	PPG0	0 0 0 0 0 0 – 1
000031H	PPG1 operation mode control register	PPGC1	R/W	PPG1	0 0 0 0 0 0 – 1
000032H, 33H	Vacancy	—	*3	—	—
000034H	PPG0 reload register	PRL0	R/W	PPG0	X X X X X X X X
000035H					X X X X X X X X
000036H	PPG1 reload register	PRL1	R/W	PPG1	X X X X X X X X
000037H					X X X X X X X X
000038H	Control status register	TMCSR0	R/W!	16-bit reload timer 0	0 0 0 0 0 0 0 0
000039H					– – – – 0 0 0 0
00003AH	16-bit timer register/ 16-bit reload register	TMR0/ TMRLR0	R/W		X X X X X X X X
00003BH					X X X X X X X X
00003CH	Control status register	TMCSR1	R/W!	16-bit reload timer 1	0 0 0 0 0 0 0 0
00003DH					– – – – 0 0 0 0
00003EH	16-bit timer register/ 16-bit reload register	TMR1/ TMRLR1	R/W		X X X X X X X X
00003FH					X X X X X X X X
000040H to 43H	Vacancy	—	*3	—	—
000044H	Serial mode register 2	SMR2	R/W!	UART2 (SCI)	0 0 0 0 0 0 0 0
000045H	Serial control register 2	SCR2	R/W!		0 0 0 0 0 1 0 0
000046H	Serial input data register 2/ Serial output data register 2	SIDR2/ SODR2	R/W		X X X X X X X X
000047H	Serial status register 2	SSR2	R/W!		0 0 0 0 1 – 0 0
000048H	CS control register 0	CSCR0	R/W	Chip select function	– – – – 0 0 0 0
000049H	CS control register 1	CSCR1	R/W		– – – – 0 0 0 0
00004AH	CS control register 2	CSCR2	R/W		– – – – 0 0 0 0
00004BH	CS control register 3	CSCR3	R/W		– – – – 0 0 0 0

(Continued)

Address	Register	Name	Access*2	Resource name	Initial value
00004C$_H$	CS control register 4	CSCR4	R/W	Chip select function	– – – – 0 0 0 0
00004D$_H$	CS control register 5	CSCR5	R/W		– – – – 0 0 0 0
00004E$_H$	CS control register 6	CSCR6	R/W		– – – – 0 0 0 0
00004F$_H$	CS control register 7	CSCR7	R/W		– – – – 0 0 0 0
000050$_H$	Vacancy	—	*3	—	—
000051$_H$	UART0 (SCI) machine clock division control register	CDCR0	W	UART0 (SCI)	– – – – 1 1 1 1
000052$_H$	Vacancy	—	*3	—	—
000053$_H$	UART1 (SCI) machine clock division control register	CDCR1	W	UART1 (SCI)	– – – – 1 1 1 1
000054$_H$	Vacancy	—	*3	—	—
000055$_H$	UART2 (SCI) machine clock division control register	CDCR2	W	UART2 (SCI)	– – – – 1 1 1 1
000056$_H$ to 8F$_H$	Vacancy	—	*3	—	—
000090$_H$ to 9E$_H$	Reserved system area	—	*1	—	—
00009F$_H$	Delayed interrupt generate/ release register	DIRR	R/W	Delayed interrupt generation module	– – – – – – – 0
0000A0$_H$	Low power consumption mode control register	LPMCR	R/W!	Low power consumption	0 0 0 1 1 0 0 0
0000A1$_H$	Clock selection register	CKSCR	R/W!	Low power consumption	1 1 1 1 1 1 0 0
0000A2$_H$ to A4$_H$	Vacancy	—	*3	—	—
0000A5$_H$	Auto-ready function selection register	ARSR	W	External pins	0 0 1 1 – – 0 0
0000A6$_H$	External address output control register	HACR	W	External pins	0 0 0 0 0 0 0 0
0000A7$_H$	Bus control signal selection register	ECSR	W	External pins	– 0 0 0 * 0 0 0
0000A8$_H$	Watchdog timer control register	WDTC	R/W!	Watchdog timer	X X X X X 1 1 1
0000A9$_H$	Timebase timer control register	TBTC	R/W!	Timebase timer	1 – – 0 0 1 0 0
0000AA$_H$ to AF$_H$	Vacancy	—	*3	—	—
0000B0$_H$	Interrupt control register 00	ICR00	R/W!	Interrupt controller	0 0 0 0 0 1 1 1
0000B1$_H$	Interrupt control register 01	ICR01	R/W!		0 0 0 0 0 1 1 1
0000B2$_H$	Interrupt control register 02	ICR02	R/W!		0 0 0 0 0 1 1 1
0000B3$_H$	Interrupt control register 03	ICR03	R/W!		0 0 0 0 0 1 1 1
0000B4$_H$	Interrupt control register 04	ICR04	R/W!		0 0 0 0 0 1 1 1
0000B5$_H$	Interrupt control register 05	ICR05	R/W!		0 0 0 0 0 1 1 1

(Continued)

(Continued)

Address	Register	Name	Access	Resource name	Initial value
0000B6H	Interrupt control register 06	ICR06	R/W!	Interrupt controller	0 0 0 0 0 1 1 1
0000B7H	Interrupt control register 07	ICR07	R/W!		0 0 0 0 0 1 1 1
0000B8H	Interrupt control register 08	ICR08	R/W!		0 0 0 0 0 1 1 1
0000B9H	Interrupt control register 09	ICR09	R/W!		0 0 0 0 0 1 1 1
0000BAH	Interrupt control register 10	ICR10	R/W!		0 0 0 0 0 1 1 1
0000BBH	Interrupt control register 11	ICR11	R/W!		0 0 0 0 0 1 1 1
0000BCH	Interrupt control register 12	ICR12	R/W!		0 0 0 0 0 1 1 1
0000BDH	Interrupt control register 13	ICR13	R/W!		0 0 0 0 0 1 1 1
0000BEH	Interrupt control register 14	ICR14	R/W!		0 0 0 0 0 1 1 1
0000BFH	Interrupt control register 15	ICR15	R/W!		0 0 0 0 0 1 1 1
0000C0H to FFH	External area *2	—	—	—	—

Initial values
- 0 : The initial value for this bit is “0”.
- 1 : The initial value for this bit is “1”.
- * : The initial value for this bit is “1” or “0”. (Determined by the level of the MD0 to MD2 pins.)
- X : The initial value for this bit is undefined.
- – : This bit is not used. The initial value is undefined.

*1: Access prohibited.

*2: This is the only external access area in the area below address 0000FFH. Access this address as an external I/O area.

*3: Areas marked as “free” in the I/O map are reserved areas. These areas are accessed by internal access. No access signals are output on the external bus.

*4: Only bit 15 can be written. The other bits are written to by the test function. Reading bits 10 to 15 returns zeros.

*5: The R/W! symbol in the Read/Write column indicates that some bits are read-only or write-only. See the resource’s register list for details.

6: Using a read-modify-write instruction (such as the bit set instruction) to access one of the registers indicated by R/W!, R/W, or W in the Read/Write column sets the specified bit to the desired value. However, this can cause misoperation if the other register bits include write-only bits. Therefore, do not use read-modify-write instructions to access these registers.

*7: This register is only available when the address/data bus is in multiplex mode. Access to the register is prohibited in non-multiplex mode.

*8: This register is only available when the external data bus is in 8-bit mode. Access to the register is prohibited in 16-bit mode.

Note: The initial values listed for write-only bits are the initial values set by a reset. They are not the values returned by a read.
Also, LPMCR/CKSCR/WDTC are sometimes initialized and sometimes not initialized, depending on the reset type. The listed initial values are for when these registers are initialized.

■ INTERRUPT VECTOR AND INTERRUPT CONTROL REGISTER ASSIGNMENTS TO INTERRUPT SOURCES

Interrupt source	I²OS support	Interrupt vector			Interrupt control register	
		Number		Address	ICR	Address
Reset	×	#08	08_H	$FFFFDC_H$	—	—
INT 9 instruction	×	#09	09_H	$FFFFD8_H$	—	—
Exception	×	#10	$0A_H$	$FFFFD4_H$	—	—
External interrupt #0	○	#11	$0B_H$	$FFFFD0_H$	ICR00	$0000B0_H$
External interrupt #1	○	#13	$0D_H$	$FFFFC8_H$	ICR01	$0000B1_H$
External interrupt #2	○	#15	$0F_H$	$FFFFC0_H$	ICR02	$0000B2_H$
External interrupt #3	○	#17	11_H	$FFFFB8_H$	ICR03	$0000B3_H$
External interrupt #4	○	#19	13_H	$FFFFB0_H$	ICR04	$0000B4_H$
External interrupt #5	○	#21	15_H	$FFFFA8_H$	ICR05	$0000B5_H$
External interrupt #6	○	#23	17_H	$FFFFA0_H$	ICR06	$0000B6_H$
UART0 • transmit complete	○	#24	18_H	$FFFF9C_H$		
External interrupt #7	○	#25	19_H	$FFFF98_H$	ICR07	$0000B7_H$
UART1 • transmit complete	○	#26	$1A_H$	$FFFF94_H$		
PPG #0	×	#27	$1B_H$	$FFFF90_H$	ICR08	$0000B8_H$
PPG #1	×	#28	$1C_H$	$FFFF8C_H$		
16-bit reload timer #0	○	#29	$1D_H$	$FFFF88_H$	ICR09	$0000B9_H$
16-bit reload timer #1	○	#30	$1E_H$	$FFFF84_H$		
A/DC measurement complete	○	#31	$1F_H$	$FFFF80_H$	ICR10	$0000BA_H$
UART2 • transmit complete	○	#33	21_H	$FFFF78_H$	ICR11	$0000BB_H$
Timebase timer interval interrupt	×	#34	22_H	$FFFF74_H$		
UART2 • receive complete	◎	#35	23_H	$FFFF70_H$	ICR12	$0000BC_H$
UART1 • receive complete	◎	#37	25_H	$FFFF68_H$	ICR13	$0000BD_H$
UART0 • receive complete	◎	#39	27_H	$FFFF60_H$	ICR14	$0000BE_H$
Delayed interrupt generation module	×	#42	$2A_H$	$FFFF54_H$	ICR15	$0000BF_H$

○ : indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal (no stop request).
◎ : indicates that the interrupt request flag is cleared by the I²OS interrupt clear signal (with stop request).
× : indicates that the interrupt request flag is not cleared by the I²OS interrupt clear signal.

Note: Do not specify I²OS activation in interrupt control registers that do not support I²OS.

■ PERIPHERAL RESOURCES

1. Parallel Port

The MB90610A series has 58 I/O pins, 18 output pins, and 8 open drain output pins.
Ports 1 to 5 and ports 7 to A are I/O ports. The ports are inputs when the corresponding direction register bit is "0" and outputs when the corresponding bit is "1".
Port 1 is only available when the external data bus is in 8-bit mode. Access is prohibited in 16-bit mode.
Ports 2 and 3 are only available when the address/data bus is in multiplex mode. Access is prohibited in non-multiplex mode.
Port 6 is an open drain port. Port 6 pins can only be used as ports when the analog input enable register is "0".

(1) Register Configuration

Port data register

bit	15	14	13	12	11	10	9	8	
Address: PDR1 000001H : PDR3 000003H : PDR5 000005H : PDR7 000007H : PDR9 000009H	PD×7	PD×6	PD×5	PD×4	PD×3	PD×2	PD×1	PD×0	PDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Port data register

bit	7	6	5	4	3	2	1	0	
Address: PDR2 000002H : PDR4 000004H : PDR6 000006H : PDR8 000008H : PDRA 00000AH	PD×7	PD×6	PD×5	PD×4	PD×3	PD×2	PD×1	PD×0	PDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Notes: No register bits are provided for bit 6 to 7 of port 5.
No register bit is provided for bit 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bits are provided for bits 6 to 7 of port 9.
No register bit is provided for bit 0 of port A.

Port direction register

bit	15	14	13	12	11	10	9	8	
Address: DDR1 000011H : DDR3 000013H : DDR5 000015H : DDR7 000017H : DDR9 000019H	DD×7	DD×6	DD×5	DD×4	DD×3	DD×2	DD×1	DD×0	DDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Port direction register

bit	7	6	5	4	3	2	1	0	
Address: DDR2 000012H : DDR4 000014H : DDR8 000018H : DDRA 00001AH	DD×7	DD×6	DD×5	DD×4	DD×3	DD×2	DD×1	DD×0	DDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Note: No register bits are provided for bit 6 to 7 of port 5.
No register bit is provided for bit 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bits are provided for bits 6 to 7 of port 9.
No register bit is provided for bit 0 of port A.
Port 6 does not have a DDR.

Analog input enable register
ADER 000016H

bit	15	14	13	12	11	10	9	8	
	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	ADER
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

(2) Register Details

- **Port Data Registers**

Port data register
Address: PDR1 000001H
: PDR3 000003H
: PDR5 000005H
: PDR7 000007H
: PDR9 000009H

bit	15	14	13	12	11	10	9	8	
	PD×7	PD×6	PD×5	PD×4	PD×3	PD×2	PD×1	PD×0	PDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Port data register
Address: PDR2 000002H
: PDR4 000004H
: PDR6 000006H
: PDR8 000008H
: PDRA 00000AH

bit	7	6	5	4	3	2	1	0	
	PD×7	PD×6	PD×5	PD×4	PD×3	PD×2	PD×1	PD×0	PDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Note: No register bits are provided for bit 6 to 7 of port 5.
No register bit is provided for bit 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bits are provided for bits 6 to 7 of port 9.
No register bit is provided for bit 0 of port A.
Port 1 is only available when the external data bus is in 8-bit mode. Access is prohibited in 16-bit mode.
Ports 2, 3 are only available in multiplex mode. Access is prohibited in non-multiplex mode.

- **Port Direction Registers**

Port direction register bit 15 14 13 12 11 10 9 8
Address : DDR1 000011H
: DDR3 000013H
: DDR5 000015H
: DDR7 000017H
: DDR9 000019H

	DD×7	DD×6	DD×5	DD×4	DD×3	DD×2	DD×1	DD×0	DDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Port direction register bit 7 6 5 4 3 2 1 0
Address : DDR2 000012H
: DDR4 000014H
: DDR8 000018H
: DDRA 00001AH

	DD×7	DD×6	DD×5	DD×4	DD×3	DD×2	DD×1	DD×0	DDR×
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

When pins are used as ports, the register bits control the corresponding pins as follows.
0: Input mode
1: Output mode

Bits are set to “0” by a reset.

Note: No register bits are provided for bit 6 to 7 of port 5.
No register bit is provided for bit 7 of port 7.
No register bit is provided for bit 7 of port 8.
No register bit is provided for bit 0 of port A.
No register bits are provided for bits 6 to 7 of port 9.
Port 6 does not have a DDR.
Port 1 is only available when the external data bus is in 8-bit mode. Access is prohibited in 16-bit mode.
Ports 2 and 3 are only available in multiplex mode. Access is prohibited in non-multiplex mode.

- **Analog Input Enable Register**

Analog input enable register bit 15 14 13 12 11 10 9 8
ADER 000016H

	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	ADER
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

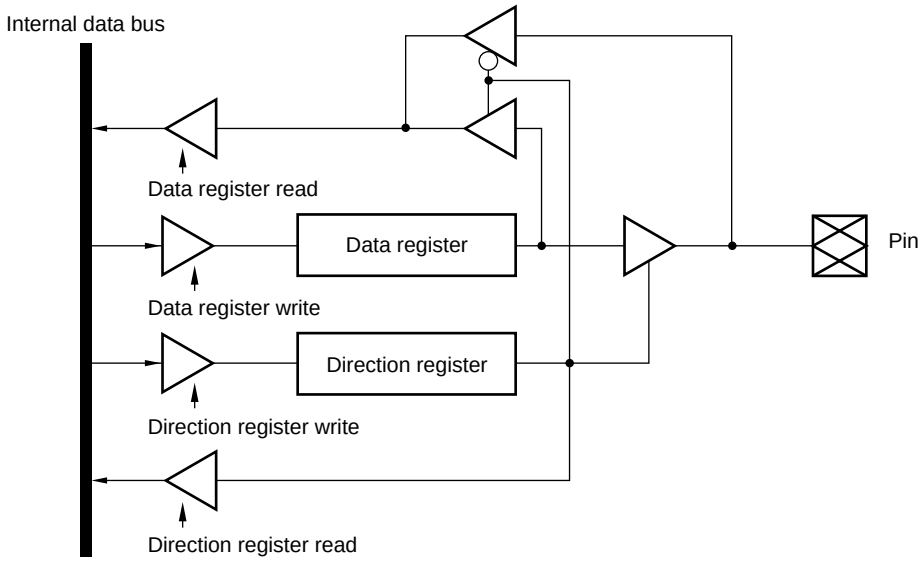
Controls each pin of port 6 as follows.
0: Port input mode
1: Analog input mode

Bits are set to “1” by a reset.

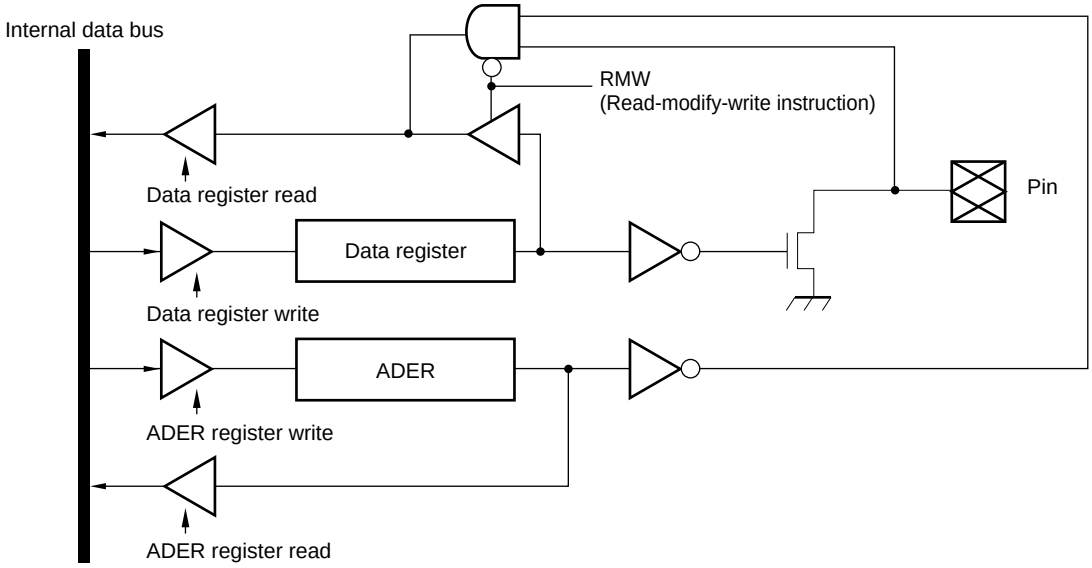
Note: Inputting an intermediate level signal in port input mode causes an input leak current to flow. Therefore, set to analog input mode when applying an analog input.

(3) Block Diagrams

- **I/O Port**



- **Open Drain Port (Also used as Analog Inputs)**



(4) Port Pin Allocation

Ports 1, 2, 3, 4, and 5 on the MB90610A series share pins with the external bus. The pin functions are determined by the bus mode and register settings.

Pin	Function							
	Non-multiplex mode				Multiplex mode			
	External address control				External address control			
	Enable (address)		Disable (port)		Enable (address)		Disable (port)	
	External bus width		External bus width		External bus width		External bus width	
	8-bit	16-bit	8-bit	16-bit	8-bit	16-bit	8-bit	16-bit
D07 to D00 AD07 to AD00	D07 to D00				AD07 to AD00			
P17 to P10/ D15 to D08/ AD15 to AD08	Port	D15 to D08	Port	D15 to D08	A15 to A08	AD15 to AD08	A15 to A08	AD15 to AD08
P27 to P20/ A07 to A00	A07 to A00		A07 to A00		Port			
P37 to P30/ A15 to A08	A15 to A08		A15 to A08					
P47 to P40/ A23 to A16	A23 to A16		Port		A23 to A16		Port	
P57/ALE	ALE				ALE			
$\overline{RD}$	$\overline{RD}$				$\overline{RD}$			
P55/$\overline{WRL}$	$\overline{WRL}$				$\overline{WRL}$			
P54/$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$	Port	$\overline{WRH}$
P53/HRQ	HRQ				HRQ			
P52/$\overline{HAK}$	$\overline{HAK}$				$\overline{HAK}$			
P51/RDY	RDY				RDY			
P50/CLK	CLK				CLK			

Note: The upper address, $\overline{WRL}$, $\overline{WRH}$, $\overline{HAK}$, HRQ, RDY, and CLK can be set for use as ports by function selection.

2. UART 0/1/2 (SCI)

UART 0/1/2 are serial I/O ports that can be used for CLK asynchronous (start-stop synchronization) or CLK synchronous (I/O expansion serial) data transfer. The ports have the following features.

- Full duplex, double buffered
- Supports CLK asynchronous (start-stop synchronization) and CLK synchronous (I/O expansion serial) data transfer
- Multi-processor mode support
- Built-in dedicated baud rate generator
  CLK asynchronous: 62500/31250/19230/9615/4808/2404/1202 bps
  CLK synchronous: 2 M/1 M/500 K/250 K bps
- Supports flexible baud rate setting using an external clock
- Error detect function (parity, framing, and overrun)
- NRZ type transmission signal
- Intelligent I/O service support

(1) Register Configuration

Serial mode register
Address: channel 0 000020_H
: channel 1 000024_H
: channel 2 000044_H

bit	7	6	5	4	3	2	1	0	
	MD1	MD0	CS2	CS1	CS0	–	SCKE	SOE	SMR
Read/write →	(R/W)	(R/W)	(W)	(W)	(W)	(–)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(–)	(0)	(0)	

Serial control register
Address: channel 0 000021_H
: channel 1 000025_H
: channel 2 000045_H

bit	15	14	13	12	11	10	9	8	
	PEN	P	SBL	CL	A/D	REC	RXE	TXE	SCR
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	

Input data register/
Output data register
Address: channel 0 000022_H
: channel 1 000026_H
: channel 2 000046_H

bit	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	SIDR (read) SODR (write)
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

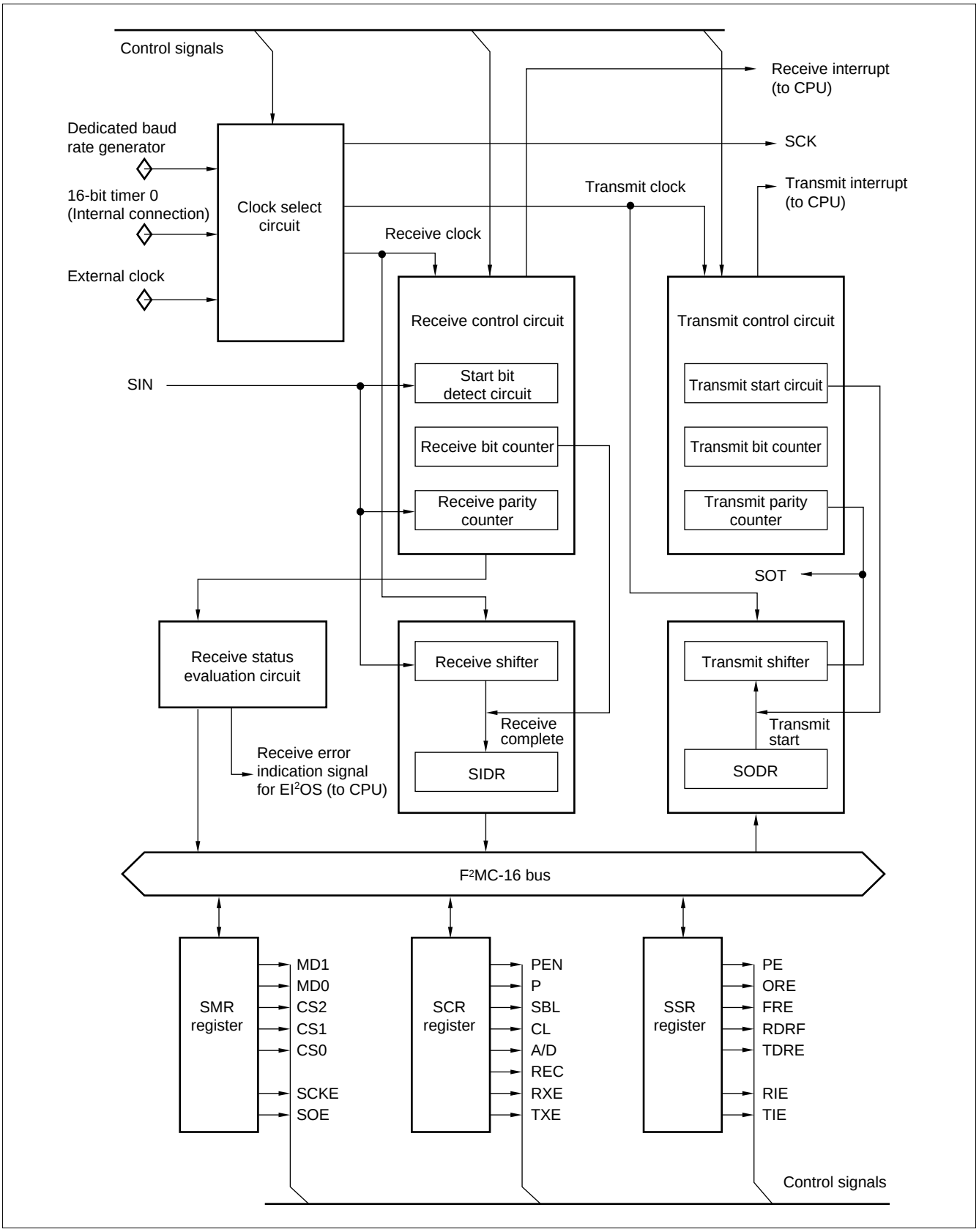
Serial status register
Address: channel 0 000023_H
: channel 1 000027_H
: channel 2 000047_H

bit	15	14	13	12	11	10	9	8	
	PE	ORE	FRE	RDRF	TDRE	–	RIE	TIE	SSR
Read/write →	(R)	(R)	(R)	(R)	(R)	(–)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(1)	(–)	(0)	(0)	

Machine clock division control register
Address: channel 0 000051_H
: channel 1 000053_H
: channel 2 000055_H

bit	15	14	13	12	11	10	9	8	
	–	–	–	–	DIV3	DIV1	DIV1	DIV0	CDCR
Read/write →	(–)	(–)	(–)	(–)	(W)	(W)	(W)	(W)	
Initial value →	(–)	(–)	(–)	(–)	(1)	(1)	(1)	(1)	

(2) Block Diagram



3. 10-bit 8-input A/D Converter (With 8-bit Resolution Mode)

The 10-bit 8-input A/D converter converts analog input voltages to digital values. The A/D converter has the following features.

- Conversion time: Minimum of 6.13 µs per channel (98 machine cycles/16 MHz machine clock. This includes the sample and hold time)
- Sample and hold time: Minimum of 3.75 µs per channel (60 machine cycles/16 MHz machine clock)
- Uses RC-type successive approximation conversion with a sample and hold circuit.
- 10-bit or 8-bit resolution
- Eight program-selectable analog input channels

  Single conversion mode : Selectively convert a one channel.

  Scan conversion mode : Continuously convert multiple channels. Maximum of 8 program-selectable channels.

  Continuous conversion mode : Repeatedly convert specified channels.

  Stop conversion mode : Convert one channel then halt until the next activation. (Enables synchronization of the conversion start timing.)
- An A/D conversion completion interrupt request to the CPU can be generated on the completion of A/D conversion. This interrupt can activate I²OS to transfer the result of A/D conversion to memory and is suitable for continuous operation.
- Activation by software, external trigger (falling edge), or timer (rising edge) can be selected.

(1) Register Configuration

A/D control status register (upper)
Address: 00002D$_H$

bit	15	14	13	12	11	10	9	8	
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	ADCS1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(–)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

A/D control status register (lower)
Address: 00002C$_H$

bit	7	6	5	4	3	2	1	0	
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	ADCS0
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

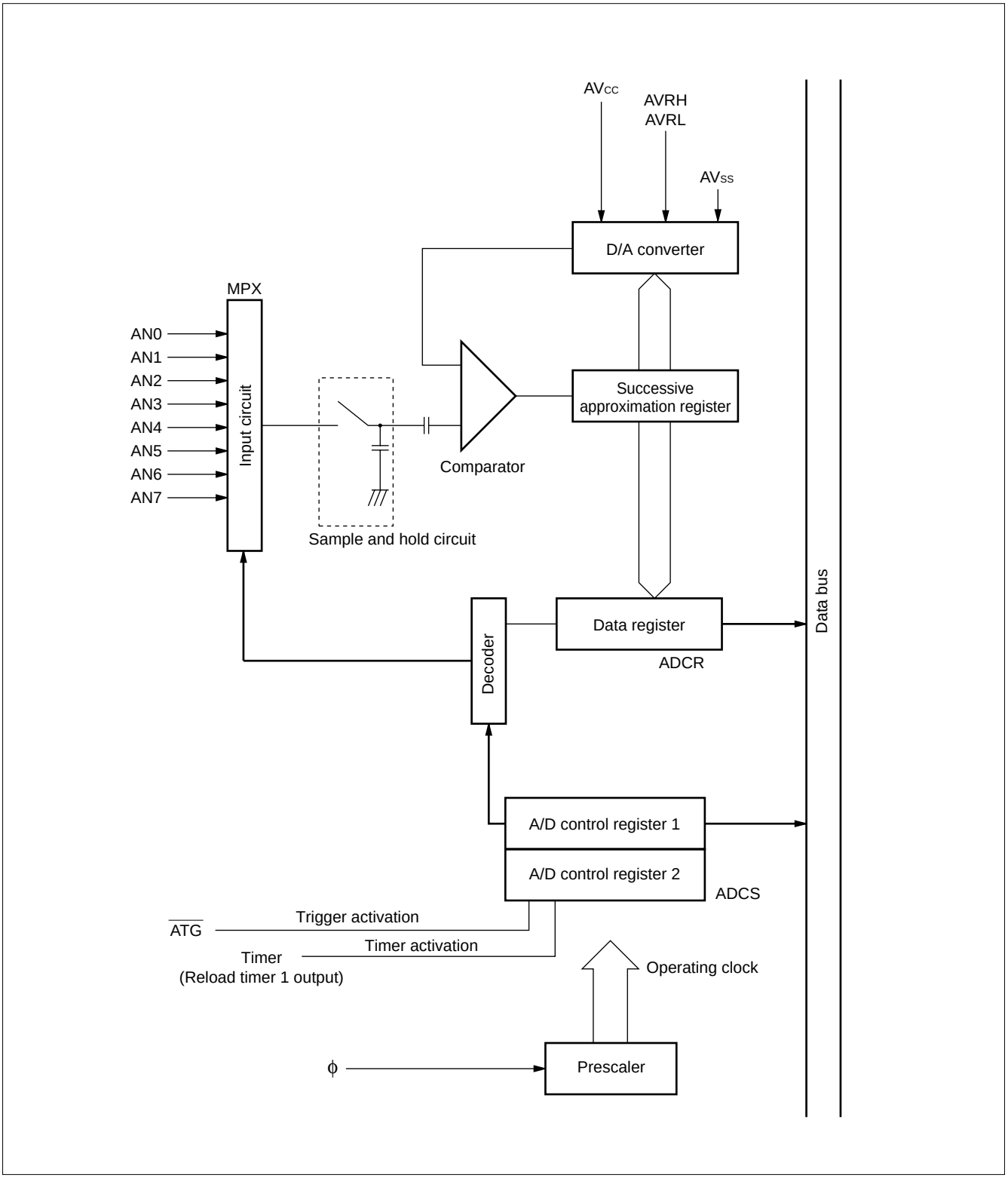
A/D data register (upper)
Address: 00002E$_H$

bit	15	14	13	12	11	10	9	8	
	S10	–	–	–	–	–	D9	D8	ADCR1
Read/write →	(R/W)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(X)	(X)	

A/D data register (lower)
Address: 00002F$_H$

bit	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	ADCR0
Read/write →	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



4. 8/16-bit PPG

This block contains the 8-bit reload timer module. The block performs PPG output in which the pulse output is controlled by the operation of the timer.
The hardware consists of two 8-bit down-counters, four 8-bit reload registers, one 16-bit control register, two external pulse output pins, and two interrupt outputs. The PPG has the following functions.

- 8-bit PPG output in 2-channel independent operation mode: Two independent PPG output channels are available.
- 16-bit PPG output operation mode : One 16-bit PPG output channel is available.
- 8+8-bit PPG output operation mode : Variable-period 8-bit PPG output operation is available by using the output of channel 0 as the clock input to channel 1.
- PPG output operation: Outputs pulse waveforms with variable period and duty ratio.
  Can be used as a D/A converter in conjunction with an external circuit.

(1) Register Configuration

PPG0 operation mode control register
Address: channel 0 000030H

bit	7	6	5	4	3	2	1	0	
	PEN0	—	POE0	PIE0	PUF0	PCM1	PCM0	Reserved	PPGC0
Read/write →	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	

PPG1 operation mode control register
Address: channel 1 000031H

bit	15	14	13	12	11	10	9	8	
	PEN1	PCS1	POE1	PIE1	PUF1	MD1	MD0	Reserved	PPGC1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	

Reload register H
Address: channel 0 000035H
: channel 1 000037H

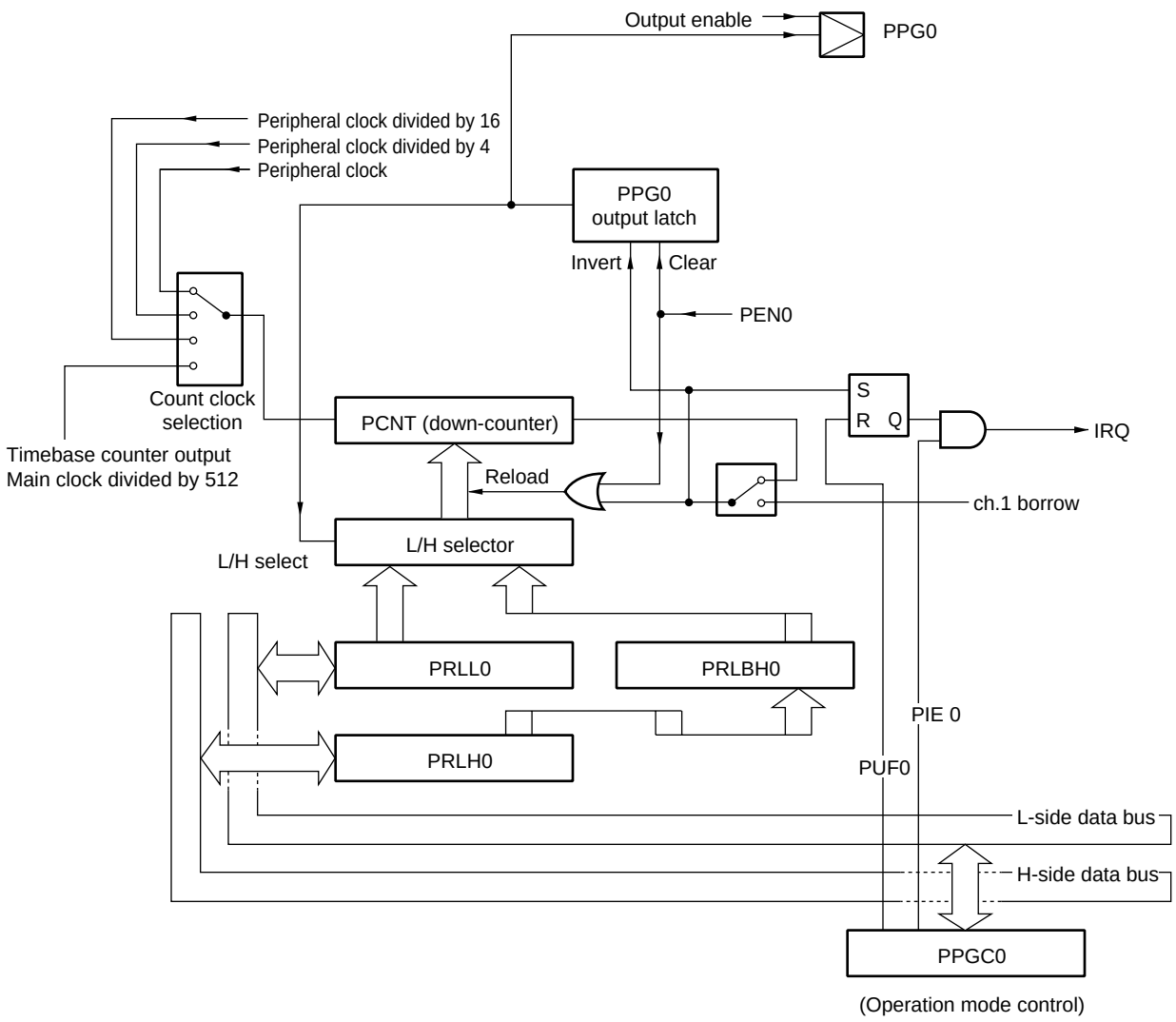
bit	15	14	13	12	11	10	9	8	
									PRLH0, 1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Reload register L
Address: channel 0 000034H
: channel 1 000036H

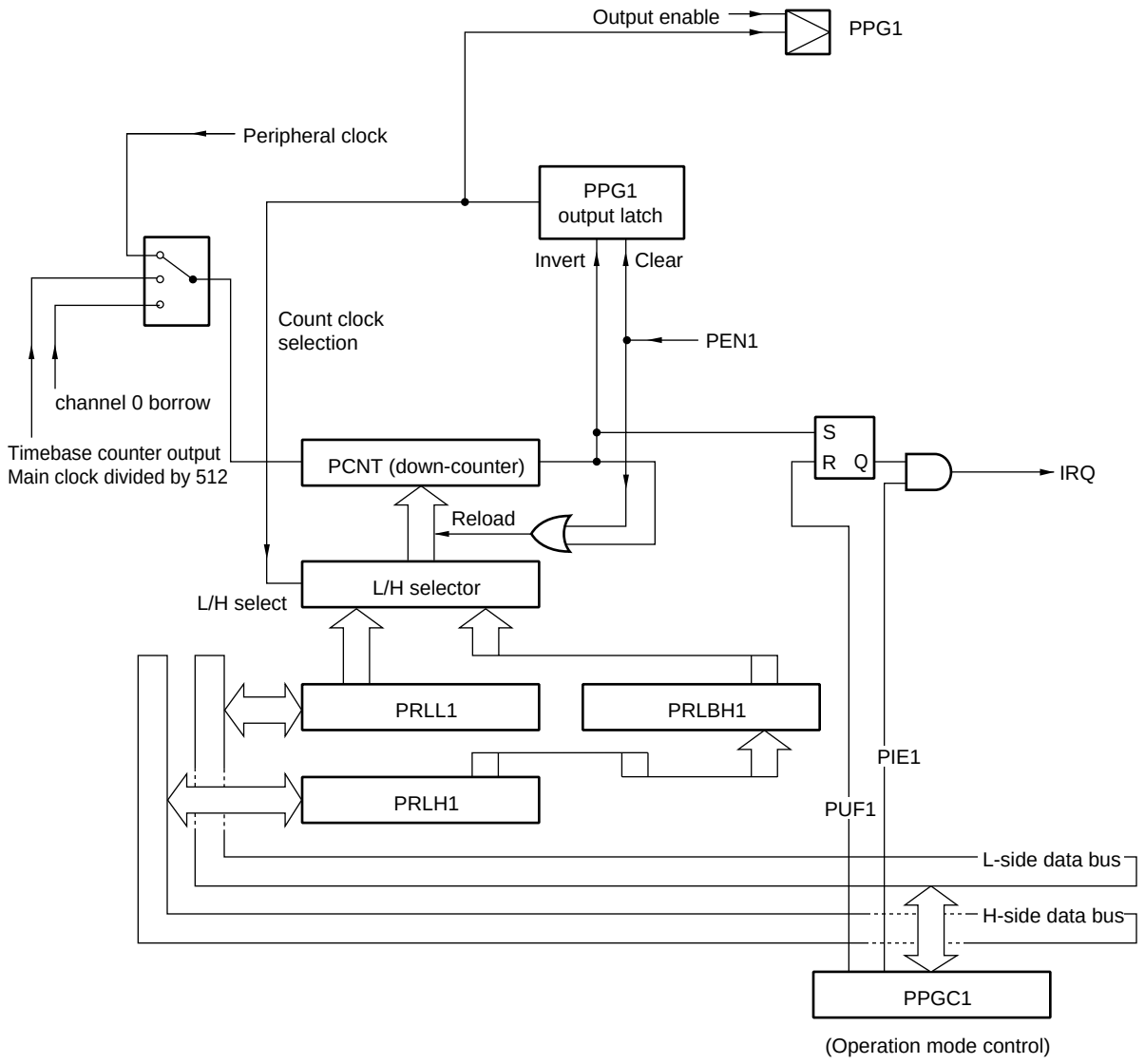
bit	7	6	5	4	3	2	1	0	
									PRLL0, 1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram

- **8/16-bit PPG (channel 0)**



- **8/16-bit PPG (channel 1)**



5. 16-bit Reload Timer (with Event Count Function)

The 16-bit reload timers consists of a 16-bit down-counter, a 16-bit reload register, one input (TIN) and one output (TOT) pin, and a control register. The input clock can be selected from one external clock and three types of internal clock. The output pin (TOT) outputs a toggle waveform in reload mode and a rectangular waveform during counting in one-shot mode. The input pin (TIN) functions as the event input in event count mode and as the trigger input or gate input in internal clock mode.
This product has two internal 16-bit reload timer channels.

(1) Register Configuration

Timer control status register (upper)
Address: channel 0 000039H
: channel 1 00003DH

bit	15	14	13	12	11	10	9	8
	—	—	—	—	CSL1	CSL2	MOD2	MOD1
Read/write →	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)

Timer control status register (lower)
Address: channel 0 000038H
: channel 1 00003CH

bit	7	6	5	4	3	2	1	0	
	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	TMCSR
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

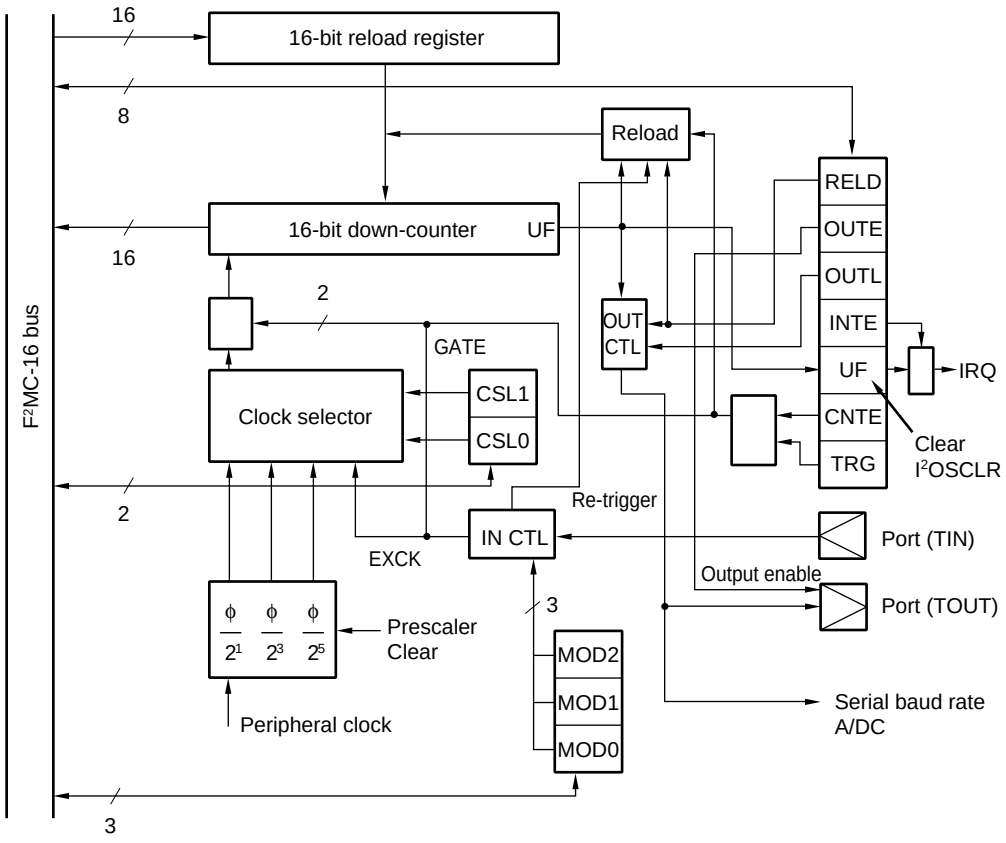
16-bit timer register (upper)/ 16-bit reload register (upper)
Address: channel 0 00003BH
: channel 1 00003FH

bit	15	14	13	12	11	10	9	8
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

16-bit timer register (lower)/ 16-bit reload register (lower)
Address: channel 0 00003AH
: channel 1 00003EH

bit	7	6	5	4	3	2	1	0	
									TMR/ TMRLR
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



6. Chip Select Function

This module generates chip select signals to simplify connection of memory or I/O devices. The module has 8 chip select output pins. The hardware outputs the chip select signals from the pins when it detects access of an address in the areas specified in the pin registers.

(1) Register Configuration

Address: 000049H
: 00004BH
: 00004DH
: 00004FH

bit	15	14	13	12	11	10	9	8
	—	—	—	—	ACTL	OPEL	CSA1	CSA0

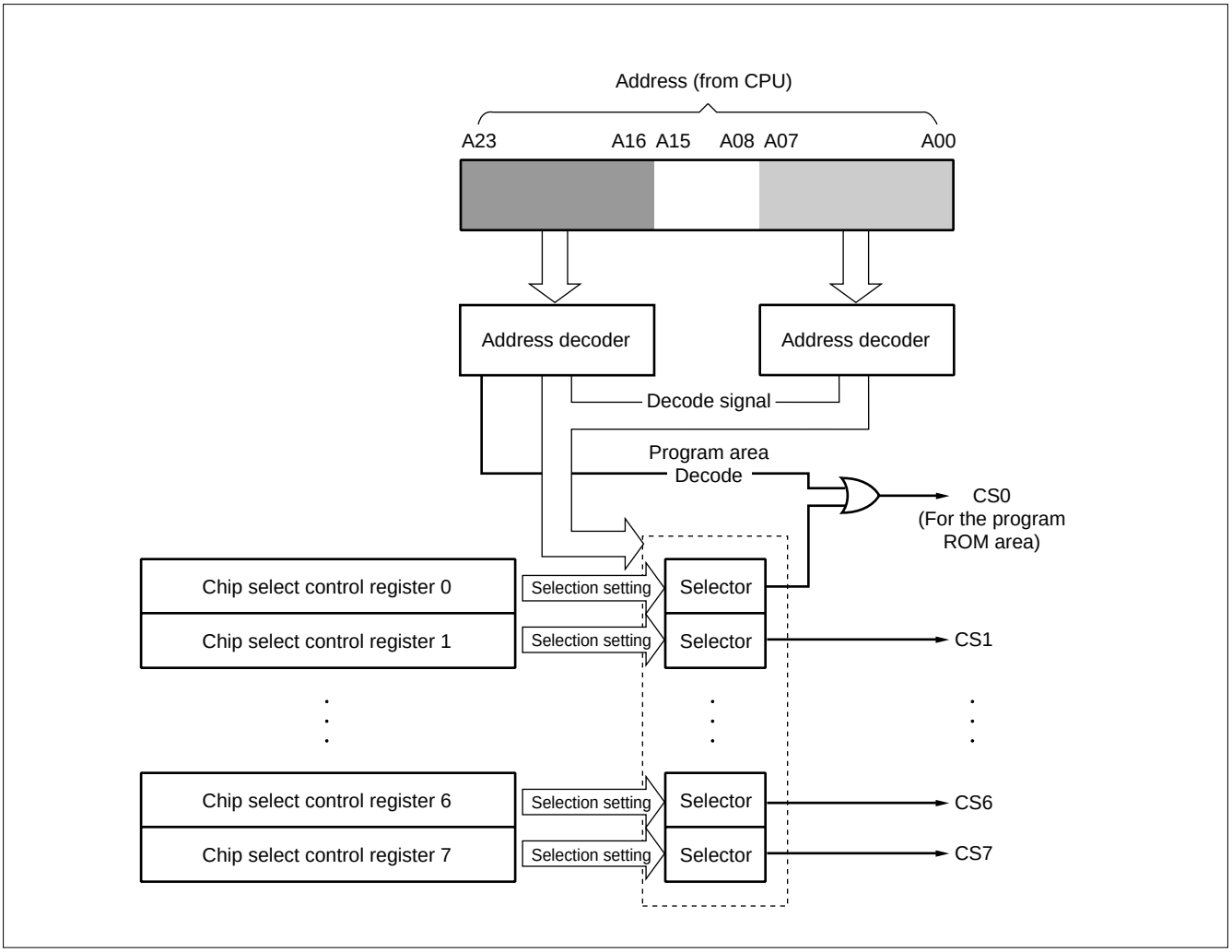
Chip select control register (odd numbers: CSCR1/3/5/7)

Address: 000048H
: 00004AH
: 00004CH
: 00004EH

bit	7	6	5	4	3	2	1	0
	—	—	—	—	ACTL	OPEL	CSA1	CSA0

Chip select control register (even numbers: CSCR0/2/4/6)

(2) Block Diagram



7. DTP/External Interrupts

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16L CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16L CPU to activate the extended intelligent I/O service or interrupt processing. Two request levels ("H" and "L") are provided for extended intelligent I/O service. For external interrupt requests, generation of interrupts on a rising or falling edge as well as on "H", "L" levels can be selected, giving a total of four types.

(1) Register Configuration

Interrupt/DTP enable register
Address: 000028H — ENIR

bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Interrupt/DTP register
Address: 000029H — EIRR

bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

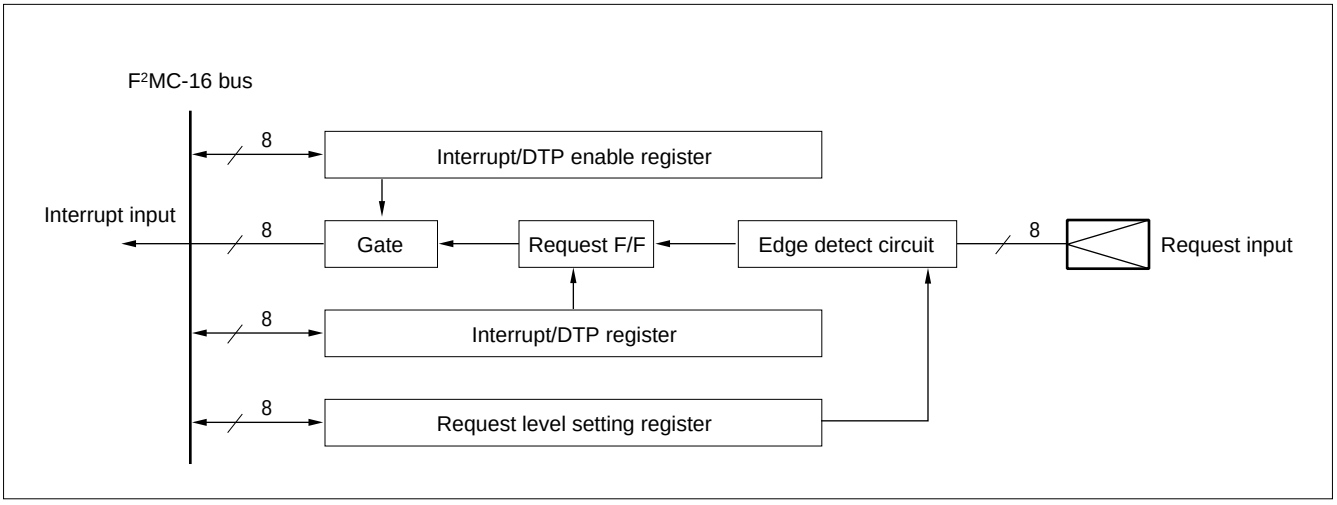
Request level setting register (upper)
Address: 00002BH

bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Request level setting register (lower)
Address: 00002AH — ELVR

bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

(2) Block Diagram



8. Delayed Interrupt Generation Module

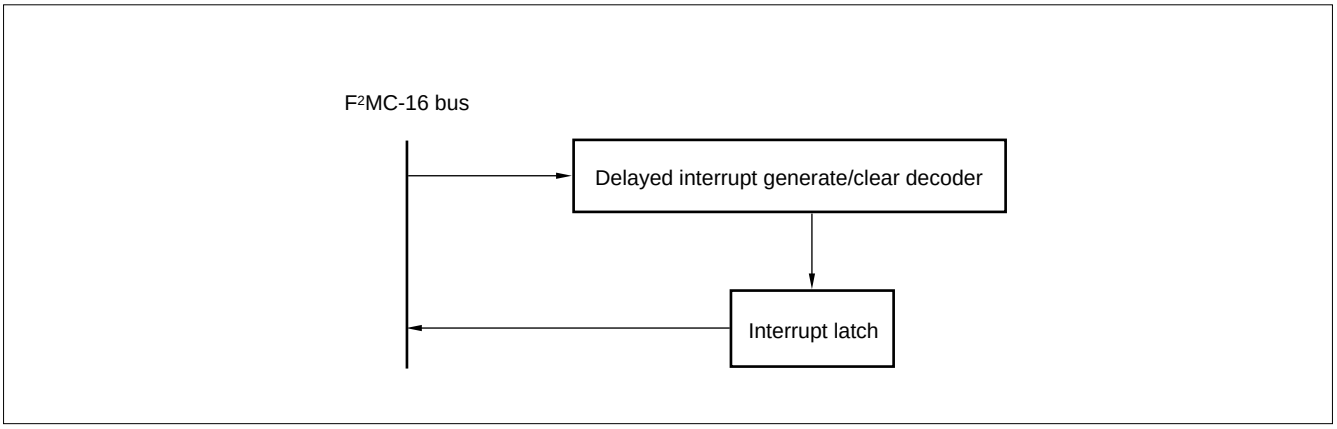
The delayed interrupt generation module is used to generate the task switching interrupt. Interrupt requests to the F²MC-16L CPU can be generated and cleared by software using this module.

(1) Register Configuration

Delayed interrupt generate/ clear decoder
Address: 00009F$_H$

bit	15	14	13	12	11	10	9	8	
	—	—	—	—	—	—	—	R0	DIRR
Read/write →	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value →	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



9. Watchdog Timer and Timebase Timer Functions

The watchdog timer consists of a 2-bit watchdog counter, a control register, and a watchdog reset controller. The watchdog counter uses the carry-up signal from the 18-bit timebase timer as its clock source. In addition to the 18-bit timer, the timebase timer contains an interval interrupt control circuit. The timebase timer uses the main clock, regardless of the value of the MCS bit in the CKSCR register.

(1) Register Configuration

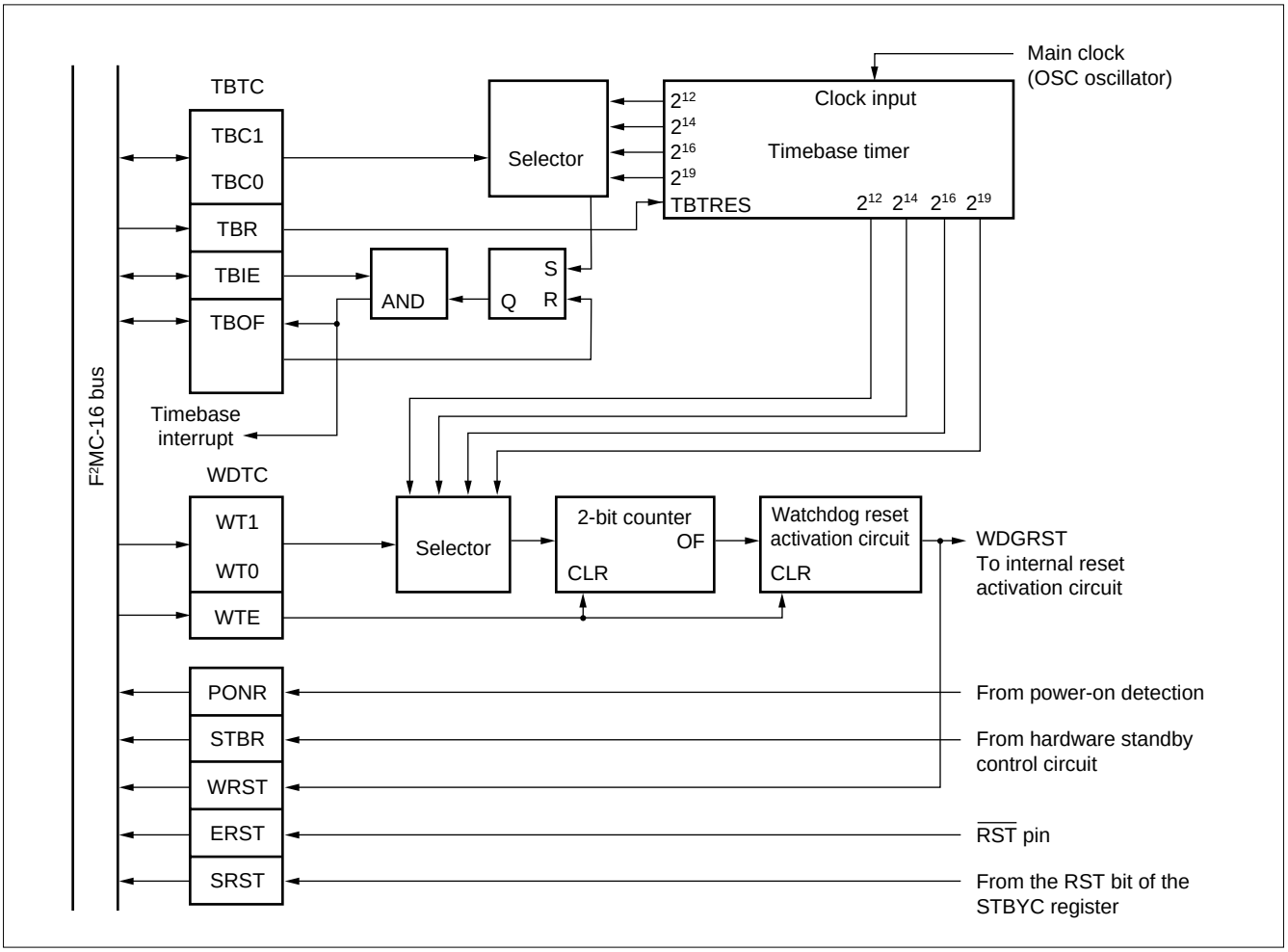
Watchdog timer control register
Address: 0000A8H

bit	7	6	5	4	3	2	1	0	
	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	WDTC
Read/write →	(R)	(R)	(R)	(R)	(R)	(W)	(W)	(W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(1)	(1)	(1)	

Timebase timer control register
Address: 0000A9H

bit	15	14	13	12	11	10	9	8	
	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	TBTC
Read/write →	(—)	(—)	(—)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
Initial value →	(1)	(—)	(—)	(0)	(0)	(1)	(0)	(0)	

(2) Block Diagram



10. Low Power Control Circuits (CPU Intermittent Operation Function, Oscillation Stabilization Delay Time, and Clock Multiplier Function)

The following operation modes are available: PLL clock mode, PLL sleep mode, timer mode, main clock mode, main sleep mode, stop mode, and hardware standby mode. Operation modes other than PLL clock mode are classified as low power consumption modes.
In main clock mode and main sleep mode, the device operates on the main clock only (OSC oscillator clock). The PLL clock (VCO oscillator clock) is stopped in these modes and the main clock divided by 2 is used as the operating clock.
In PLL sleep mode and main sleep mode, the CPU's operating clock only is stopped and other elements continue to operate.
In timer mode, only the timebase timer operates.
Stop mode and hardware standby mode stop the oscillator. These modes maintain existing data with minimum power consumption.
The CPU intermittent operation function provides an intermittent clock to the CPU when register, internal memory, internal resource, or external bus access is performed. This function reduces power consumption by lowering the CPU execution speed while still providing a high-speed clock to internal resources.
The PLL clock multiplier ratio can be set to 1, 2, 3, 4 by the CS1, 0 bits.
The WS1, 0 bits set the delay time to wait for the main clock oscillation to stabilize when recovering from stop mode or hardware standby mode.

(1) Register Configuration

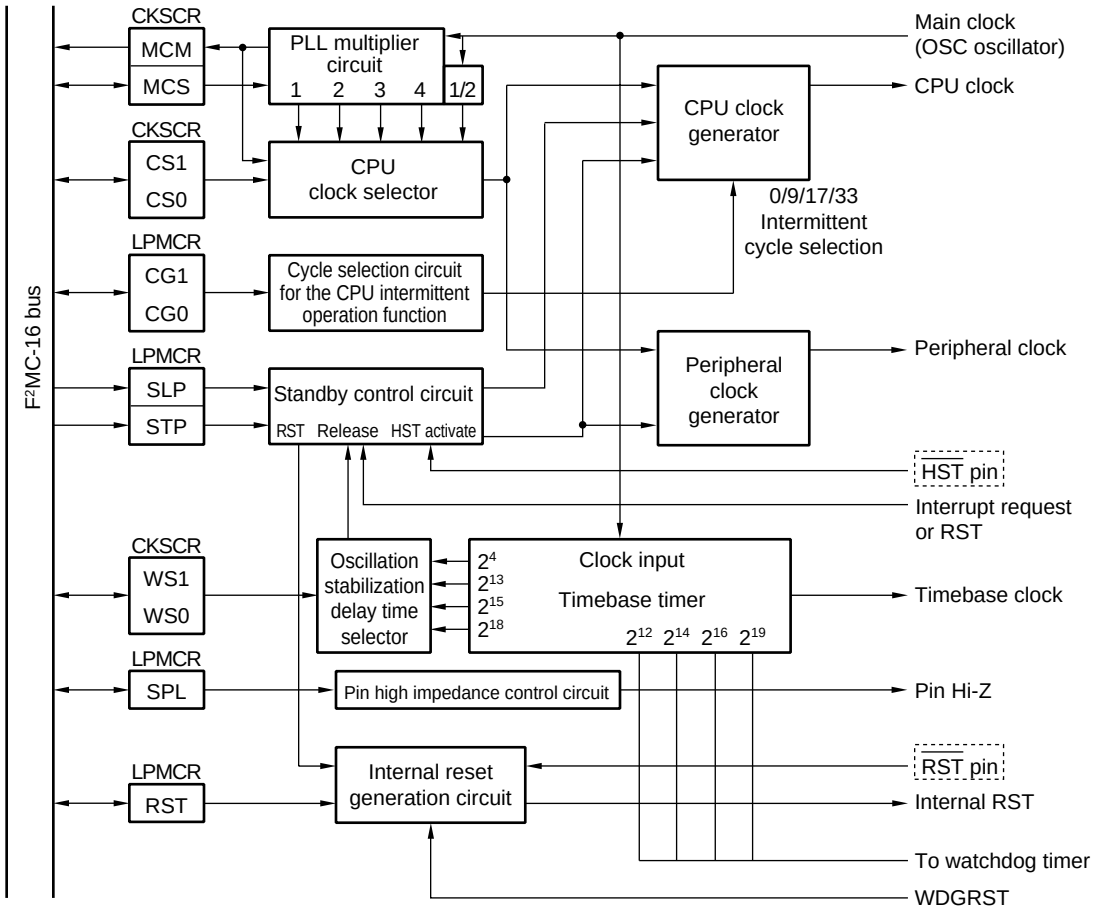
Low power consumption mode control register
Address: $0000A0_H$

bit	7	6	5	4	3	2	1	0	
	STP	SLP	SPL	RST	Reserved	CG1	CG0	Reserved	LPMCR
Read/write →	(W)	(W)	(R/W)	(W)	(—)	(R/W)	(R/W)	(—)	
Initial value →	(0)	(0)	(0)	(1)	(1)	(0)	(0)	(0)	

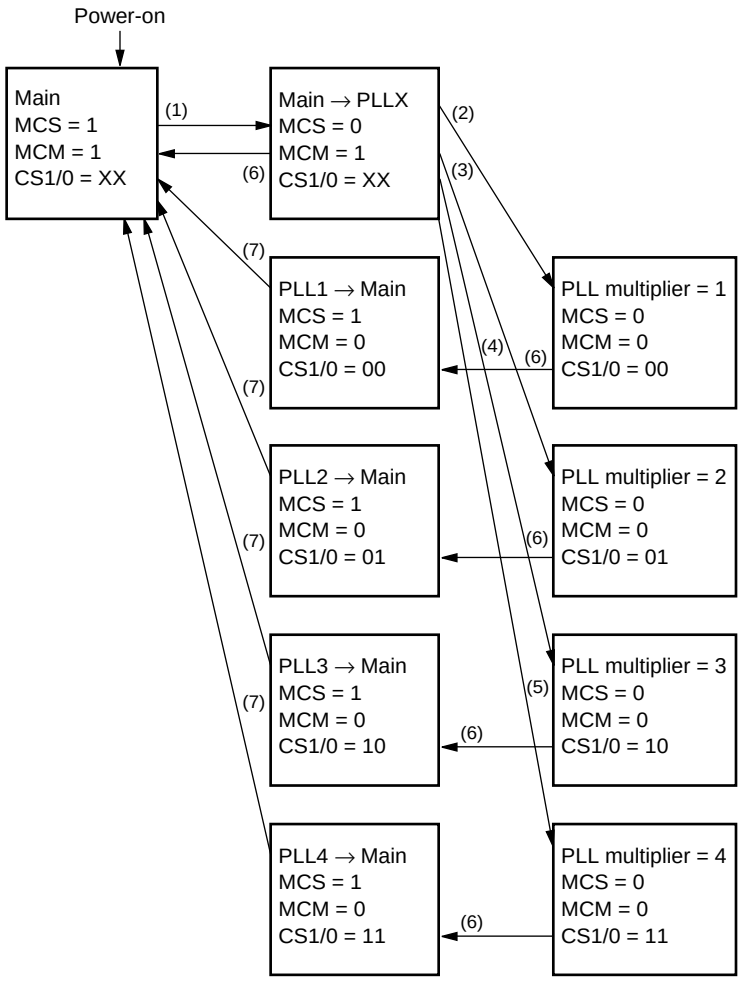
Clock select register
Address: $0000A1_H$

bit	15	14	13	12	11	10	9	8	
	Reserved	MCM	WS1	WS0	Reserved	MCS	CS1	CS0	CKSCR
Read/write →	(—)	(R)	(R/W)	(R/W)	(—)	(R/W)	(R/W)	(R/W)	
Initial value →	(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	

(2) Block Diagram



- **State Transition Diagram for Clock Selection**



(1) MCS bit cleared
(2) PLL clock oscillation stabilization delay complete and CS1/0 = “00”
(3) PLL clock oscillation stabilization delay complete and CS1/0 = “01”
(4) PLL clock oscillation stabilization delay complete and CS1/0 = “10”
(5) PLL clock oscillation stabilization delay complete and CS1/0 = “11”
(6) MCS bit set (including a hardware standby or watchdog reset)
(7) PLL clock and main clock synchronized timing

11. Interrupt Controller

The interrupt control registers are located in the interrupt controller. An interrupt control register is provided for each I/O with an interrupt function. The registers have the following three functions.

- Set the interrupt level of the corresponding peripheral.
- Select whether to treat interrupts from the corresponding peripheral as standard interrupts or activate the extended intelligent I/O service.
- Select the extended intelligent I/O service channel.

(1) Register Configuration

Interrupt control register

Address : ICR01 0000B1H
: ICR03 0000B3H
: ICR05 0000B5H
: ICR07 0000B7H
: ICR09 0000B9H
: ICR11 0000BBH
: ICR13 0000BDH
: ICR15 0000BFH

bit	15	14	13	12	11	10	9	8
	ICS3	ICS2	ICS1 or S1	ICS0 or S0	ISE	IL2	IL1	IL0
Read/write →	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)

ICRxx

Interrupt control register

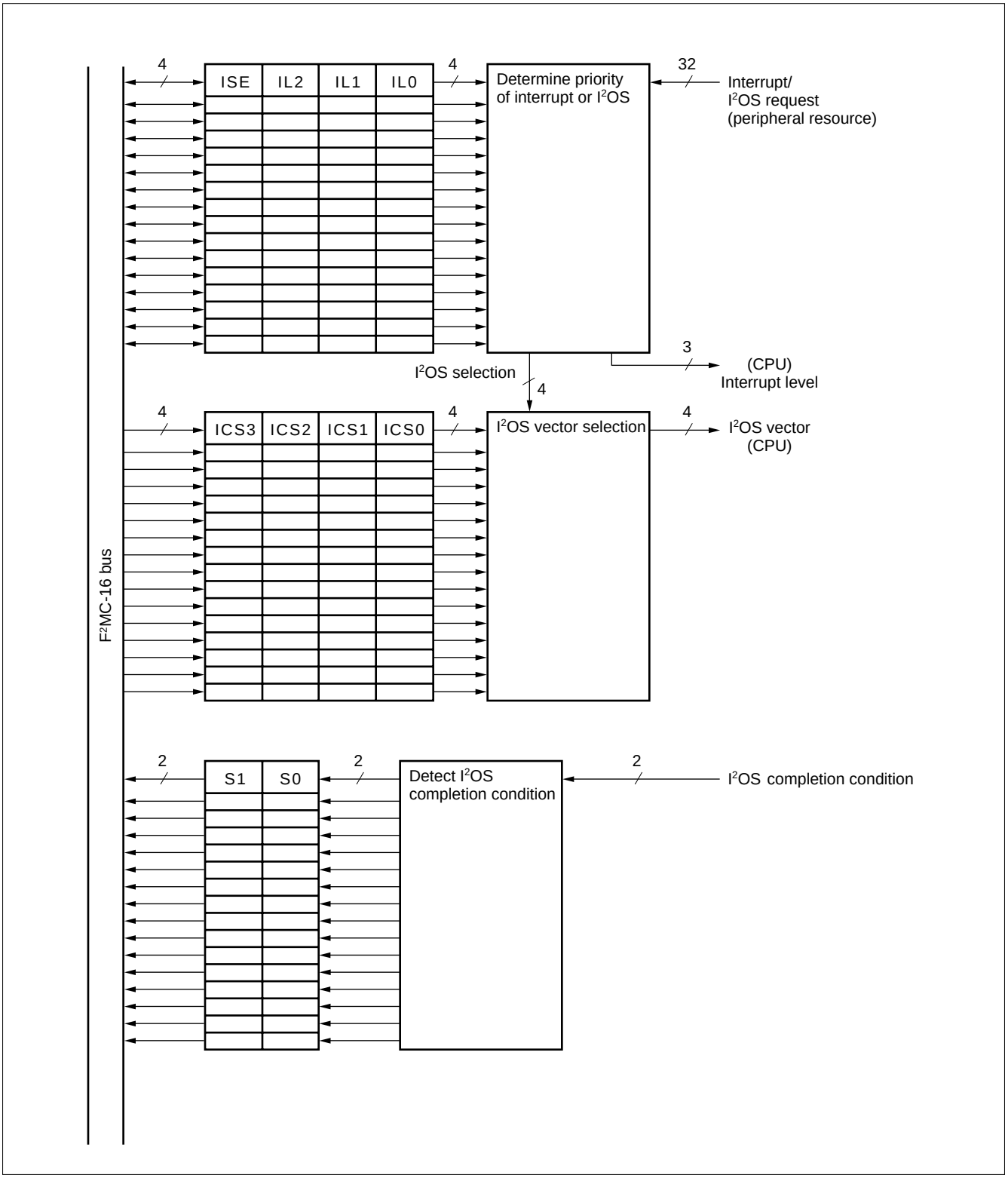
Address : ICR00 0000B0H
: ICR02 0000B2H
: ICR04 0000B4H
: ICR06 0000B6H
: ICR08 0000B8H
: ICR10 0000BAH
: ICR12 0000BCH
: ICR14 0000BEH

bit	7	6	5	4	3	2	1	0
	ICS3	ICS2	ICS1 or S1	ICS0 or S0	ISE	IL2	IL1	IL0
Read/write →	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value →	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)

ICRxx

Note: Do not access these registers using read-modify-write instructions as this can cause misoperation.

(2) Block Diagram



12. External Bus Terminal Control Circuit

This circuit controls the external bus terminals intended to extend outwardly the CPU's address/data bus.

(1) Register Configuration

Register for selection of AUTO ready function
Address: 0000A5H

bit	15	14	13	12	11	10	9	8	
	IOR1	IOR0	HMR1	HMR0	—	—	LMR1	LMR0	ARSR
Read/write →	(W)	(W)	(W)	(W)	(—)	(—)	(W)	(W)	
Initial value →	(0)	(0)	(1)	(1)	(—)	(—)	(0)	(0)	

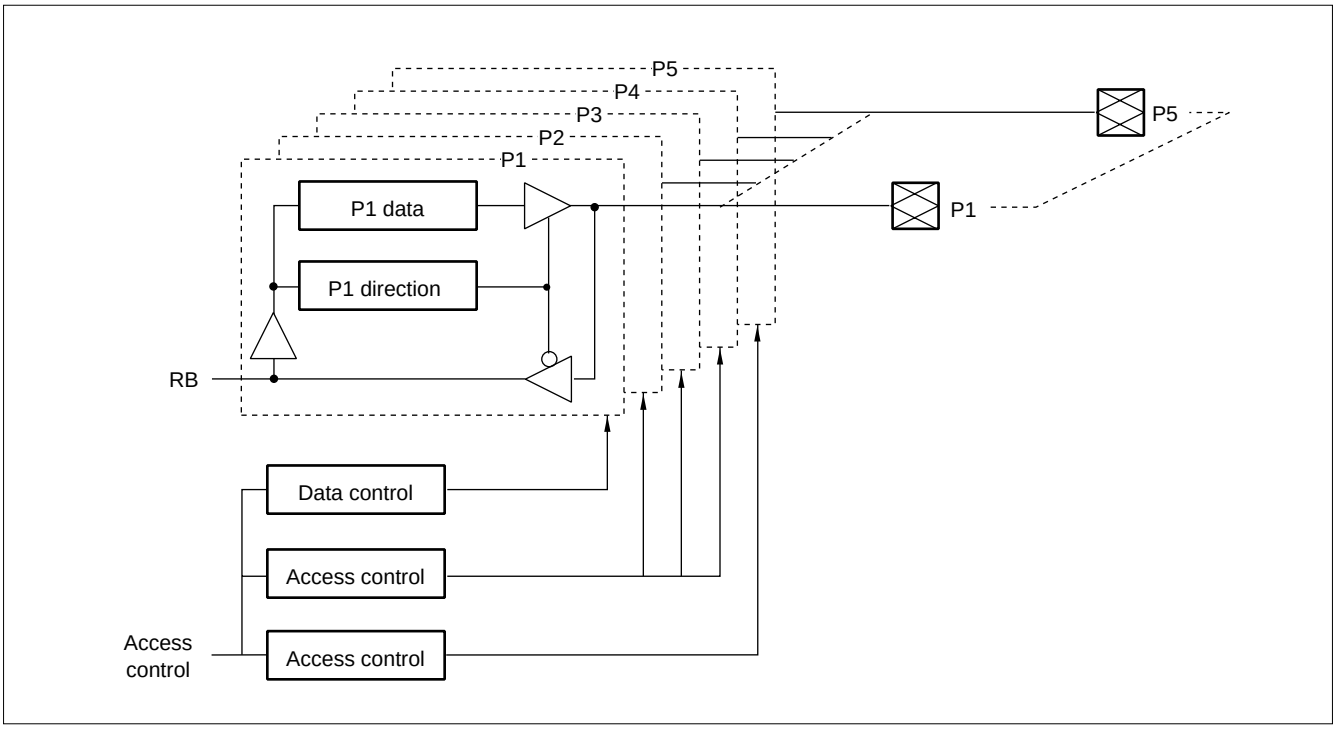
Register for control of external address output
Address: 0000A6H

bit	7	6	5	4	3	2	1	0	
	E23	E22	E21	E20	E19	E18	E17	E16	HACR
Read/write →	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Register for selection of bus control signal
Address: 0000A7H

bit	15	14	13	12	11	10	9	8	
	—	LMBS	WRE	HMBS	IOBS	HDE	RYE	CKE	ECSR
Read/write →	(—)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
Initial value →	(—)	(0)	(0)	(1/0)	(0)	(0)	(0)	(0)	

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}*1	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AVRH*1 AVRL*1	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage*2	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage*2	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current*3	I_{OL}	—	15	mA	
“L” level average output current*4	I_{OLAV}	—	4	mA	
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current*5	$\sum I_{OLAV}$	—	50	mA	
“H” level maximum output current*3	I_{OH}	—	–15	mA	
“H” level average output current*4	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	$\sum I_{OH}$	—	–100	mA	
“H” level total average output current*5	$\sum I_{OHAV}$	—	–50	mA	
Power consumption	P_d	—	+400	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: AV_{CC}, AVRH, and AVRL must not exceed V_{CC}. Similarly, it may not exceed AVRL, nor AVRH.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V.

*3: The maximum output current must not be exceeded at any individual pin.

*4: The average output current is the rating for the current from an individual pin averaged over a duration of 100 ms.

*5: The average total output current is the rating for the current from all pins averaged over a duration of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.7	5.5	V	For normal operation
		2.0	5.5	V	To maintain statuses in stop mode
Operating temperature	T_A	–40	+85	°C	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}			0.8 V_{CC}	—	V_{CC} + 0.3	V	*1
	V_{IHM}			V_{CC} – 0.3	—	V_{CC} + 0.3	V	
	V_{IHT}		V_{CC} = +5.0 V±10%	2.2	—	—	V	*2
			V_{CC} = +3.0 V±10%	0.7 V_{CC}	—	—	V	*2
"L" level input voltage	V_{IL}		—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}			V_{SS} – 0.3	—	0.2 V_{CC}	V	*1
	V_{ILM}			V_{SS} – 0.3	—	V_{SS} + 0.3	V	
	V_{ILT}		V_{CC} = +5.0 V±10%	V_{SS} – 0.3	—	0.8	V	*2
			V_{CC} = +3.0 V±10%	V_{SS} – 0.3	—	0.2 V_{CC}	V	*2
"H" level output voltage	V_{OH}	Other than P60 to P67	V_{CC} = +5.0 V±10% I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
			V_{CC} = +3.0 V±10% I_{OH} = –1.6 mA	V_{CC} – 0.3	—	—	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = +5.0 V±10% I_{OL} = –4.0 mA	—	—	0.4	V	
			V_{CC} = +3.0 V±10% I_{OL} = –2.0 mA	—	—	0.4	V	
Pull-up resistance	R_{pu}	$\overline{RST}$, P50 to P55, $\overline{RD}$, ALE, PA1 to PA7, CS0	—	30	—	100	kΩ	
Supply current	I_{CC}	V_{CC}	V_{CC} = +5.0 V±10% 16 MHz internal operation	—	50	70	mA	
	I_{CCS}			—	25	30	mA	
	I_{CC}		V_{CC} = +3.0 V±10% 8 MHz internal operation	—	10	20	mA	
	I_{CCS}			—	5	10	mA	
	I_{CCH}		V_{CC} = +5.0 V±10% T_A = 25°C	—	0.1	10	µA	
Input pin capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	10	—	pF	
Input leakage current	I_{IL}	Other than P60 to P67	V_{CC} = 5.5 V V_{SS} < V_I < V_{CC}	–10	—	10	µA	
Leakage current for open drain outputs	I_{leak}	Other than P60 to P67	—	—	0.1	10	µA	
Pull-down resistance	R_{pd}	MD2	—	40	—	200	kΩ	

*1: Hysteresis input pins: $\overline{RST}$, $\overline{HST}$, P60 to P67, P70 to P76, P80 to P86, P90 to P95, PA1 to PA7

*2: TTL input pins: AD00/D00 to AD07/D07, AD08/D08/P10 to AD15/D15/P17, HRQ/P53, RDY/P51

4. AC Characteristics

(1) Clock Timing

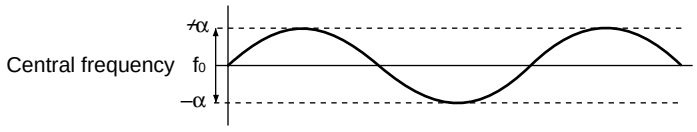
- **When V_{CC} = +5.0 V±10%**

(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	f_C	X0, X1	—	3	32	MHz	
Clock cycle time	t_C	X0, X1	—	31.25	333	ns	
Frequency variation ratio* (when locked)	Δf	—	—	—	3	%	
Input clock pulse width	P_{WH} P_{WL}	X0	—	10	—	ns	The duty ratio should be in the range 30 to 70%
Input clock rise time and fall time	t_{cr} t_{cf}	X0	—	—	5	ns	
Internal operating clock frequency	f_{CP}	—	—	1.5	16	MHz	
Internal operating clock cycle time	t_{CP}	—	—	62.5	666	ns	

* : The frequency variation ratio is the maximum variation from the specified central frequency when the multiplier PLL is locked. The value is expressed as a proportion.

$$\Delta f = \frac{| \alpha |}{f_0} \times 100\ (\%)$$

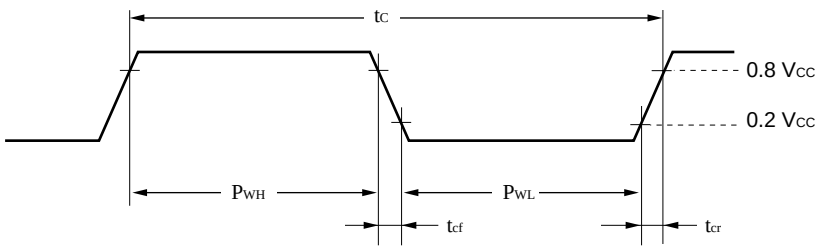


- **When V_{CC} = +2.7 V (min.)**

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

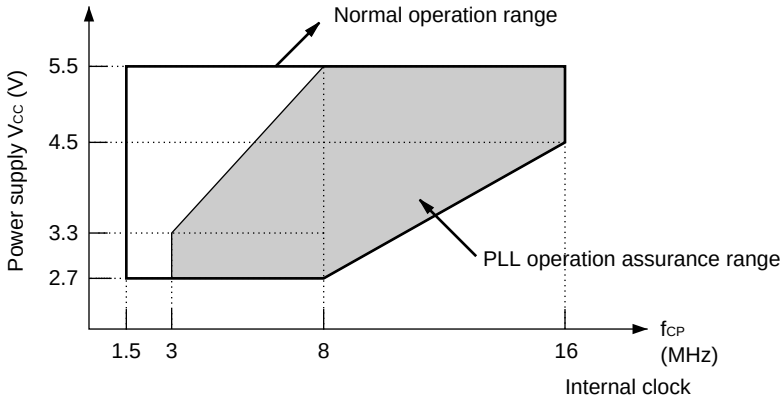
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	f_C	X0, X1	—	3	16	MHz	
Clock cycle time	t_C	X0, X1	—	62.5	333	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	ns	The duty ratio should be in the range 30 to 70%
Input clock rise time and fall time	t_{cr} t_{cf}	X0	—	—	5	ns	
Internal operating clock frequency	f_{CP}	—	—	1.5	8	MHz	
Internal operating clock cycle time	t_{CP}	—	—	125	666	ns	

- **Clock Timing**

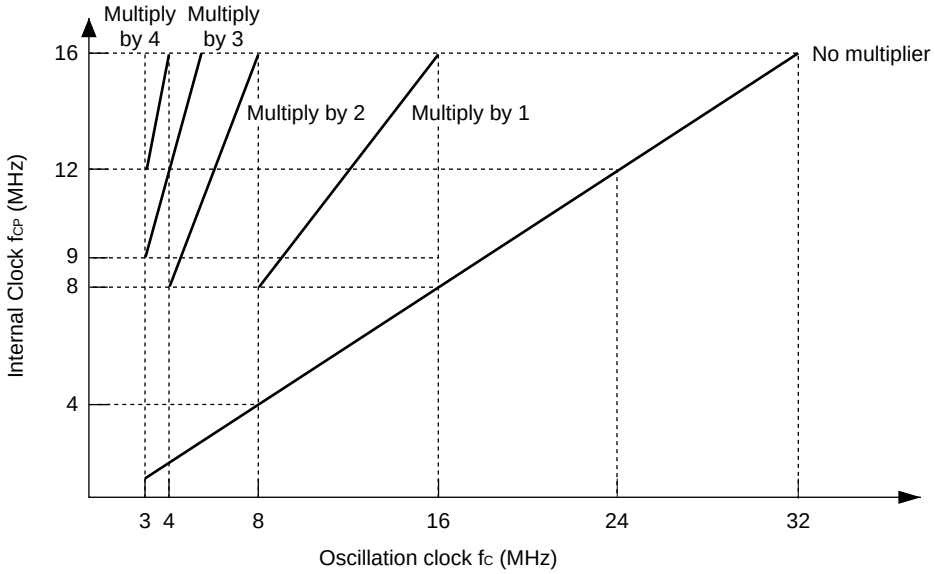


- **PLL Operation Assurance Range**

Relationship between the internal operating clock frequency and supply voltage



Relationship between the oscillation frequency and internal operating clock frequency



Note: Low voltage operation down to 2.7V is also assured for the evaluation tools.

The AC characteristics are for the following measurement reference voltages.

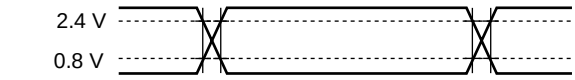
- **Input Signal Waveform**

Hysteresis input pins

Other than hysteresis/MD input pins

- **Output Signal Waveform**

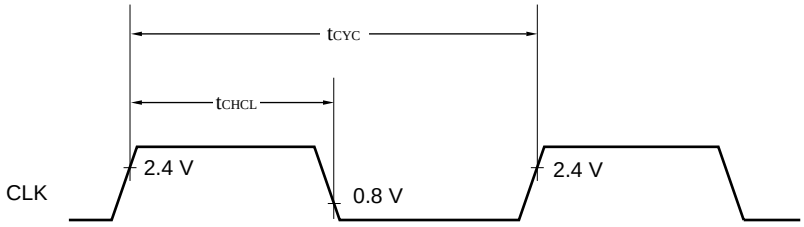
Output pins



(2) Clock Output Timing

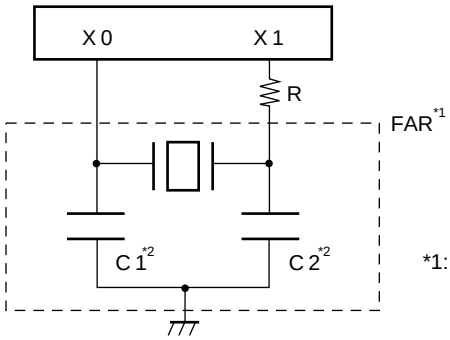
(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	V_{CC} = +5 V±10%	t_{CP}	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}			$t_{CP}/2$ – 20	$t_{CP}/2$ + 20	ns	



(3) Recommended Resonator Manufacturers

- **Sample Application of Piezoelectric Resonator (FAR Family)**

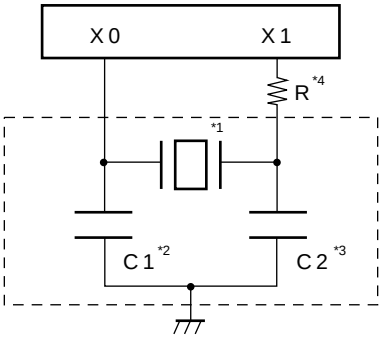


*1: Fujitsu Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristics of FAR frequency (T_A = –20°C to +60°C)	Loading capacitors*2
FAR-C4CC-02000-L20	2.00	1 KΩ	±0.5%	±0.5%	Built-in
FAR-C4CA-04000-M01	4.00	—	±0.5%	±0.5%	
FAR-C4CB-08000-M02	8.00	—	±0.5%	±0.5%	
FAR-C4CB-10000-M02	10.00	—	±0.5%	±0.5%	
FAR-C4CB-16000-M02	16.00	—	±0.5%	±0.5%	

Inquiry: FUJITSU LIMITED

- **Sample Application of Ceramic Resonator**



Resonator manufacturer*1	Resonator	Frequency (MHz)	C1 (pF)*2	C2 (pF)*3	R*4
Kyocera Corporation	KBR-2.0MS	2.00	150	150	Not required
	PBRC2.00A		150	150	Not required
	KBR-4.0MSA	4.00	33	33	680 Ω
	KBR-4.0MKS		Built-in	Built-in	680 Ω
	PBRC4.00A		33	33	680 Ω
	PBRC4.00B		Built-in	Built-in	680 Ω
	KBR-6.0MSA	6.00	33	33	Not required
	KBR-6.0MKS		Built-in	Built-in	Not required
	PBRC6.00A		33	33	Not required
	PBRC6.00B		Built-in	Built-in	Not required
	KBR-8.0M	8.00	33	33	560 Ω
	PBRC8.00A		33	33	Not required
	PBRC8.00B		Built-in	Built-in	Not required
	KBR-10.0M	10.00	33	33	330 Ω
	PBRC10.00B		Built-in	Built-in	680 Ω
	KBR-12.0M	12.00	33	33	330 Ω
	PBRC12.00B		Built-in	Built-in	680 Ω

(Continued)

(Continued)

Resonator manufacturer*1	Resonator	Frequency (MHz)	C1 (pF)*2	C2 (pF)*3	R*4
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CST2.00MG040		Built-in	Built-in	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CST4.00MGW040		Built-in	Built-in	Not required
	CSA6.00MG	6.00	30	30	Not required
	CST6.00MGW		Built-in	Built-in	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CST8.00MTW		Built-in	Built-in	Not required
	CSA10.00MTZ	10.00	30	30	Not required
	CST10.00MTW		Built-in	Built-in	Not required
	CSA12.00MTZ	12.00	30	30	Not required
	CST12.00MTW		Built-in	Built-in	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CST16.00MXW0C3		Built-in	Built-in	Not required
	CSA20.00MXZ040	20.00	10	10	Not required
	CSA24.00MXZ040	24.00	5	5	Not required
	CSA32.00MXZ040	32.00	5	5	Not required

Inquiry: Kyocera Corporation

- AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
- AVX Limited
  European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303

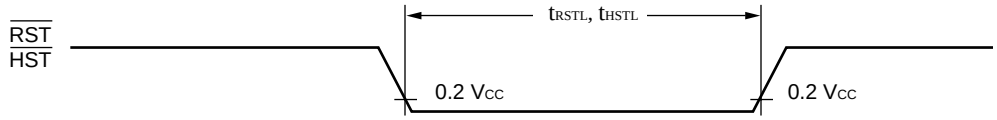
Murata Mfg. Co., Ltd.

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

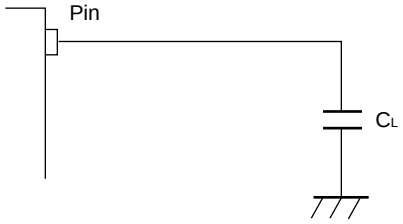
(4) Reset and Hardware Standby Inputs

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		16 t_{CP}	—	ns	



- **Conditions for Measurement of AC Reference**



C_L: Load capacity during testing

For CLK and ALE, C_L = 30 pF.
For address and data buses (AD15 to AD00), $\overline{RD}$ and $\overline{WR}$, C_L = 80 pF.

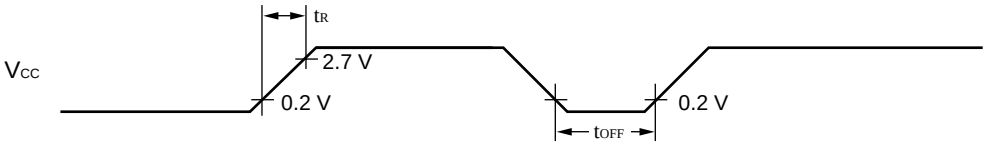
(5) Power-on Reset

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

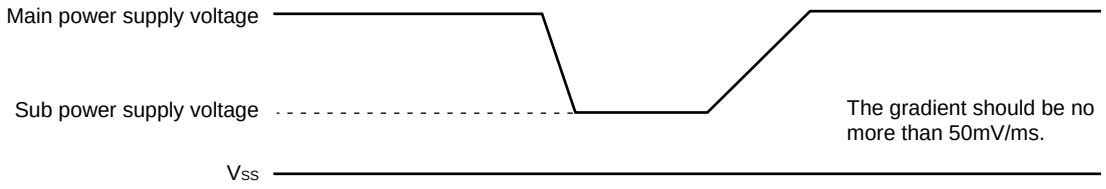
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}		1	—	ms	For repetition of the operation

* : V_{CC} should be lower than 0.2 V before power supply rise.

Notes: • The above values are the values required for a power-on reset
- .When $\overline{HST}$ = “L”, this standard must be followed to turn on power supply for power-on reset whether or not necessary.
- The device has built-in registers which are initialized only by power-on reset. For possible initialization of these registers, turn on power supply according to this standard.



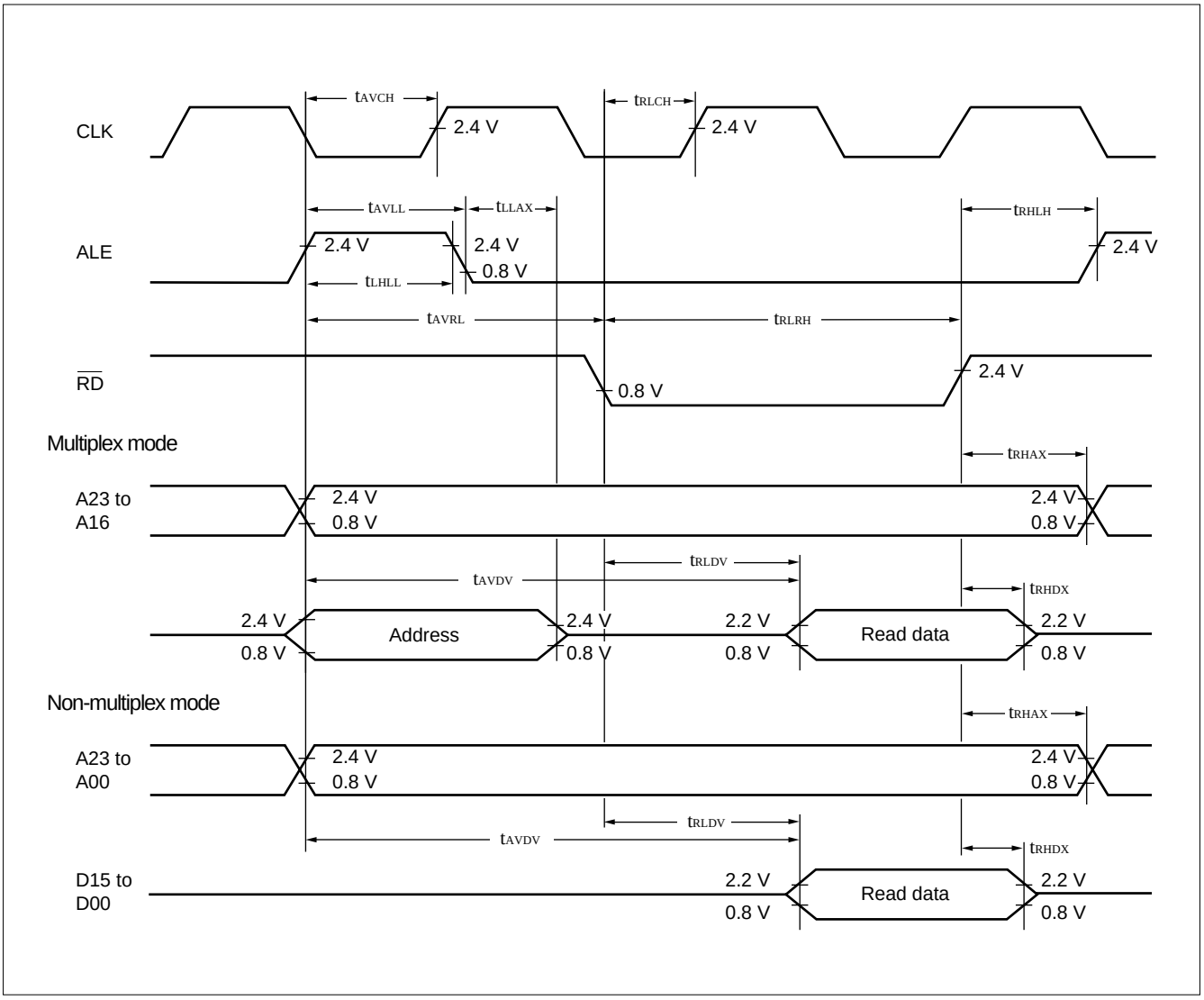
Abrupt changes in the power supply voltage may cause a power-on reset.
When changing the power supply voltage during operation, the change should be as smooth as possible, as shown in the following figure.



(6) Bus Timing (Read)

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

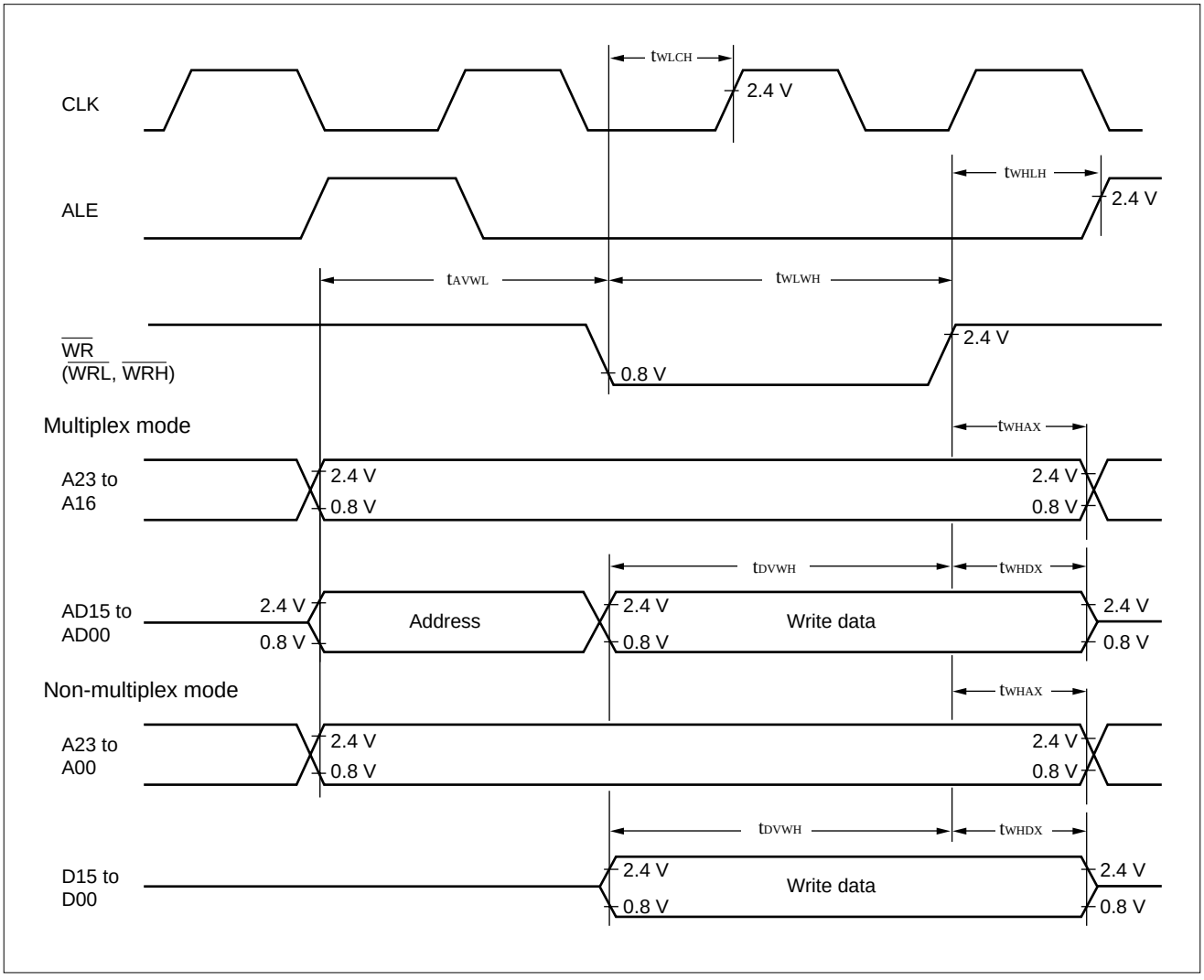
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	V_{CC} = +5.0 V±10%	$t_{CP}/2 - 20$	—	ns	
			V_{CC} = +3.0 V±10%	$t_{CP}/2 - 35$	—	ns	
Valid address → ALE ↓ time	t_{AVLL}	Address	V_{CC} = +5.0 V±10%	$t_{CP}/2 - 20$	—	ns	
			V_{CC} = +3.0 V±10%	$t_{CP}/2 - 40$	—	ns	
ALE ↓ → address valid time	t_{LLAX}	Address	—	$t_{CP}/2 - 15$	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, Address		$t_{CP} - 15$	—	ns	
Valid address → valid data input	t_{AVDV}	Address/ data	V_{CC} = +5.0 V±10%	—	$5\ t_{CP}/2 - 60$	ns	
			V_{CC} = +3.0 V±10%	—	$5\ t_{CP}/2 - 80$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	$3\ t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → valid data input	t_{RLDV}	Data	V_{CC} = +5.0 V±10%	—	$3\ t_{CP}/2 - 60$	ns	
			V_{CC} = +3.0 V±10%		$3\ t_{CP}/2 - 80$	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}		—	0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ → address valid time	t_{RHAX}	Address, $\overline{RD}$		$t_{CP}/2 - 10$	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	Address, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	


CLK
ALE
RD
Multiplex mode
A23 to A16
A23 to A00
D15 to D00
Non-multiplex mode
tAVCH
tRLCH
tAVLL
tLLAX
tLHLL
tRHLH
tAVRL
tRLRH
tRHAX
tRLDV
tAVDV
tRHDX
2.4 V
0.8 V
2.2 V
Address
Read data

(7) Bus Timing (Write)

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$		3 t_{CP}/2 – 20	—	ns	
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	Data		3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}		V_{CC} = +5.0 V±10%	20	—	ns	
			V_{CC} = +3.0 V±10%	30	—	ns	
$\overline{WR}$ ↑ → address valid time	t_{WHAX}	Address	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	ALE, $\overline{WRL}$, $\overline{WRH}$		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↓ time	t_{WLCL}	$\overline{WRL}$, $\overline{WRH}$, CLK		t_{CP}/2 – 20	—	ns	

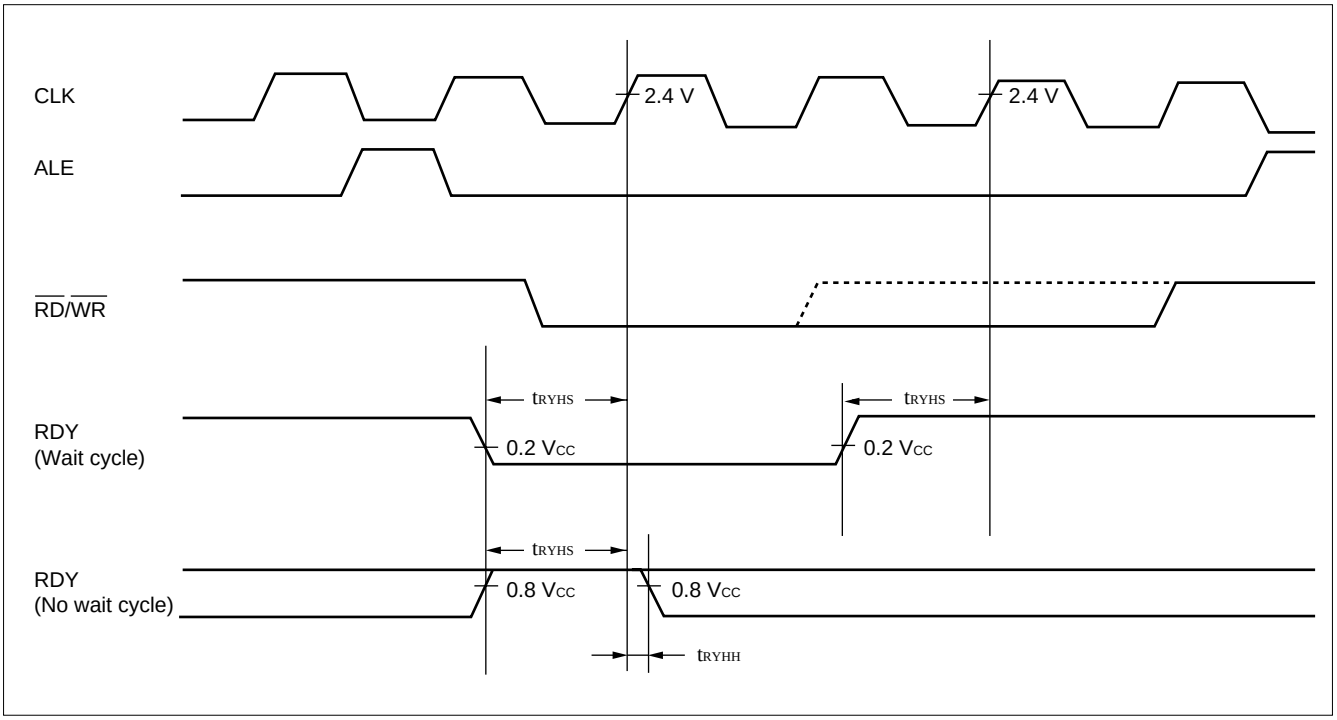


(8) Ready Input Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	V_{CC} = +5.0 V±10%	45	—	ns	
			V_{CC} = +3.0 V±10%	70	—	ns	
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note: Use the auto-ready function if the setup time at fall of the RDY is too short.

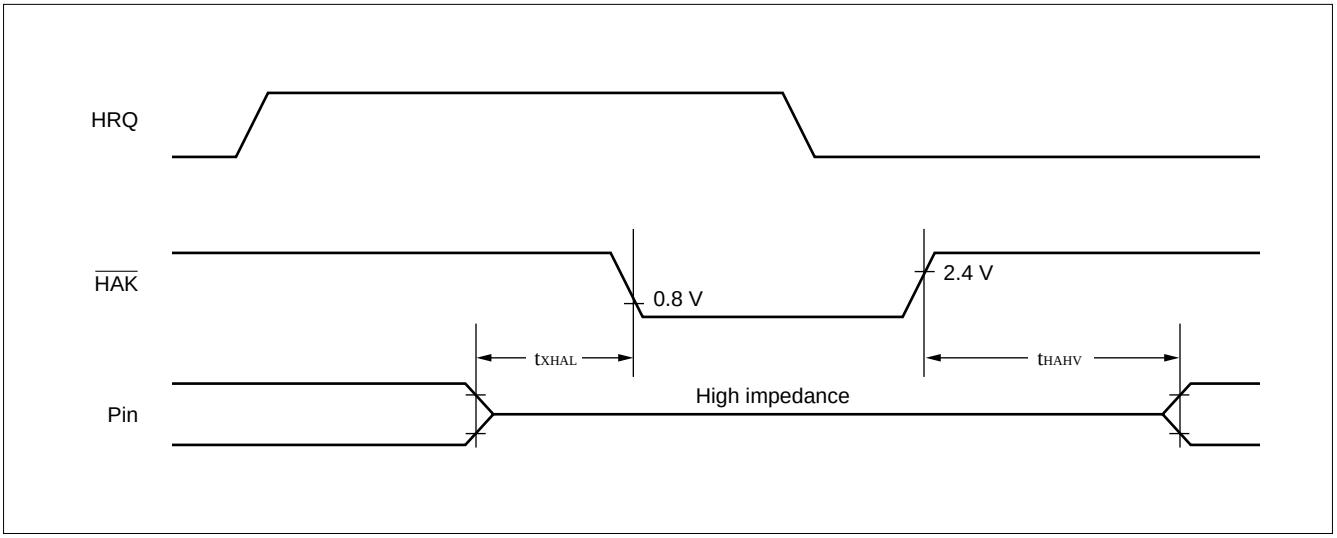


(9) Hold Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → pin valid time	t_{HAHV}	$\overline{HAK}$	—	t_{CP}	2 t_{CP}	ns	

Note: After reading HRQ, more than one cycle is required before changing $\overline{HAK}$.



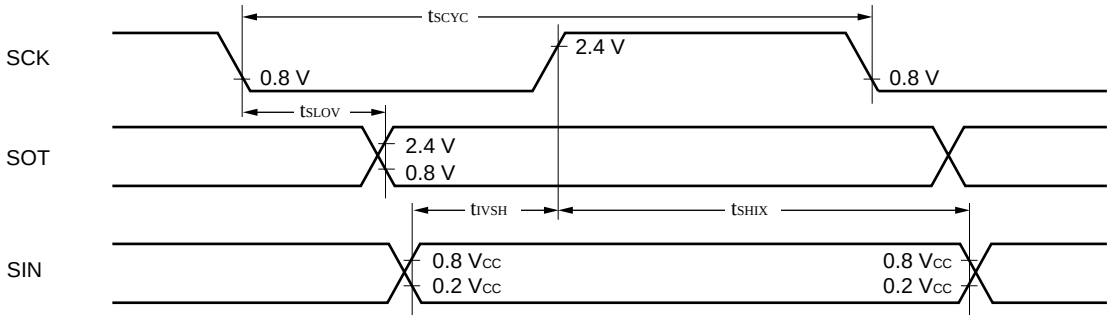
(10) I/O Expansion Serial Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

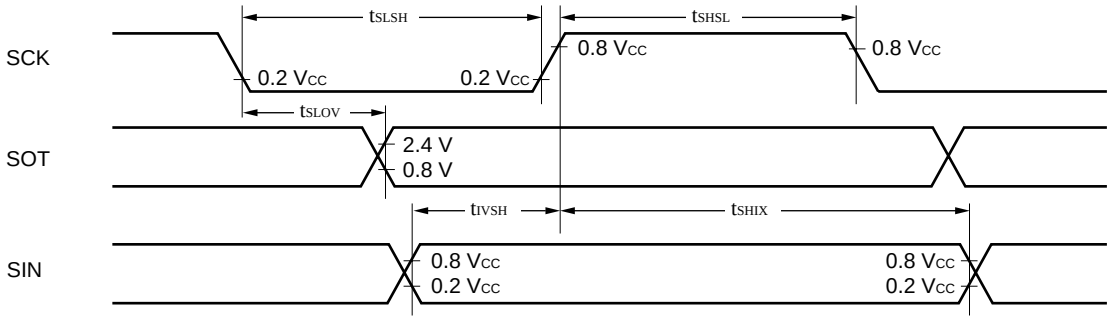
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to 2	—	8 t_{CP}	—	ns	C_L = 80 pF + 1 TTL for the internal shift clock mode output pin.
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to 2 SOT0 to 2	V_{CC} = +5.0 V±10%	–80	80	ns	
			V_{CC} = +3.0 V±10%	–120	120	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to 2 SIN0 to 2	V_{CC} = +5.0 V±10%	100	—	ns	
			V_{CC} = +3.0 V±10%	200	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to 2 SIN0 to 2	V_{CC} = +5.0 V±10%	60	—	ns	
			V_{CC} = +3.0 V±10%	120	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to 2	—	4 t_{CP}	—	ns	C_L = 80 pF + 1 TTL for the external shift clock mode output pin.
Serial clock “L” pulse width	t_{SLSH}	SCK0 to 2	—	4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to 2 SOT0 to 2	V_{CC} = +5.0 V±10%	—	150	ns	
			V_{CC} = +3.0 V±10%	—	200	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to 2 SIN0 to 2	V_{CC} = +5.0 V±10%	60	—	ns	
			V_{CC} = +3.0 V±10%	120	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to 2 SIN0 to 2	V_{CC} = +5.0 V±10%	60	—	ns	
			V_{CC} = +3.0 V±10%	120	—	ns	

Notes: • These are the AC characteristics for CLK synchronous mode.
• C_L is the load capacitance connected to the pin at testing.
• t_{CP} is the machine cycle period (unit: ns).

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

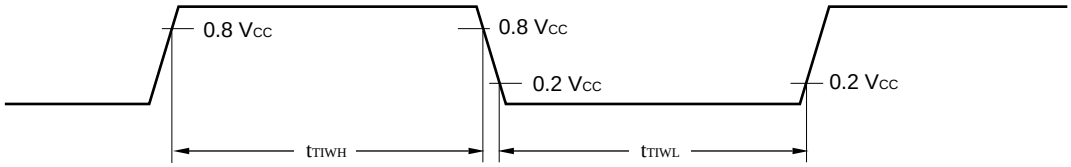


(11) Timer Input Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	$t_{TIWH/L}$	TIN0 to 1	—	4 t_{CP}	—	ns	

- **Timer Input Timing**

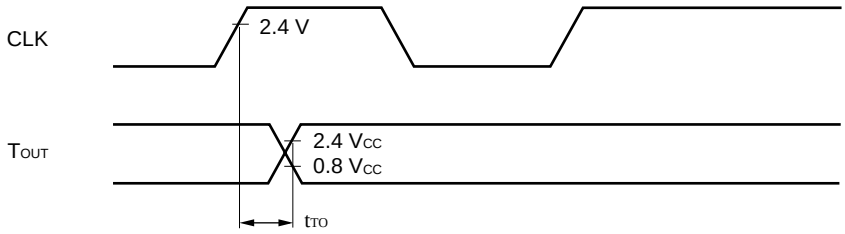


(12) Timer Output Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change timing	t_{TO}	TOT0 to 1	V_{CC} = +5.0 V±10%	30	—	ns	
			V_{CC} = +3.0 V±10%	80	—	ns	

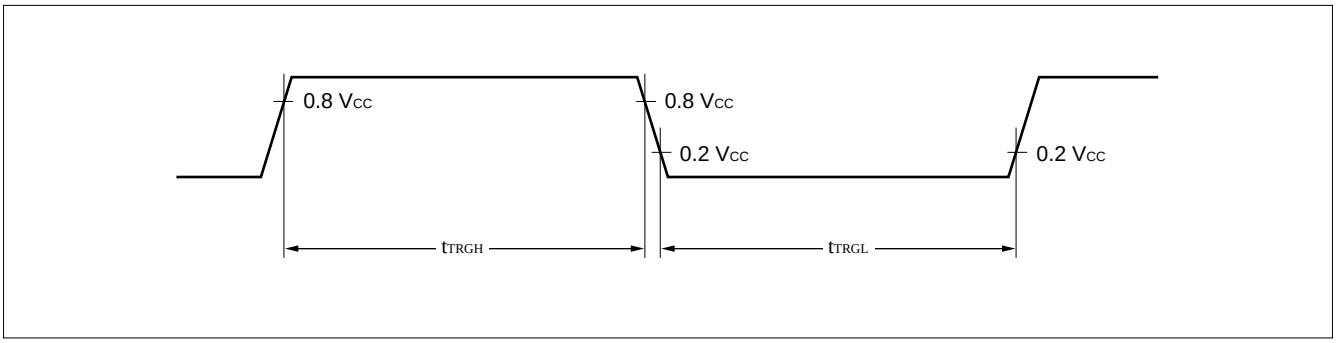
- **Timer Output Timing**



(13) Trigger Input Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

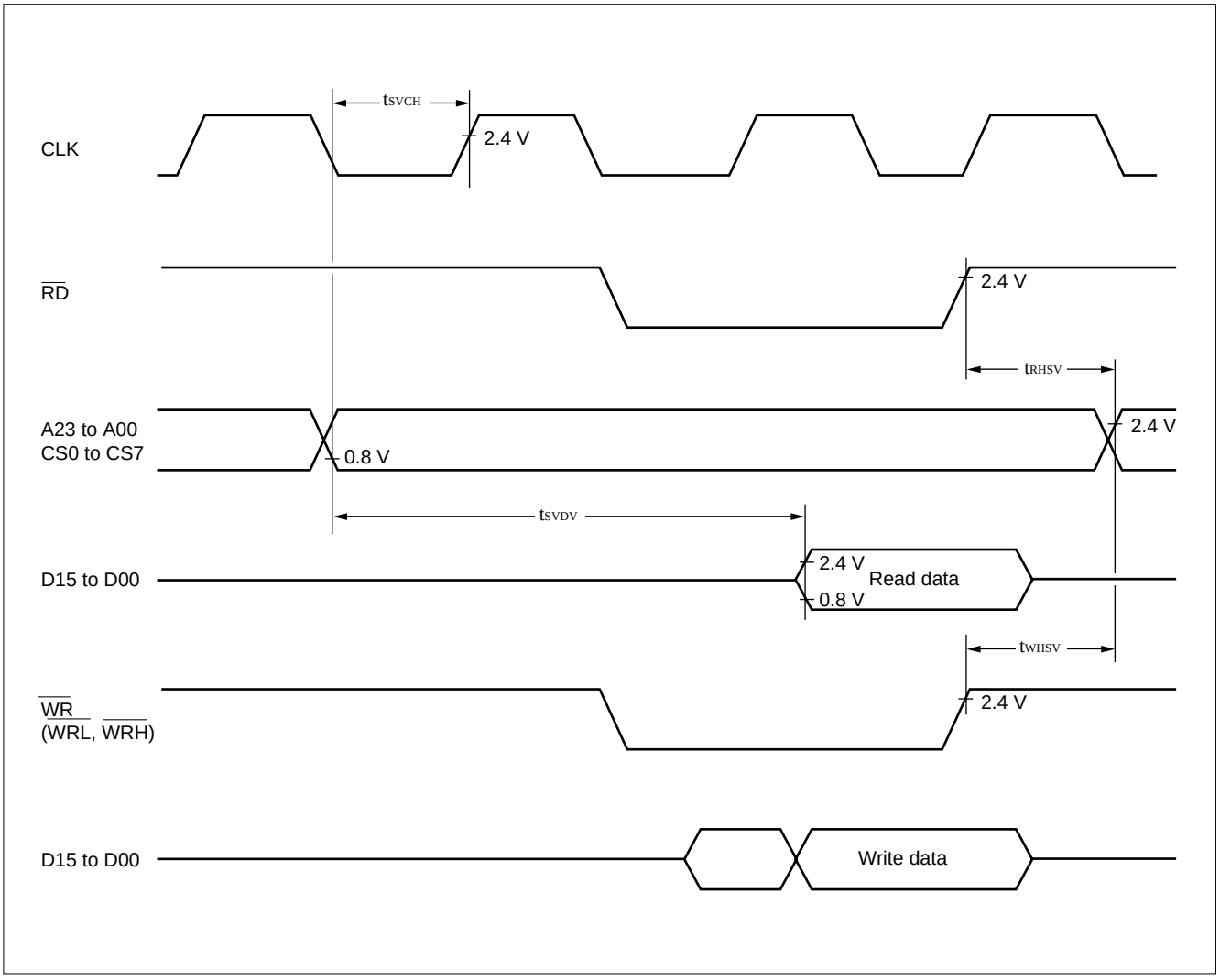
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	$\overline{ATG}$ INT0 to INT1	—	5 t_{CP}	—	ns	



(14) Chip Select Output Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Chip select enabled → Valid data input time	t_{SVDV}	CS0 to CS7 D15 to D00	V_{CC} = +5.0 V±10%	—	5 t_{CP}/2 – 60	ns	
			V_{CC} = +3.0 V±10%	—	5 t_{CP}/2 – 80	ns	
$\overline{RD}$ ↑ → Chip select enabled time	t_{RHSV}	CS0 to CS7 $\overline{RD}$	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → Chip select enabled time	t_{WHSV}	CS0 to CS7 $\overline{WRH}$, $\overline{WRL}$	—	t_{CP}/2 – 10	—	ns	
Enabled chip select → CLK ↑ time	t_{SVCH}	CS0 to CS7 CLK	—	—	t_{CP}/2 – 20	ns	


tSVCH
2.4 V
CLK
RD
2.4 V
tRHSV
A23 to A00
CS0 to CS7
0.8 V
2.4 V
tSVDV
D15 to D00
2.4 V
Read data
0.8 V
tWHSV
WR
(WRL, WRH)
2.4 V
D15 to D00
Write data

5. A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = +2.7 V to +5.5 V, AV_{SS} = V_{SS} = 0.0 V, 2.7 V ≤ AVRH – AVRL, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	±3.0	LSB
Linearity error	—	—	—	—	±2.0	LSB
Differential linearity error	—	—	—	—	±1.5	LSB
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 4.5	AVRH – 1.5	AVRH + 0.5	LSB
Conversion time	—	—	6.125*1	—	—	µs
			12.25*2	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V
Reference voltage	—	AVRH	AVRL + 2.7	—	AV_{CC}	V
	—	AVRL	0	—	AVRH – 2.7	V
Power supply current	I_A	AV_{CC}	—	3	—	mA
	I_{AH}	AV_{CC}	—	—	5*3	µA
Reference voltage supply current	I_R	AVRH	—	200	—	µA
	I_{RH}	AVRH	—	—	5*3	µA
Variation between channels	—	AN0 to AN7	—	—	4	LSB

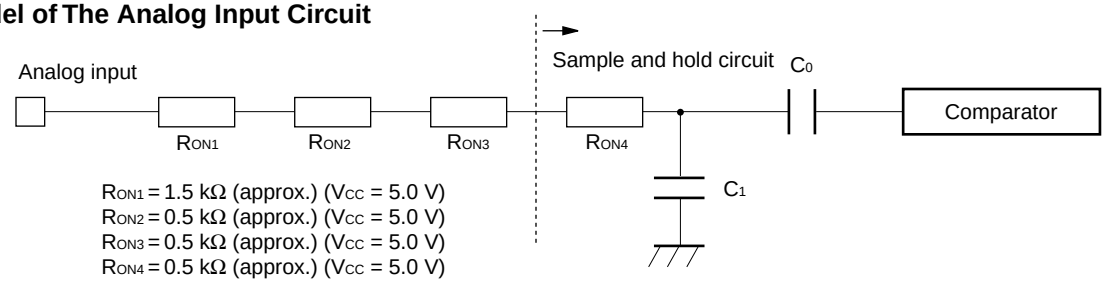
*1: For V_{CC} = +5.0 V±10% and a 16 MHz machine clock

*2: For V_{CC} = +3.0 V±10% and a 8 MHz machine clock

*3: The current when the A/D converter is not operating or the CPU is in stop mode (for V_{CC} = AV_{CC} = AVRH = +5.0 V).

Notes:
- The relative error increases as |AVRH – AVRL| decreases.
- The output impedance of the external circuit for the analog input should be in the following range.
  Output impedance of external circuit < approx. 7 kΩ
- If the output impedance of the external circuit is too high, the sampling time for the analog voltage may be too short. (Sampling time = 3.75 µs @4 MHz (This corresponds to 16 MHz internal operation if the multiplier is 4.))
- For an external capacitor to be provided outside the chip, its capacity should desirably be thousands times larger than that of the capacity in the chip taking in consideration the influence of the capacity distribution of the external and internal capacitors.

- **Model of The Analog Input Circuit**

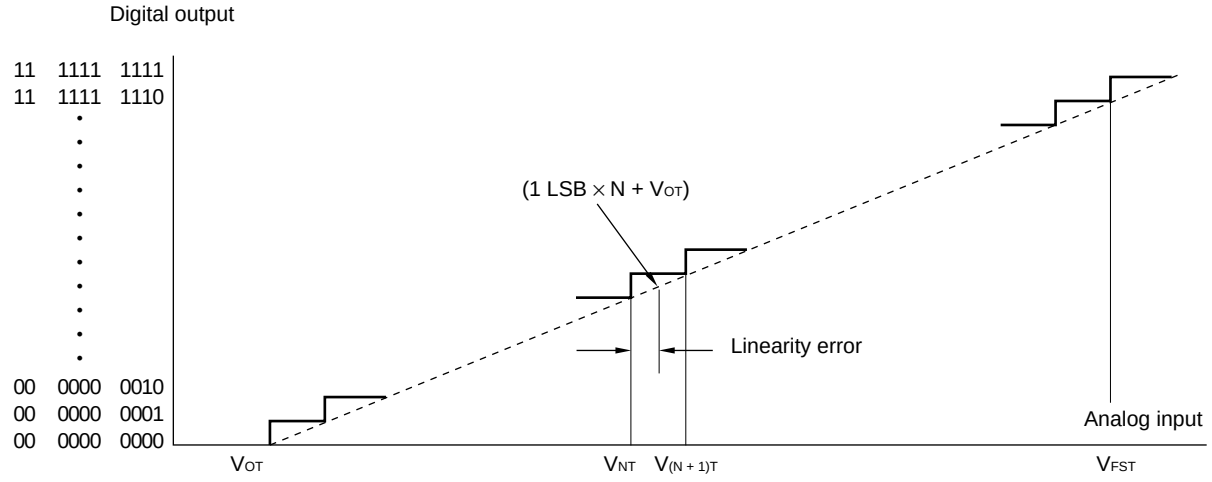


R_{ON1} = 1.5 kΩ (approx.) (V_{CC} = 5.0 V)
R_{ON2} = 0.5 kΩ (approx.) (V_{CC} = 5.0 V)
R_{ON3} = 0.5 kΩ (approx.) (V_{CC} = 5.0 V)
R_{ON4} = 0.5 kΩ (approx.) (V_{CC} = 5.0 V)
C_0 = 60 pF (approx.)
C_1 = 4 pF (approx.)

Note: The above values are for reference only.

6. A/D Converter Glossary

- Resolution
  The change in analog voltage that can be recognized by the A/D converter.
  If the resolution is 10 bits, the analog voltage can be resolved into 2^{10} = 1024 steps.
- Total error
  The deviation between the actual and logic value attributable to offset error, gain error, non-linearity error, and noise.
- Linearity error
  The deviation between the actual conversion characteristic of the device and the line linking the zero transition point (00 0000 0000 ↔ 00 0000 0001) and the full scale transition point (11 1111 1110 ↔ 11 1111 1111).
- Differential linearity error
  The variation from the ideal input voltage required to change the output code by 1 LSB.



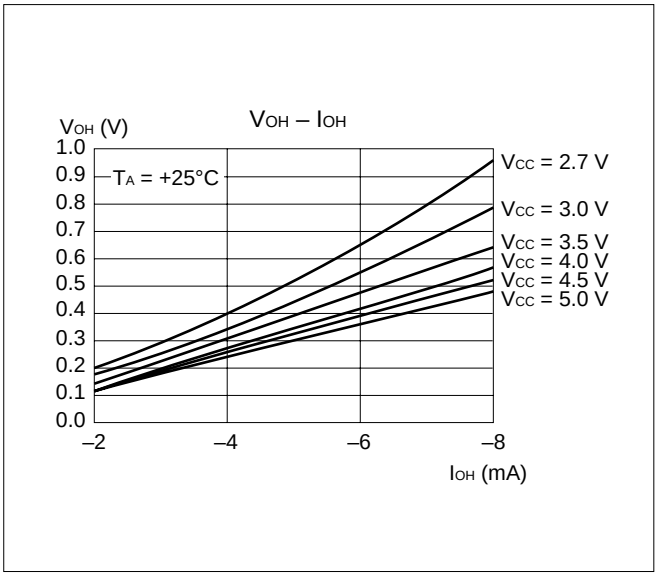
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}\ \text{(LSB)}$$

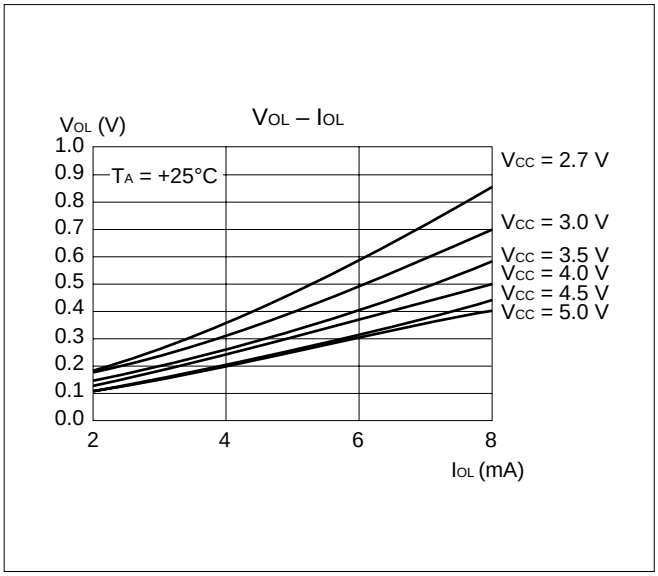
$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{(LSB)}$$

■ EXAMPLES CHARACTERISTICS

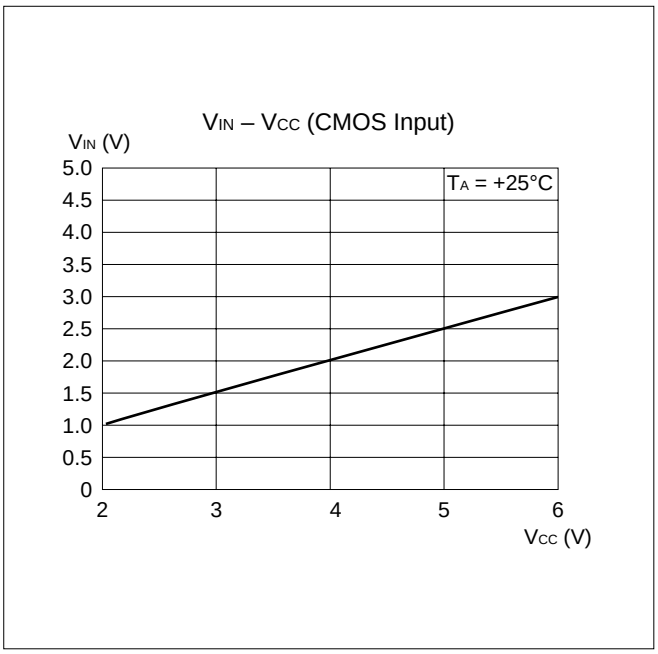
(1) "H" Level Output Voltage



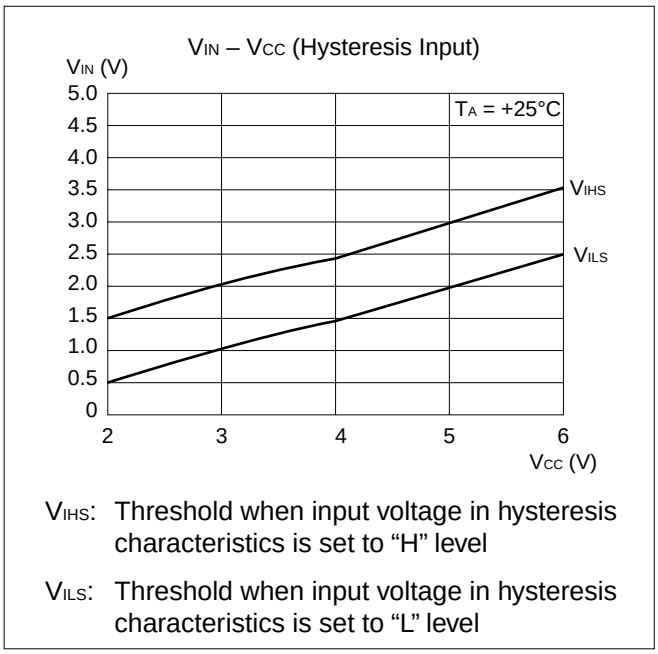
(2) "L" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage



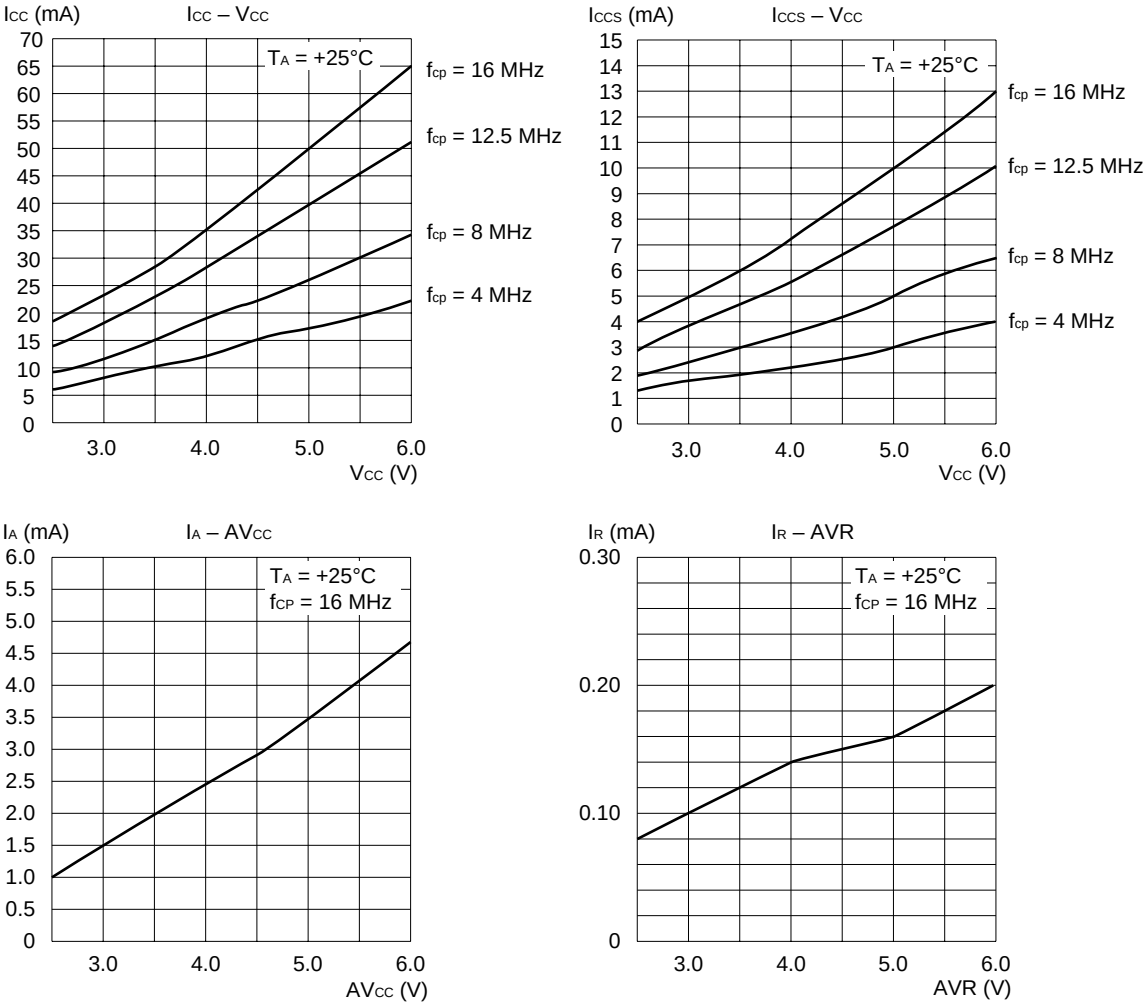
(4) "H" Level Input Voltage/"L" Level Input Voltage



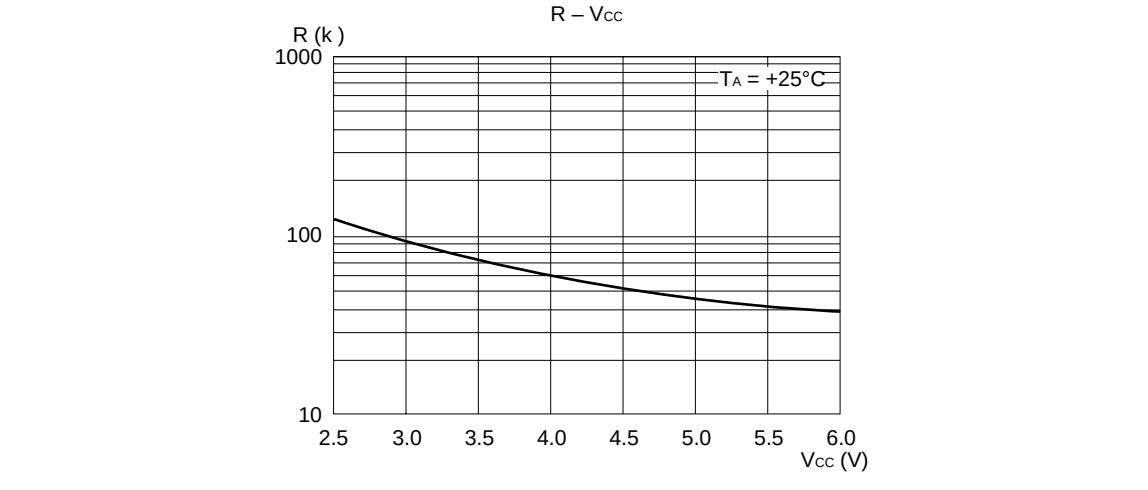
V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

(5) Power Supply Current (fcp = internal frequency)



(6) Pull-up Resistance



■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00_H to AH. X : Transfers 00_H or FF_H to AH by signing and extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL:AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000_H to $0000FF_H$)
imm4 imm8 imm16 imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address

(Continued)

(Continued)

Symbol	Meaning
rel	Branch specification relative to PC
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation	Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 RW0 RL0 R1 RW1 (RL0) R2 RW2 RL1 R3 RW3 (RL1) R4 RW4 RL2 R5 RW5 (RL2) R6 RW6 RL3 R7 RW7 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3	Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +	Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8	Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16	Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a) Number of execution cycles for each type of addressing	Number of register accesses for each type of addressing
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	4 4 2 1	2 2 0 0

Note: “(a)” is used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Number of cycles	Number of access	Number of cycles	Number of access	Number of cycles	Number of access
Internal register	+0	1	+0	1	+0	2
Internal memory even address Internal memory odd address	+0 +0	1 1	+0 +2	1 2	+0 +4	2 4
Even address on external data bus (16 bits) Odd address on external data bus (16 bits)	+1 +1	1 1	+1 +4	1 2	+2 +8	2 4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes: • “(b)”, “(c)”, and “(d)” are used in the “~” (number of states) column and column B (correction value) in the tables of instructions.
• When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes: • When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.
• Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for “worst case” calculations.

Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	Z	*	–	–	–	*	*	–	–	–
MOVN A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX A, ear	2	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX A, io	2	3	0	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX A, @A	2	3	0	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX A,@RWi+disp8	2	5	1	(b)	byte (A) ← ((RWi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOV dir, A	2	3	0	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV addr16, A	3	4	0	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, A	1	2	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV ear, A	2	2	1	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV eam, A	2+	3+ (a)	0	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV io, A	2	3	0	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV @RLi+disp8, A	3	10	2	(b)	byte ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, ear	2	3	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV Ri, eam	2+	4+ (a)	1	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOV ear, Ri	2	4	2	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV eam, Ri	2+	5+ (a)	1	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV io, #imm8	3	5	0	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV ear, #imm8	3	2	1	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV eam, #imm8	3+	4+ (a)	0	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV @AL, AH /MOV @A, T	2	3	0	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCH A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH A, eam	2+	5+ (a)	0	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH Ri, eam	2+	9+ (a)	2	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	1	0	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	3	0	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	1	0	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	1	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	3+ (a)	0	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	3	0	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	3	2	(0)	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	4+ (a)	1	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	5+ (a)	1	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW AL, AH /MOVW @A, T	2	3	0	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	5+ (a)	0	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	9+ (a)	2	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
MOVL A, ear	2	4	2	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	4	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD A,#imm8	2	2	0	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD A, dir	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD A, ear	2	3	1	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD ear, A	2	3	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADD eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, ear	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC A	1	3	0	0	byte (A) ← (AH) + (AL) + (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
SUB A, #imm8	2	2	0	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB A, dir	2	5	0	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB A, ear	2	3	1	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB ear, A	2	3	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUB eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC A	1	2	0	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, ear	2	3	1	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC A	1	3	0	0	byte (A) ← (AH) – (AL) – (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW A	1	2	0	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW A, ear	2	3	1	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW A, #imm16	3	2	0	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW ear, A	2	3	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADDW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW A, ear	2	3	1	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW A	1	2	0	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW A, ear	2	3	1	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW A, #imm16	3	2	0	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW ear, A	2	3	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUBW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW A, ear	2	3	1	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL A, ear	2	6	2	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL A, #imm32	5	4	0	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL A, ear	2	6	2	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL A, #imm32	5	4	0	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC	ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC	ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW	ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW	ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL	ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL	ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP	A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP	A, ear	2	2	1	0	byte (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMP	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMP	A, #imm8	2	2	0	0	byte (A) ← imm8	–	–	–	–	–	*	*	*	*	–
CMPW	A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW	A, ear	2	2	1	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPW	A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPW	A, #imm16	3	2	0	0	word (A) ← imm16	–	–	–	–	–	*	*	*	*	–
CMPL	A, ear	2	6	2	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPL	A, eam	2+	7+ (a)	0	(d)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPL	A, #imm32	5	3	0	0	word (A) ← imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU	A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU	A, eam	2+	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2+	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	1	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2+	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.
*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.
*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.
*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.
*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.
*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.
*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.
*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.
*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.
*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.
*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 13 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	3	1	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
AND	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	3	1	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
OR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XOR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	3	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOT	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	3	1	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	2	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	3	1	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	2	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	3	1	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	3	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOTW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 14 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ea	2	6	2	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

Table 15 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	3	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	3	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

Table 16 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) ← Shift until first digit is "1" byte (R0) ← Current shift count	–	–	–	–	–	–	*	–	–	–

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 17 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	0	byte (A) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	3	2	0	byte (ear) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	3	2	0	byte (ear) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–

*1: 6 when R0 is 0, 5 + (R0) in all other cases.
*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 18 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch when (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	0	Branch when (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	0	Branch when (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	0	Branch when (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	0	Branch when (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	0	Branch when (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	0	Branch when (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	0	Branch when (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	0	Branch when (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	0	Branch when (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	0	Branch when (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	0	Branch when (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	0	Branch when (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	0	Branch when (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	3	0	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	1	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2+	4+ (a)	0	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear +2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2+	7+ (a)	0	2× (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	7	0	2× (c)	Vector call instruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	10	2	2× (c)	word (PC) ← (ear) 0 to 15 (PCB) ← (ear) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2+	11+ (a)	0	*2	word (PC) ← (eam) 0 to 15 (PCB) ← (eam) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	10	0	2× (c)	word (PC) ← addr0 to 15, (PCB) ← addr16 to 23	–	–	–	–	–	–	–	–	–	–

*1: 4 when branching, 3 when not branching.
*2: (b) + 3 × (c)
*3: Read (word) branch address.
*4: W: Save (word) to stack; R: read (word) branch address.
*5: Save (word) to stack.
*6: W: Save (long word) to W stack; R: read (long word) R branch address.
*7: Save (long word) to stack.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 19 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE A, #imm16, rel	4	*1	0	0	Branch when word (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE eam, #imm8, rel*9	4+	*3	0	(b)	Branch when byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE ear, #imm16, rel	5	*4	1	0	Branch when word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE eam, #imm16, rel*9	5+	*3	0	(c)	Branch when word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ ear, rel	3	*5	2	0	Branch when byte (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ eam, rel	3+	*6	2	2× (b)	Branch when byte (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ ear, rel	3	*5	2	0	Branch when word (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ eam, rel	3+	*6	2	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT #vct8	2	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT addr16	3	16	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP addr24	4	17	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9	1	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI	1	15	0	6× (c)	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK #local8	2	6	0	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK	1	5	0	(c)	At constant entry, retrieve old frame pointer from stack.	–	–	–	–	–	–	–	–	–	–
RET *7	1	4	0	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *8	1	6	0	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

*1: 5 when branching, 4 when not branching
*2: 13 when branching, 12 when not branching
*3: 7 + (a) when branching, 6 + (a) when not branching
*4: 8 when branching, 7 when not branching
*5: 7 when branching, 6 when not branching
*6: 8 + (a) when branching, 7 + (a) when not branching
*7: Retrieve (word) from stack
*8: Retrieve (long word) from stack
*9: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 20 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*5	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	0	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	0	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	4	0	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*5	*4	(rlst) ← ((SP)), (SP) ← (SP) +2n	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	14	0	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	1	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	1	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	1	0	0	word(A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	0	word (SP) ← (SP) +ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	0	word (SP) ← (SP) +imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	0	No operation	–	–	–	–	–	–	–	–	–	–
ADB	1	1	0	0	Prefix code for accessing AD space	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	0	Prefix code for accessing DT space	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	0	Prefix code for accessing PC space	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	0	Prefix code for accessing SP space	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	0	Prefix code for common register bank	–	–	–	–	–	–	–	–	–	–

*1: PCB, ADB, SSB, USB, and SPB : 1 state
DTB, DPR : 2 states

*2: 7 + 3 × (pop count) + 2 × (last register number to be popped), 7 when rlst = 0 (no transfer register)

*3: 29 + (push count) – 3 × (last register number to be pushed), 8 when rlst = 0 (no transfer register)

*4: Pop count × (c), or push count × (c)

*5: Pop count or push count.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 21 Bit Manipulation Instructions [21 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB	A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	io:bp, A	3	6	0	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS	addr16:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS	io:bp	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC	io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

*1: 8 when branching, 7 when not branching
*2: 7 when branching, 6 when not branching
*3: 10 when condition is satisfied, 9 when not satisfied
*4: Undefined count
*5: Until condition is satisfied

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 22 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 to 7 ↔ (A) 8 to 15	–	–	–	–	–	–	–	–	–	–
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) ↔ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	0	byte sign extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	0	word sign extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	0	byte zero extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	1	0	0	word zero extension	–	Z	–	–	–	R	*	–	–	–

Table 23 String Instructions [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*5	*3	Byte transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*5	*3	Byte transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*5	*4	Byte retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FISL/FILSI	2	6m +6	*5	*3	Byte filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*8	*6	Word transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*8	*6	Word transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*8	*7	Word retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	6m +6	*8	*6	Word filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)
n: Loop count

*1: 5 when RW0 is 0, 4 + 7 × (RW0) for count out, and 7 × n + 5 when match occurs
*2: 5 when RW0 is 0, 4 + 8 × (RW0) in any other case
*3: (b) × (RW0) + (b) × (RW0) when accessing different areas for the source and destination, calculate (b) separately for each.
*4: (b) × n
*5: 2 × (RW0)
*6: (c) × (RW0) + (c) × (RW0) when accessing different areas for the source and destination, calculate (c) separately for each.
*7: (c) × n
*8: 2 × (RW0)

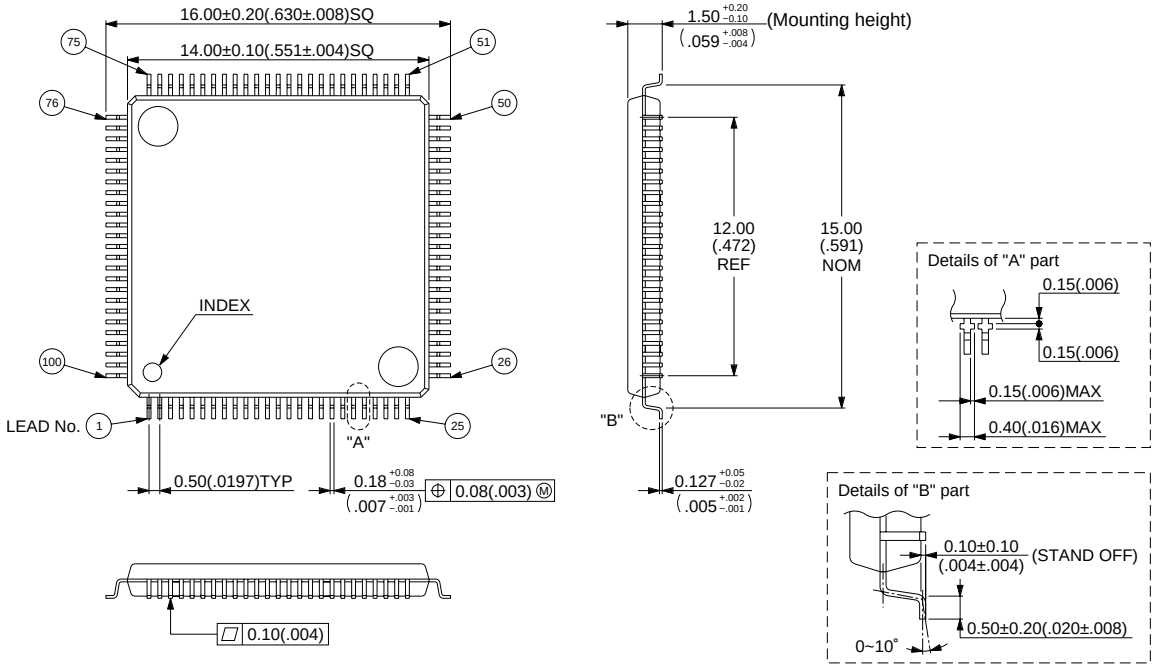
Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90611APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90611APF	100-pin Plastic QFP (FPT-100P-M06)	

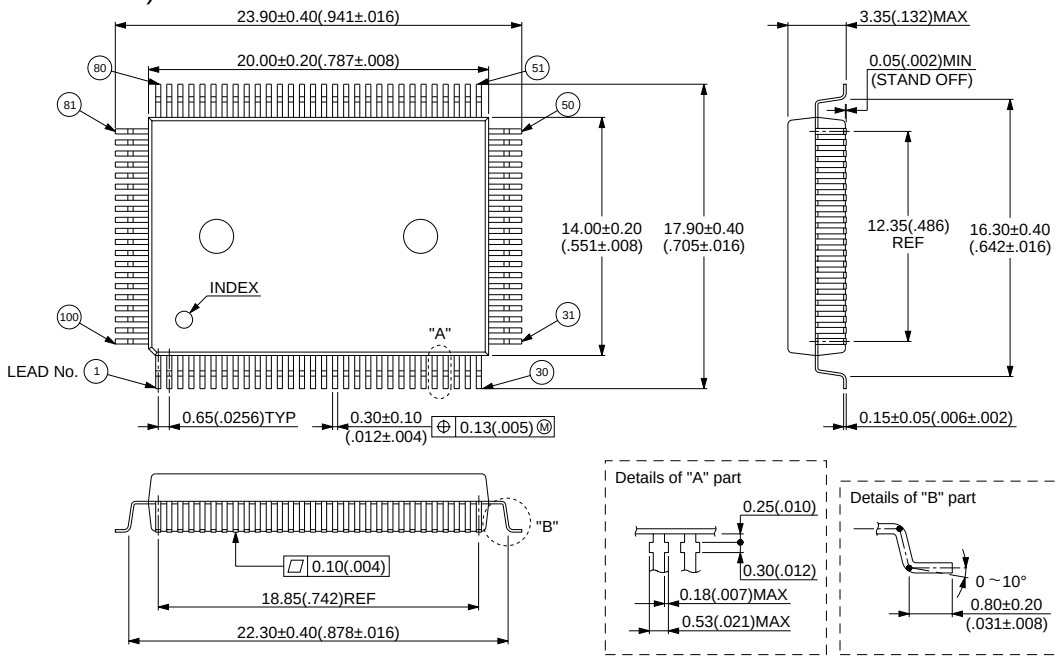
■ PACKAGE DIMENSIONS

100-pin Plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

100-pin Plastic QFP
(FPT-100P-M06)



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