Preliminary Information

High-power, Four-channel Programmable DC-DC System Power Managers

FEATURES & APPLICATIONS

- **Digital programming of all major parameters via I^2C interface and non-volatile memory**
  - **Output voltage set point**
  - **Input/battery voltage monitoring**
  - **Output power-up/down sequencing**
  - **Digital soft-start and output slew rate**
  - **Dynamic voltage control of all outputs**
  - **UV/OV monitoring of all outputs**
  - **Enable/Disable outputs independently**
- **User friendly Graphical User Interface (GUI)**
- **Four synchronous step-down output channels**
- **Integrated RESET monitor**
- **+2.7V to +6.0V Input Range**
- **Highly accurate output voltage: <1.5%**
- **Factory programmable dead times**
- **0% to 100% Duty Cycle operation**
- **Undervoltage Lockout (UVLO) with hysteresis**
- **250kHz (SMB117A), 400kHz (SMB117), 800kHz (SMB113A), 1MHz (SMB113B) operating frequency**
- **96 bytes of user configurable nonvolatile memory**

Applications

- **Car & Marine Navigation Systems**
- **Set-top Boxes**
- **TVs**
- **DDR Memory**
- **Mobile Computing/PDAs**
- **Office Equipment**
- **DMB Systems**

INTRODUCTION

The SMB113A/B and SMB117/A are highly integrated and flexible four-channel power managers designed for use in a wide range of applications. The built-in digital programmability allows system designers to custom tailor the device to suit almost any multi-channel power supply application from digital camcorders to set-top boxes. Complete with a user friendly GUI, all programmable settings, including output voltages and input/output voltage monitoring, can be customized with ease.

The SMB113A/B and SMB117/A integrate all the essential blocks required to implement a complete four-channel power subsystem consisting of four synchronous step-down "buck" controllers. Additionally sophisticated power control/monitoring functions required by complex systems are built-in. These include digitally programmable output voltage set point, power-up/down sequencing, enable/disable, dynamic voltage management and UV/OV monitoring on all channels.

The integration of features and built-in flexibility of the SMB113A/B and SMB117/A allows the system designer to create a "platform solution" that can be easily modified via software without major hardware changes. Combined with the re-programmability of the SMB113A/B and SMB117/A, this facilitates rapid design cycles and proliferation from a base design to future product generations.

The SMB113A/B and SMB117/A are suited to a wide variety of applications with an input range of +2.7V to +6.0V. Higher input voltage operation can easily be implemented with a small number of external components. Output voltages are extremely accurate (<1.5%). Communication is accomplished via the industry standard I^2C bus. All user-programmed settings are stored in non-volatile EEPROM of which 96 bytes may be used as general-purpose memory. The devices are offered in both the commercial and the industrial operating temperature range. The package type is a lead-free, RoHS compliant, 5x5 QFN-32.

SIMPLIFIED APPLICATIONS DRAWING

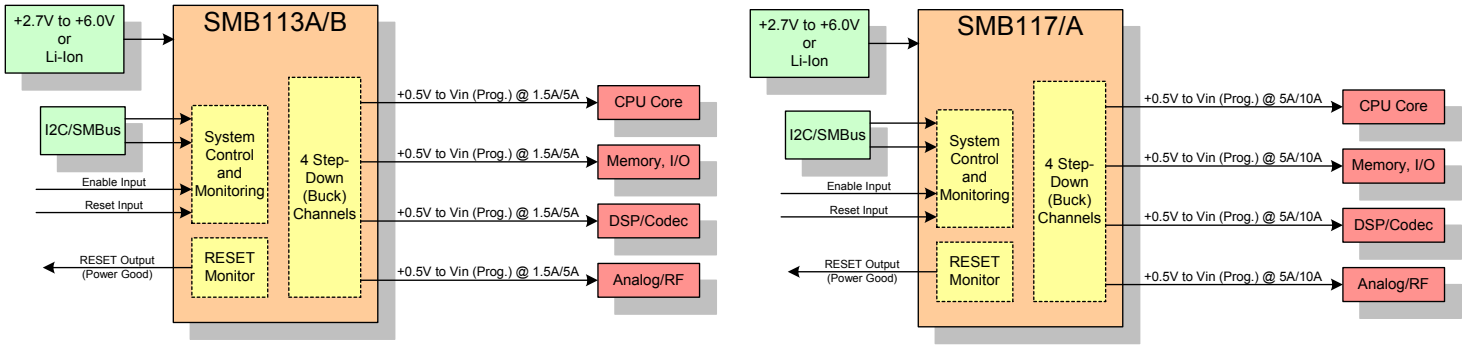


Figure 1 – Applications schematic featuring the SMB113A/B/117/A programmable DC-DC controllers.

Note: This is an applications example only. Some pins, components and values are not shown.

757 N. Mary Avenue • Sunnyvale CA 94085

Phone 408 523-1000 • FAX 408 523-1266

http://www.summitmicro.com/

GENERAL DESCRIPTION

The SMB113A/B and SMB117/A are fully programmable DC-DC controllers that incorporate power delivery and advanced power monitoring and control functionality. The devices integrate four synchronous "buck" step-down controllers in a space saving package.

The SMB113A uses a fixed 800kHz whereas the SMB113B uses a fixed 1MHz, the SMB117 a fixed 400kHz and the SMB117A a fixed 250kHz Pulse Width Modulation (PWM) control circuit. A type-three voltage mode compensation network is used offering a cost effective solution without compromising transient response performance. By utilizing external N- and P–type MOSFET transistors the efficiency and load current level can be customized to fit a wide array of system requirements.

The SMB113A/B and SMB117/A contain four buck outputs capable of producing an output voltage less than the input voltage. Each buck output voltage is set by an internal resistor divider and a programmable voltage reference. The integrated resistor divider eliminates the cost and space necessary for external components and has several programmable values. Through the programmability of the reference and the resistor divider, practically any output voltage smaller than the battery can be produced without the need to change external components.

The SMB113A/B and SMB117/A are capable of power-on/off cascade sequencing where each channel can be assigned one of four unique sequence positions. During sequencing each channel in a given sequencing position is guaranteed to reach its programmed output voltage before the channel(s) occupying the next sequence position initiate their respective soft-start sequence. A unique programmable delay exists between each power on/off sequence position. In addition to power on/off sequencing all supplies can be powered on/off individually through an I^2C command or by assertion of the enable pin.

Each output voltage is monitored for under-voltage and over-voltage (UV/OV) conditions, using a comparator-based circuit where the output voltage is compared against an internal programmable reference. An additional feature of the output voltage monitoring is a programmable glitch filter capable of digitally filtering a transient OV/UV fault condition from a true system error. When a fault is detected for a period in excess of the glitch filter, all supplies may be sequenced down or immediately disabled and an output status pin can be asserted. The current system status is always accessible via internal registers containing the status of all four channels.

The SMB113A/B and SMB117/A also possess an Under-voltage Lockout (UVLO) circuit to ensure the devices will not power up until the input voltage has reached a safe operating voltage. The UVLO function exhibits hysteresis, ensuring that noise or a brown out voltage on the supply rail does not inadvertently lead to a system failure.

The SMB113A/B and SMB117/A provide dynamic voltage management over all of their output voltages. Through an I^2C command, all output voltage levels can be increased or decreased to a pre-programmed level. In addition, each output is slew rate limited by soft-start circuitry that is user-programmable and requires no external capacitors.

All programmable settings on the SMB113A/B and the SMB117/A are stored in non-volatile registers and are easily accessed and modified over an industry standard I^2C serial bus. For fastest prototype development times Summit offers an evaluation card and a Graphical User Interface (GUI).

TYPICAL APPLICATION

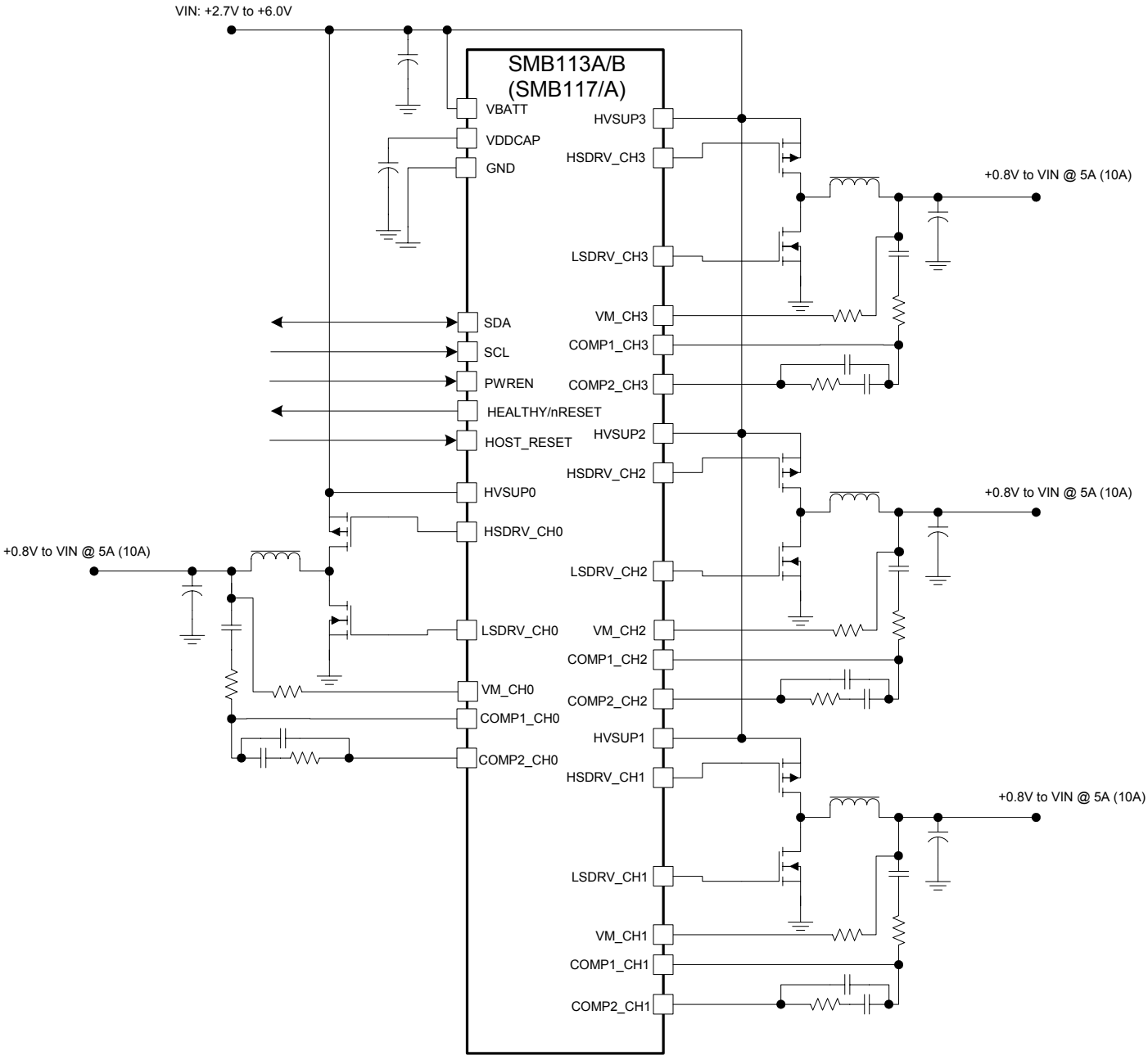


Figure 2 – Typical application schematic

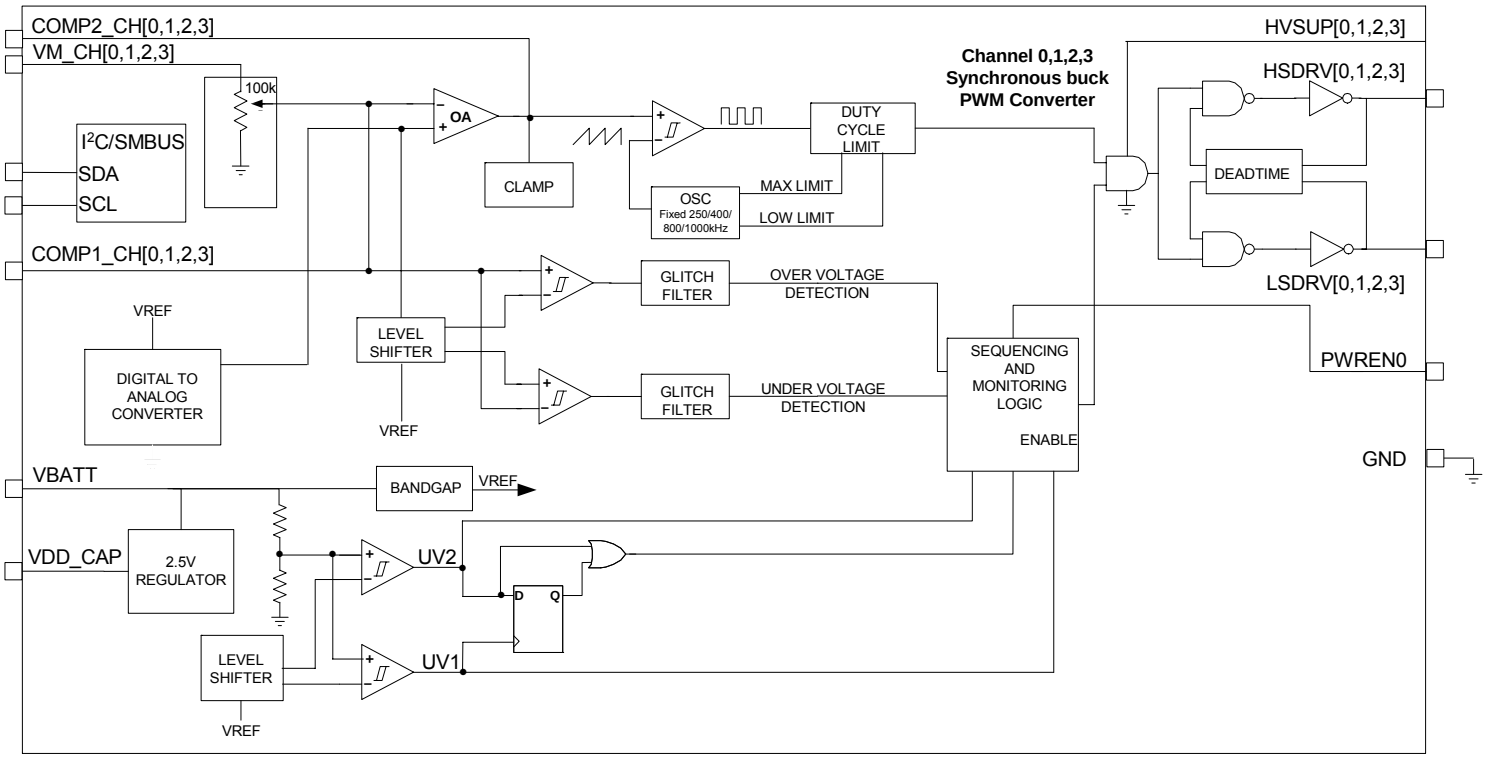


Figure 3 –SMB113A/B and SMB117/A internal block diagram. Programmable functional blocks include: level shifters, digital to analog converter and the VM_CH[0,1,2,3] voltage dividers.

PIN DESCRIPTION

Pin Number	Pin Type	Pin Name	Pin Description
1	OUT	HSDRV_CH0	The HSDRV_CH0 (Channel 0 High-side Driver) pin is the upper switching node of the channel 0 synchronous step-down buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH0 and assertion of LSDRV_CH0 to prevent excessive current flow during switching.
2	OUT	HEALTHY (nRESET)	The HEALTHY pin is an open drain output. High when all enabled output supplies are within the programmed levels. HEALTHY will ignore any disabled supply. There is a programmable glitch filter on the under-voltage and over-voltage sensors so that short transients outside of the limits will be ignored by HEALTHY. This pin can also be programmed to act as a Reset Output (nRESET). In this case, it releases with a programmable delay after all outputs are valid. When used, this pin should be pulled high by an external pull-up resistor.
3	IN	COMP1_CH0	The COMP1_CH0 (Channel 0 primary Compensation) pin is the primary feedback input of the channel 0 step-down buck controller. The COMP1_CH0 pin is internally connected to a programmable resistor divider.
4	IN	COMP2_CH0	The COMP2_CH0 (Channel 0 secondary Compensation) pin is the secondary feedback input of the channel 0 step-down buck controller.
5	IN	VM_CH0	The VM_CH0 (Channel 0 Voltage Monitor) pin connects the channel 0 step-down controller output. Internally the VM_CH0 pin connects to a programmable resistor divider.
6	I/O	SDA	SDA (Serial Data) is an open drain bi-directional pin used as the I^2C data line. SDA must be tied high through a pull-up resistor.
7	IN	SCL	SCL (Serial Clock) is an open drain input pin used as the I^2C clock line. SCL must be tied high through a pull-up resistor.
8	OUT	LSDRV_CH1	The LSDRV_CH1 (Channel 1 Low-side Driver) pin is the lower switching node of the channel 1 synchronous step-down buck controller. Attach to the gate of n-channel MOSFET.
9	PWR	HVSUP1	Channel 1 High Voltage Supply for Channel 1 buck driver.
10	OUT	HSDRV_CH1	The HSDRV_CH1 (Channel 1 High-side Driver) pin is the upper switching node of the channel 1 synchronous step-down buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH1 and assertion of LSDRV_CH1 to prevent excessive current flow during switching.
11	IN	HOST_RESET	The HOST_RESET pin is an active high reset input. When this pin is asserted high, the nRESET output will immediately go low. When HOST_RESET is brought low, nRESET will go high after a programmed reset delay. When pin 2 is used as a HEALTHY output, this pin needs to be attached to GND or VBATT via a resistor.
12	IN	COMP1_CH1	The COMP1_CH1 (Channel 1 primary Compensation) pin is the primary compensation input of the channel 1 step-down buck controller. The COMP1_CH1 pin is internally connected to a programmable resistor divider.
13	IN	COMP2_CH1	The COMP2_CH1 (Channel 1 secondary Compensation) pin is the secondary compensation input of the channel 1 step-down buck controller.

PIN DESCRIPTION

Pin Number	Pin Type	Pin Name	Pin Description
14	IN	VM_CH1	The VM_CH1 (Channel 1 Voltage Monitor) pin connects the channel 1 step-down controller output. Internally the VM_CH1 pin connects to an internal programmable resistor divider.
15	CAP	VDD_CAP	The VDD_CAP (VDD Capacitor) pin is an external capacitor input used to filter the internal supply.
16	PWR	VBATT	Power supply to part.
17	OUT	LSDRV_CH2	The LSDRV_CH2 (Channel 2 Low-side Driver) pin is the lower switching node of the channel 2 synchronous step-down buck controller. Attaches to the gate of n-channel MOSFET.
18	PWR	HVSUP2	Channel 2 High Voltage Supply for Channel 2 buck driver.
19	OUT	HSDRV_CH2	The HSDRV_CH2 (Channel 2 High-side Driver) pin is the upper switching node of the channel 2 synchronous step-down buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH2 and assertion of LSDRV_CH2 to prevent excessive current flow during switching.
20	IN	COMP2_CH2	The COMP2_CH2 (Channel 2 secondary Compensation) pin is the secondary compensation input of the channel 2 step-down buck controller.
21	IN	COMP1_CH2	The COMP1_CH2 (Channel 2 primary Compensation) pin is the primary compensation input of the channel 2 step-down buck controller. Each pin is internally connected to a programmable resistor divider.
22	IN	VM_CH2	The VM_CH2 (Channel 2 Voltage Monitor) pin connects the channel 6 step-down controller output. Internally the VM_CH2 pin connects to an internal programmable resistor divider.
23	OUT	LSDRV_CH3	The LSDRV_CH3 (Channel 3 Low-side Driver) pin is the lower switching node of the channel 3 synchronous step-down buck controller. Attaches to the gate of n-channel MOSFET.
24	PWR	HVSUP3	Channel 3 High Voltage Supply for Channel 3 buck driver.
25	OUT	HSDRV_CH3	The HSDRV_CH3 (Channel 3 High-side Driver) pin is the upper switching node of the channel 3 synchronous step-down buck controller. Attach to the gate of p-channel MOSFET. A delay exists between the assertion of HSDRV_CH3 and assertion of LSDRV_CH3 to prevent excessive current flow during switching.
26	IN	PWREN	The PWREN (Power Enable) pin is a programmable input used to enable (disable) selected supplies. This pin can also be programmed to latch and act as a debounced, manual push button input. Active high when level triggered, active low when used as a push- button input. When unused this pin should be tied to a solid logic level.
27	IN	COMP2_CH3	The COMP2_CH3 (Channel 3 secondary Compensation) pin is the secondary compensation input of the channel 3 step-down buck controller.
28	IN	COMP1_CH3	The COMP1_CH3 (Channel 3 primary Compensation) pin is the primary compensation input of the channel 3 step-down buck controller. Each pin is internally connected to a programmable resistor divider.

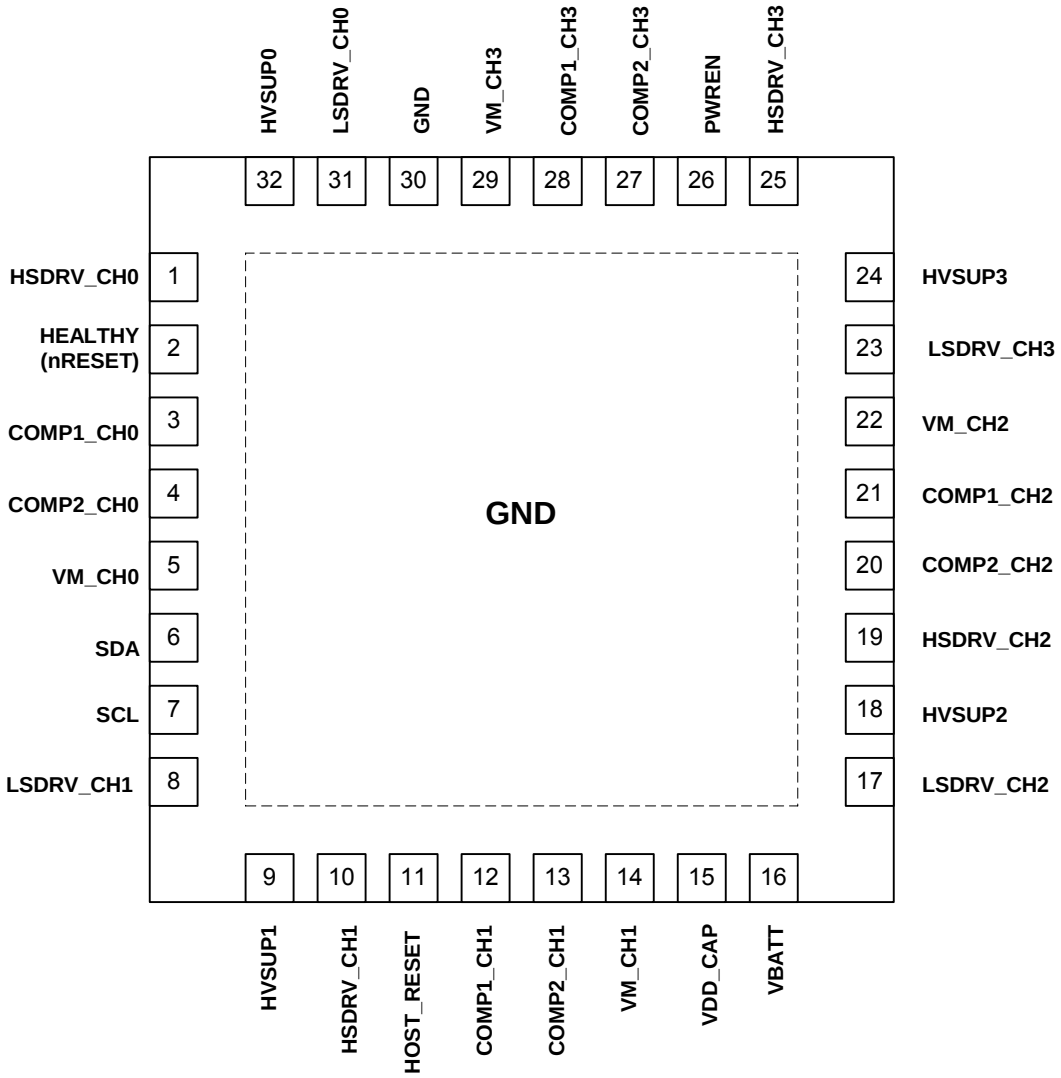
PIN DESCRIPTION

Pin Number	Pin Type	Pin Name	Pin Description
29	IN	VM_CH3	The VM_CH3 (Channel 3 Voltage Monitor) pin connects the channel 3 step-down controller output. Internally the VM_CH3 pin connects to an internal programmable resistor divider.
30	PWR	GND	Ground
31	OUT	LSDRV_CH0	The LSDRV_CH0 (Channel 0 Low-side Driver) pin is the lower switching node of the channel 0 synchronous step-down buck controller. Attach to the gate of n-channel MOSFET.
32	PWR	HVSUP0	Channel 0 High Voltage Supply used to power the channel 0 buck driver.
PAD	PWR	GND	Exposed metal (thermal) Pad on bottom of SMB113A/B and SMB117/A. The thermal pad of the QFN package must be connected to the PCB GND.

PACKAGE AND PIN DESCRIPTION

Top View

SMB113A/B/SMB117/A
5mm x 5mm QFN-32



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Terminal Voltage with Respect to GND:
VBATT Supply Voltage ..... -0.3V to +6.5V
HVSUP Supply Voltage ..... -0.3V to +6.5V
All Others ..... -0.3V to VBATT
Output Short Circuit Current 100mA
Reflow Solder Temperature (30 secs)..... +260°C
Junction Temperature..... +150°C
ESD Rating per JEDEC ..... +2000V
Latch-Up testing per JEDEC..... ±100mA

RECOMMENDED OPERATING CONDITIONS

Commercial Temperature Range..... 0°C to +70°C
Industrial Temperature Range ..... -40°C to +85°C
VBATT Supply Voltage ..... +2.7V to +6.0V
HVSUP Supply Voltage..... +2.7V to +6.0V
All Others.....GND to VBATT
Package Thermal Resistance (θ_{JA}), 32-Lead QFN (thermal pad connected to PCB)..... 37.2°C/W
Moisture Classification Level 3 (MSL 3) per J-STD-020

RELIABILITY CHARACTERISTICS

Data Retention ..... 100 Years
Endurance..... 100,000 Cycle
Temperature Range ..... -40°C to +85°C

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBATT	Input supply voltage	Input supply voltage (operational), Note 4	2.7		6.0	V
V_{HVSUP}	Buck driver supply voltage	Gate drive voltage	2.7		6.0	V
V_{UVLO}	Under-voltage lockout	VBATT rising		2.2	2.3	V
		VBATT falling	1.9	2.0		
V_{BATTSR}	Required input supply voltage slew-rate	Input supply voltage rising	0.037			V / msec
$I_{DD-MONITOR}$	Monitoring current	All voltage inputs monitored. No supplies switching, VBATT at 4.2V.		290	400	µA
$I_{DD-ACTIVE}$	Active current	Total current all channels enabled. No load. VBATT at 4.2V. Note 2.		1.2	2.0	mA
VDD_CAP	Internal supply, present on VDD_CAP pin	No load	2.4	2.5	2.6	V
Oscillator						
f_{OSC}	Oscillator frequency	SMB113B	875	1000	1125	kHz
		SMB113A	720	800	880	
		SMB117	360	400	440	
		SMB117A	212	250	288	
$O_{PP\ LT}$	Oscillator peak-to-peak			1		V
Δf_{SV}	Frequency stability for voltage			0.1		%/V
Δf_{ST}	Frequency stability for temperature	+25°C to +70°C, f_{OSC} = 800kHz		0.18		kHz/°C
		+25°C to +85°C, f_{OSC} = 800kHz		0.22		

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Error Amplifier						
A_{VOL}	Open loop voltage Gain	At DC		60		dB
BW	Frequency bandwidth	At A_{VOL} = 0 dB		30		MHz
I_{SOURCE}	Output source current	At 0.5V		20		µA
I_{SINK}	Output sink current	At 0.5V		800		µA
Output Block						
V_{OUT}	Voltage set point range. 100% Maximum Duty cycle	VBATT= 4.2V, I_{LOAD}=0 V_{OUT} = V_{BATT} x (duty cycle)	0.5		4.2	V
		VBATT= 6.0V, I_{LOAD}=0 V_{OUT} = V_{BATT} x (duty cycle)	0.5		6.0	
ΔV_{OUT}	Output accuracy, excluding external resistor divider[1]	Commercial temperature range	-1.5		+1.5	%
		Industrial temperature range	-2.0		+2.0	
R_{DRVH}	HSDRV ON resistance	Output high		2		Ω
		Output low		2		
R_{DRVL}	LSDRV ON resistance	Output high		2		
		Output low		2		
V_{COMP1}	Feedback voltage reference	COMP1 pin Programmable in 4mV steps		1.0		V
D.C.	100% Max Duty Cycle	High Duty Cycle		100		%
		Low Duty Cycle, Note 3			35	
	90% Max Duty Cycle	High Duty Cycle, Note 3	70			
		Low Duty Cycle		0		
Logic Levels						
V_{IH}	Input high voltage		0.7 x VDD_CAP		6.0	V
V_{IL}	Input low		0		0.3 x VDD_CAP	V
V_{OL}	Open drain outputs	I_{SINK} = 1mA	0		0.4	V

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Programmable Monitoring Thresholds						
V_{PUV1}	Programmable UV1 threshold	Programmable UV1 threshold voltage measured on VBATT pin in 150 mV increments	2.55		3.60	V
V_{PUV2}	Programmable UV2 threshold	Programmable UV2 threshold voltage measured on VBATT pin in 150 mV increments	2.55		3.60	V
ΔV_{PUV2}	UV2 accuracy			±2		%
ΔV_{PUV1}	UV1 accuracy			±2		%
P_{UVTH}	Programmable under-voltage threshold	Output voltage relative to nominal operating voltage. Note 3.	-3	-5	-7	%
			-8	-10	-12	
			-12	-15	-18	
			-16	-20	-24	
P_{OVTH}	Programmable over-voltage threshold	Output voltage relative to nominal operating voltage. Note 3.	+3	+5	+7	%
			+8	+10	+12	
			+12	+15	+18	
			+16	+20	+24	

Note 1: Voltage accuracies are only guaranteed for factory-programmed settings. Changing the output voltage from that reflected in the customer specific CSIR code might result in inaccuracies exceeding those specified above by 1%.

Note 2: For more accurate active current levels under several load conditions, Summit's proprietary design software can be used. Contact the factory for more information.

Note 3: Guaranteed by Design and Characterization – not 100% tested in Production.

Note 4: Contact the factory for designs that require an input voltage lower than 4.5V.

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.) Note 5

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{PPTO}	Programmable power-On sequence timeout period.	Programmable power-on sequence position to sequence position delay.		1.5		ms
				12.5		
				25		
				50		
t_{DPOFF}	Programmable power-off sequence timeout period.	Programmable power-off sequence position to sequence position delay.		1.5		ms
				12.5		
				25		
				50		
t_{PST}	Programmable sequence termination period	Time between active enable in which corresponding outputs must exceed there programmed under voltage threshold. If exceeded, a force shutdown will be initiated.		OFF		ms
				50		
				100		
				200		
t_{PGF}	Programmable glitch filter	Period for which fault must persist before fault triggered actions are taken.		0		µs
				8		
t_{RESET}	Reset timeout period	Applicable when HEALTHY pin is used as an nRESET output pin. Programmable time following assertion of last supply before nRESET pin is released high.		25		ms
				50		
				100		
				200		
SR_{REF}	Programmable slew rate reference	Adjustable slew rate factor proportional to output slew rate.		400		V/s
				200		
				100		
				67		
				50		
				33		
				25		
				20		
Channels 0 to 3						
t_{RL}	LS Driver output rise time	C_G=100pF, V_{BATT}=4.2V		4.2		ns
t_{FL}	LS Driver output fall time	C_G=100pF, V_{BATT}=4.2V		4.2		ns
t_{RL}	HS Driver output rise time	C_G=100pF, V_{BATT}=4.2V		2.9		ns
t_{FL}	HS Driver output fall time	C_G=100pF, V_{BATT}=4.2V		2.9		ns
t_{DT}	Driver non-overlap delay	High to low transition on HSDRV		30		ns
		Low to high transition on buck HSDRV		60		

Note 5: Timing specifications are 20% shorter for the SMB113B device and 60% longer for SMB117A.

I²C-2 WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100 kHz

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	100kHz			
			Min	Typ	Max	Units
f_{SCL}	SCL clock frequency		0		100	kHz
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period		4.0			µs
t_{BUF}	Bus free time	Before new transmission – Note 6	4.7			µs
$t_{SU:STA}$	Start condition setup time		4.7			µs
$t_{HD:STA}$	Start condition hold time		4.0			µs
$t_{SU:STO}$	Stop condition setup time		4.7			µs
t_{AA}	Clock edge to data valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data output hold time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA rise time	Note 6			1000	ns
t_F	SCL and SDA fall time	Note 6			300	ns
$t_{SU:DAT}$	Data in setup time		250			ns
$t_{HD:DAT}$	Data in hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		136		ns
t_{WR_CONFIG}	Write cycle time config	Configuration registers			10	ms
t_{WR_EE}	Write cycle time EE	Memory array			5	ms

Note 6: Guaranteed by Design.

TIMING DIAGRAMS

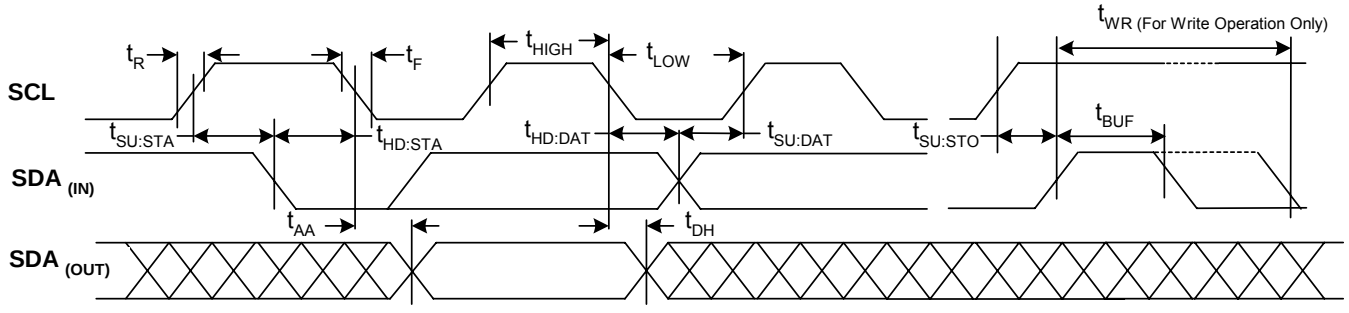
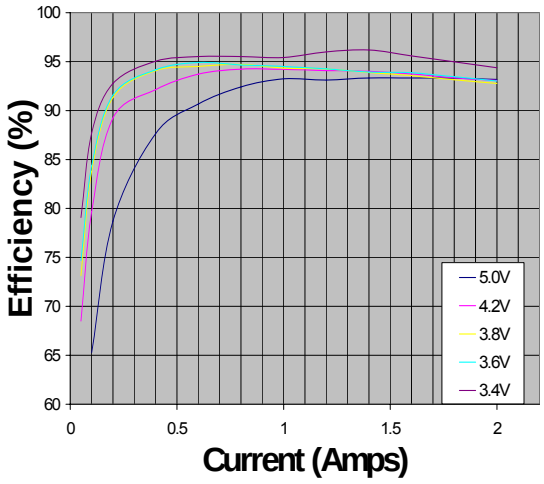


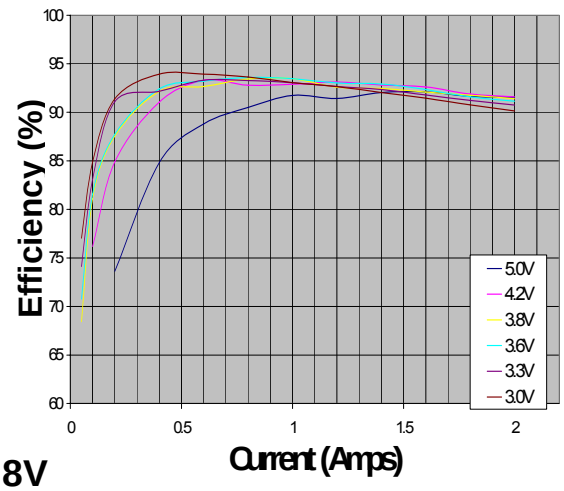
Figure 4 – I²C timing diagram

SMB113A EFFICIENCY GRAPHS

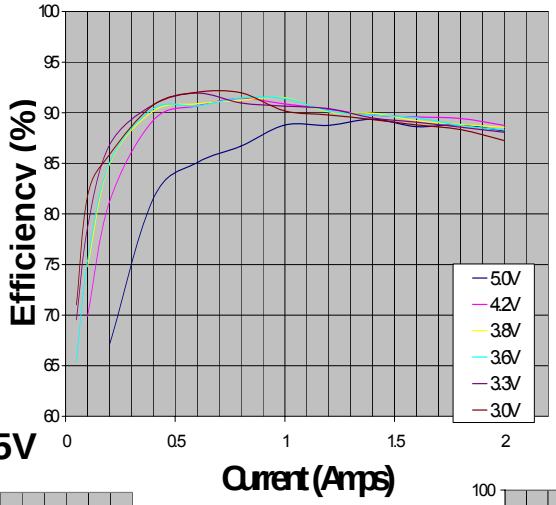
Efficiency at 3.3V



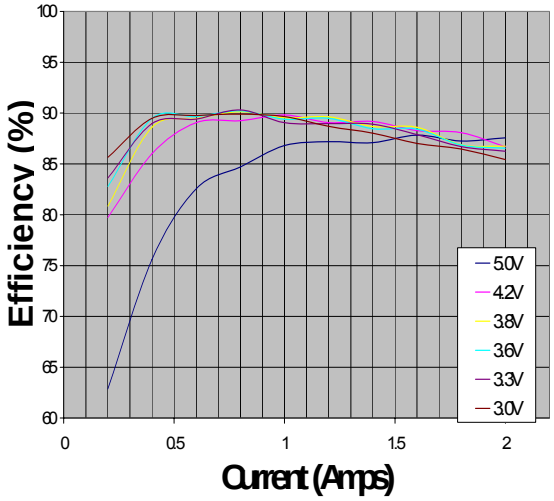
Efficiency at 2.5V



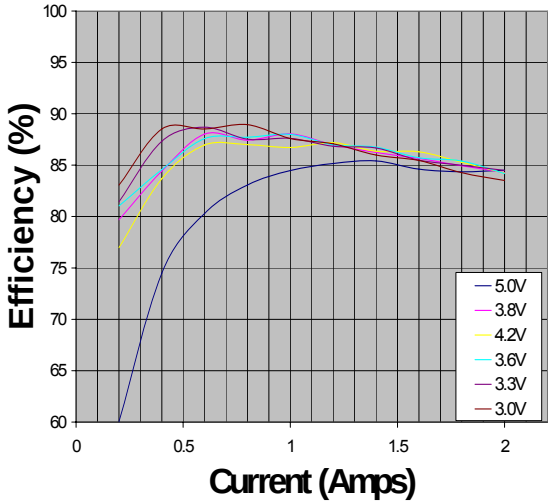
Efficiency at 1.8V



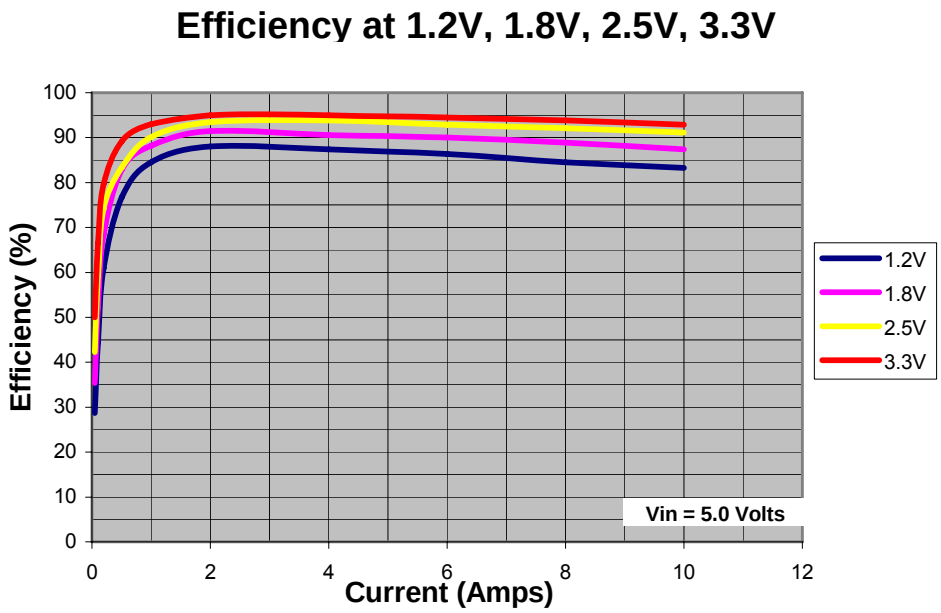
Efficiency at 1.5V



Efficiency at 1.2V



SMB117 EFFICIENCY GRAPHS



APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

There are five supply input pins on the SMB113A/B and SMB117/A: four HVSUP pins and the VBATT pin. Each supply must be powered from an input voltage between 2.7-6.0 volts.

The HVSUP1 though HVSUP4 are used to power the HSDRV (PMOS driver) and LSDRV (NMOS driver) outputs. The rail-to-rail swing on the HSDRV and LSDRV pins is equal to the associated HVSUP supply voltage.

The VBATT pin is internally regulated to 2.5V. This 2.5V supply is then filtered on the VDD_CAP pin and used to power all internal circuitry. The VBATT pin is monitored by an Under-Voltage Lockout (UVLO) circuit, which prevents the device from turning on when the voltage at this node is less than the UVLO threshold.

OUTPUT VOLTAGE

All output voltages on the SMB113A/B and SMB117/A can be set via the non-volatile configuration registers.

Each of the four step-down output voltages on the SMB113A/B and SMB117/A can be adjusted for 100% duty cycle or 0% duty cycle operation.

When 100% duty cycle mode is selected, the output voltage can be set up to the input voltage on the device, while the minimum output voltage is limited to the min duty cycle specification in the DC operating characteristics section.

When the 0% duty cycle mode is selected, the maximum duty cycle is limited to the max duty cycle specification in the DC operating characteristics section.

POWER-ON/OFF CONTROL

Sequencing can be initiated: automatically, by a volatile I^2C **Power on** command, or by asserting the PWREN pin. When the PWREN pin is programmed to initiate sequencing, it can be level or edge triggered. The PWREN input has a programmable de-bounce time of 100, 50, or 25ms. The de-bounce time can also be disabled.

When configured as a push-button enable, PWREN must be asserted longer than the de-bounce time before sequencing can commence, and pulled low for the same period to disable the channels.

ENABLE

Each output can be enabled and disable by an enable signal. The enable signal is can be provided from either the PWREN pin or by the contents of the enable register.

When enabling a channel from the enable register, the register contents default state must be set so that the output will be enabled or disabled following a POR (power on reset). The default state is programmable.

CASCADE SEQUENCING

Each channel on the SMB113A/B and SMB117/A may be placed in any one of 4 unique sequence positions, as assigned by the configurable non-volatile register contents. The SMB113A/B and SMB117/A navigate between each sequence position using a feedback-based cascade-sequencing circuit. Cascade sequencing is the process in which each channel is continually compared against a programmable reference voltage until the voltage on the monitored channel exceeds the reference voltage, at which point an internal sequence position counter is incremented and the next sequence position is entered. In the event that a channels enable input is not asserted when the channel is to be sequenced on, that sequence position will be skipped and the channel in the next sequence position will be enabled.

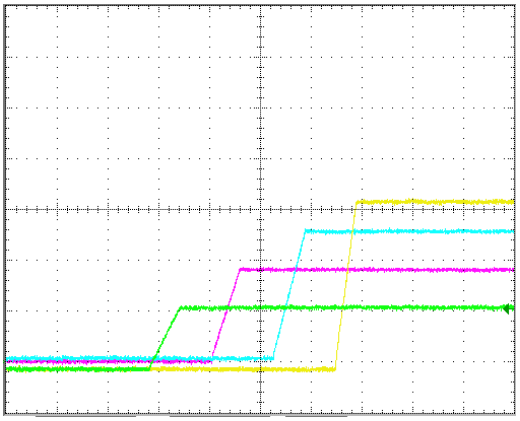


Figure 5 – Power on sequencing waveforms.
Time = 4ms/devision, Scale = 1V/devision
Ch 1 = 3.3V output (Yellow trace)
Ch 2 = 2.5V output (Blue trace)
Ch 3 = 1.8V output (Purple trace)
Ch 4 = 1.2V output (Green trace)

POWER ON/OFF DELAY

There is a programmable delay between when channels in subsequent sequence positions are enabled. The delay is programmable at 50, 25, 12.5 and 1.5ms intervals. This delay is programmable for each of the four sequence positions.

APPLICATIONS INFORMATION (CONTINUED)

MANUAL MODE

The SMB113A/B and SMB117/A provide a manual power-on mode in which each channel may be enabled individually irrespective of the state of other channels. In this mode, the enable signal has complete control over the channel, and all sequencing is ignored. In Manual mode, channels will not be disabled in the event of a UV/OV fault on any output or the VBATT pin.

FORCE-SHUTDOWN

When a battery fault occurs, a UV/OV is detected on any output, or an I^2C force-shutdown command is issued, all channels will be immediately disabled, ignoring sequence positions or power off delay times.

SEQUENCE TERMINATION TIMER

At the beginning of each sequence position, an internal programmable timer will begin to time out. When this timer has expired, the SMB113A/B and SMB117/A will automatically perform a force-shutdown operation. This timer is user programmable with a programmable sequence termination period (t_{PST}) of 50, 100, 200 ms; this function can also be disabled.

POWER OFF SEQUENCING

The SMB113A/B and SMB117/A have a power-off sequencing operation. During a power off operation, the supplies will be powered off in the reverse order they where powered on in. During the power off sequencing, all enables are ignored.

When a power-off command is issued the SMB113A/B and SMB117/A will set the sequence position counter to the last sequence position and disable that channel without soft-start control; once off, the power off delay for the channel(s) in the next to last sequence position will begin to timeout, after which that channel(s) will be disabled. This process will continue until all channels have been disabled and are off. The programmable

If a channel fails to turn off within the sequence termination period, the sequence termination timer will initiate a force shutdown, if enabled.

INPUT AND OUTPUT MONITORING

Both products monitor all outputs for under-voltage (UV) and over-voltage (OV) faults. The monitored levels are user programmable, and may be set at 5, 10, 15, and 20 percent of the nominal output voltage.

The VBATT pin is monitored for two user programmable UV settings. The VBATT UV settings are programmable from 2.55V to 3.45V in 150mV increments. Once the UV/OV voltage set points have been violated, the SMB113A/B and SMB117/A can be programmed to respond in one of three ways, perform: a power-off operation, a force-shutdown operation and-or it can trigger the nRESET/HEALTHY pin.

SOFT START

The SMB113A/B and SMB117/A provide a programmable soft-start function for all PWM outputs. The soft-start control limits the slew rate that each output is allowed to ramp up without the need for an external capacitor. The soft start slew rate is proportional to the product of the output voltage and a slew rate reference. This global reference is programmable and may be set to 400, 200, 100, 67, 50, 33, 25, and 20 Volts per second. The slew rate control can also be disabled on any channel not requiring the feature.

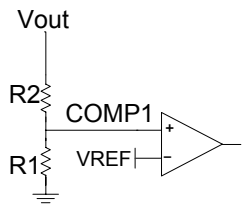
DYNAMIC VOLTAGE MANAGEMENT

The SMB113A/B/117/A have two additional voltage settings, dynamic voltage control high and low settings. Together with the nominal voltage setting, three pre-determined voltage levels can be used. The three voltage levels are ideal for situations where a core voltage needs to be reduced for power conservation.

The dynamic voltage control high and low settings have the same voltage range as the controllers' nominal output voltage. These settings are stored in the non-volatile configuration registers and can be set by a write to volatile configuration registers. The dynamic voltage control command registers contain two bits for each channel that adjust the output voltages to the high, low or nominal set point after a volatile I2C write command.

A seven level dynamic voltage control option is available for channel 3. When enabled, seven level dynamic voltage control allows channel 3 to be dynamically modified to one of seven pre-determined voltage levels. This transition is made by means of a volatile I^2C write command.

When all channels are at their voltage setting, a bit is set in the dynamic voltage control status registers.



Soft-Start Slew Rate=SRref* (1 + R2/R1)
Vout= Vref* (1 + R2/R1)

Figure 6 – The output voltage is set by the voltage divider. The VREF voltage is programmable from 0 to 1.0 volt in 4mV increments via the I^2C interface

APPLICATIONS INFORMATION

High Voltage Operation:

While the SMB113A has a max input voltage of 6.0V the controller can operate to0 much higher voltages by using the circuit depicted below. By inserting a capacitor, C1, in series with the HSDRV gate signal the HSDRV pin is isolated from the 12V supply, and the AC coupling capacitor acts as a level translator transferring the 0-5V signal from the HSDRV pin to a 12V to 7V (12V-5V = 7V) signal at the gate of the PFET. When the gate stops switching the capacitor becomes an open circuit and the gate will be pulled high by R1 turning off the output. The schottky diode and the pull-up resistor are used for DC restoration and as a pull-up respectively.

Since the converter runs directly from the input supply (12V in this instance) the efficiency is consistent with that of a synchronous converter. Typical efficiency curves are shown below.

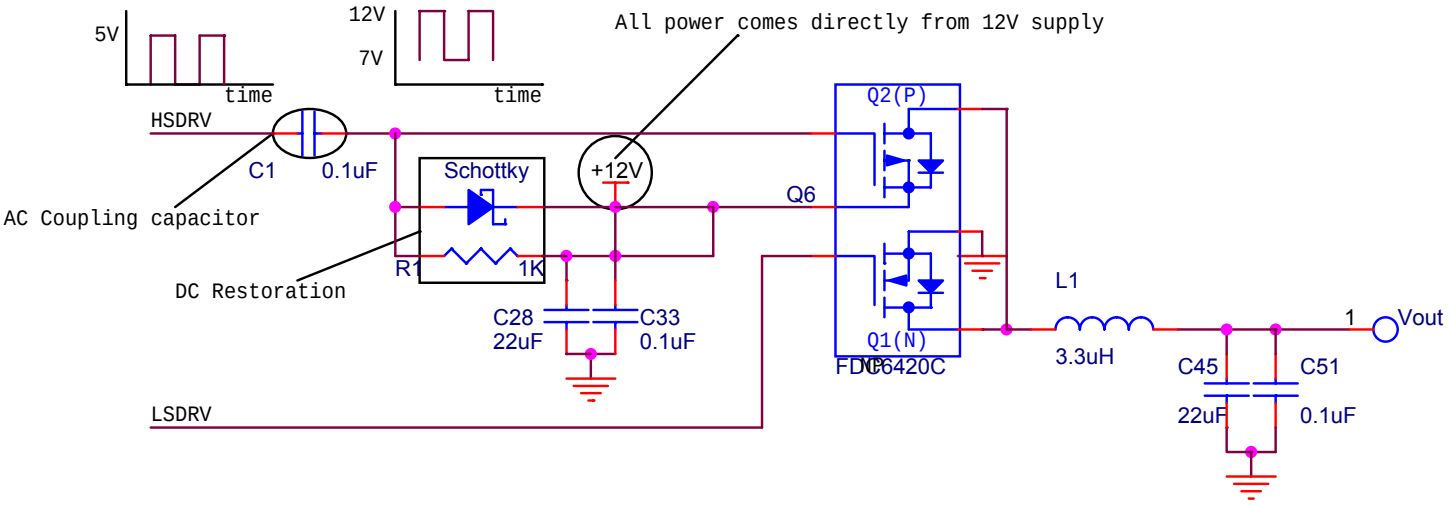


Figure 7 – High-voltage operation

APPLICATIONS INFORMATION (CONTINUED)

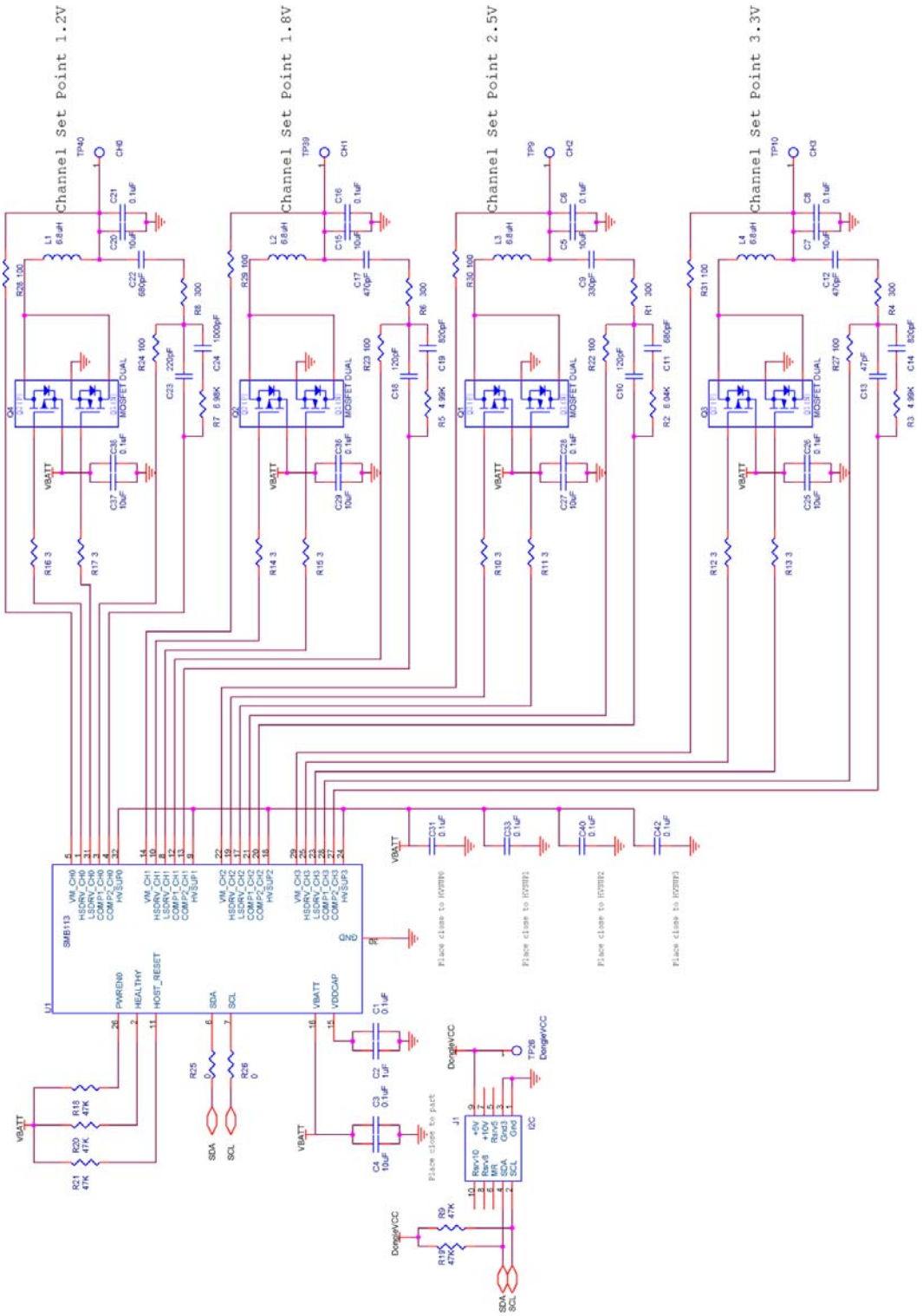


Figure 8 – SMB113A applications schematic.

APPLICATIONS INFORMATION (CONTINUED)

Item	Description	Vendor / Part Number	Qty	Ref. Des.
Resistors				
1	300Ω, 1/16W, 1%, 0603, SMD	Vishay CRCW06033000F	4	R1, R4, R6, R8
2	6.04KΩ, 1/16W, 1%, 0603, SMD	Vishay CRCW06036041F	1	R2
3	4.99KΩ, 1/16W, 1%, 0603, SMD	Vishay CRCW06034991F	2	R3, R5
4	6.98KΩ, 1/16W, 1%, 0603, SMD	Vishay CRCW06036981F	1	R7
5	47Ω, 1/16W, 1%, 0603, SMD	Vishay CRCW06034702F	5	R9, R18, R19, R20, R21
6	3Ω, 1/16W, 1%, 0603, SMD	Vishay CRCW06033R01F	8	R10, R11, R12, R13, R14, R15, R16, R17
7	10KΩ, 1/16W, 1%, 0603, SMD	Vishay CRCW06031002F	1	R20
8	300Ω, 1/16W, 1%, 0603, SMD	Vishay CRCW06031000F	4	R22, R23, R24, R27
Capacitors				
9	0.1uF, 16V, ceramic, X7R, 0603, SMD	Kemet C0603C104K4RACTU	15	C1, C3, C6, C8, C16, C21, C26, C28, C31, C33, C34, C36, C38, C40, C42
10	1uF, 10V, ceramic, Y5V, 0603, SMD	Panasonic ECJ-1VF1A105Z	2	C2, C35
11	10uF, 6.3V, ceramic, X5R, 0805, SMD	Kemet C0805C106K9PACTU	9	C4, C25, C27, C29, C37
12	10uF, 25V, ceramic, X7R, 1210, SMD	TDK C3225X7R1E106M	4	C5, C7, C15, C20,
13	330pF, 50V, ceramic, C0G, 0603, SMD	Murata GRM1885C2A331JA01D	1	C9
14	120pF, 50V, ceramic, C0G, 0603, SMD	Vishay VJ0603A121KXAA	2	C10, C18
	680pF, 100V, ceramic, X7R, 0603, SMD	Murata GRM188R72A681KA01D	2	C11, C22
15	47pF, 50V, ceramic, NP0, 0603, SMD	Panasonic ECJ-1VC1H470J	1	C13
16	470pF, 50V, ceramic, X7R, 0603, SMD	Kemet C0603C471K5RACTU	2	C17, C12
17	820pF, 50V, ceramic, C0G, 0603, SMD	Murata GRM1885C2A331JA01D	2	C14, C19
18	220pF, 50V, ceramic, C0G, 0603, SMD	Murata GRM188R72A221KA01D	1	C23
19	1000pF, 50V, ceramic, C0G, 0603, SMD	Vishay VJ0603A102KXAA	1	C24
Semiconductors				
20	MOSFET, Complementary	Fairchild, FDC6420C	4	Q1-Q4
21	SMB113ANC	Summit Microelectronics	1	U1
Magnetics				
22	Inductor, 6.8uH, 2.75A, SMD, Shielded	Sumida CDR7D28MNNP-6R8NC	4	L1-4

APPLICATIONS INFORMATION (CONTINUED)

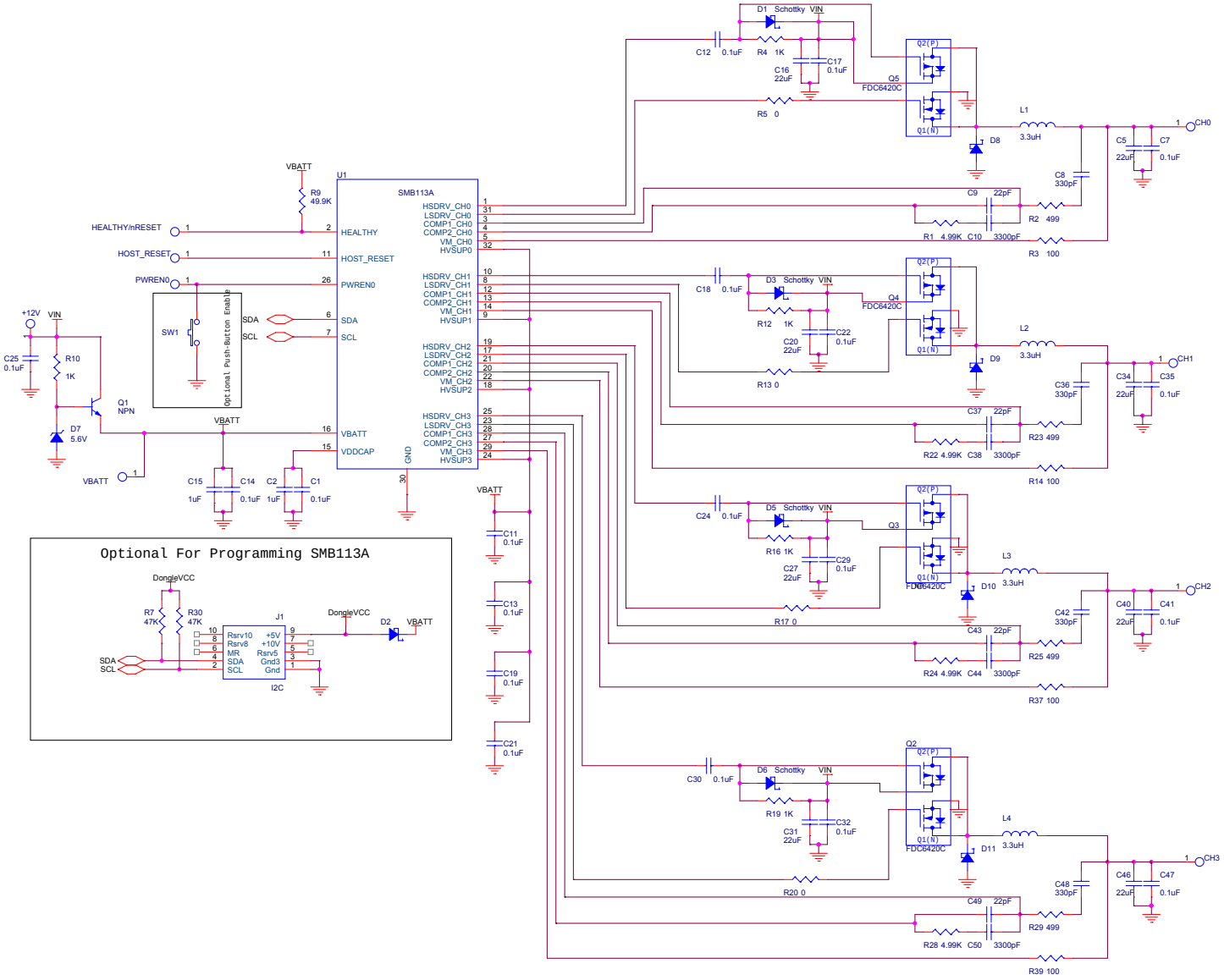


Figure 9 – Applications schematic showing SMB113A operation from a +12V input supply.

APPLICATIONS INFORMATION (CONTINUED)

Item	Description-	Vendor / Part Number	Qty	Ref. Des.
	Capacitors			
1	0.1uF, 50V, ceramic, X7R, 0603, SMD	Murata GRM188R71H104KA93D	19	C1, C3, C7, C11, C13, C12, C14, C17, C18, C19, C21, C22, C24, C25, C29, C30, C32, C35, C41, C47
2	1uF, 25V, ceramic, X5R, 0805, SMD	Murata GRM216R61E105KA12	2	C2, C15
3	22uF, 16V, ceramic, X5R, 1210, SMD	Murata GRM32ER61C226ME20L	9	C5, C16, C20, C27, C31, C34, C40, C46
4	330pF, 50V, ceramic, NP0, 0603, SMD	Panasonic ECJ-1VC1H331J	4	C8, C36, C42, C48
5	22pF, 50V, ceramic, NP0, 0603, SMD	Murata GRM1885C1H470JA01D	4	C9, C37, C43, C49
6	3300pF, 100V, ceramic, X7R, 0603, SMD	Murata GRM188R71H332KA01D	4	C10, C38, C44, C50
	Resistors			
7	499Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06034990F	4	R2, R23, R25, R29
8	100Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06031000F	4	R3, R14, R37, R39
9	1KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06031001F	5	R4, R10, R12, R16, R19
10	0Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06030R00F	4	R5, R13, R17, R20
11	49.9KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06034992F	4	R6, R7, R8, R30
12	2KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06032001F	1	R9
13	4.99KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06034991F	4	R1, R22, R24, R28
	Semiconductors			
14	Diode Schottky, 20V, 200mA, SS-mini	Panasonic MA2SD2400L	4	D1, D3, D5, D6
15	Diode, Schottky, 40V, 500mA SOD-123	Diodes Inc. B0540W-7	5	D2, D8, D9, D10, D11
16	LED, Red, 0805, SMD	Lumex SML-LXT0805SRW-TR	2	D4
17	Zener Diode, 5.6V, 500mW, SOD-123	ON Semi MMSZ5V6T1G	1	D7
18	NPN, 40V, 1A, SOT-89	Zetex FCX491A	1	Q1
19	MOSFET, Complementary, 20V, SSOT-6	Analog Power AM3520C	4	Q2, Q3, Q4, Q5
20	SMB113A	Summit Microelectronics	1	U1
	Magnetics			
21	Inductor 3.3uH	TDK HCP0703-3R3-R	4	L1, L2, L3, L4

APPLICATIONS INFORMATION (CONTINUED)

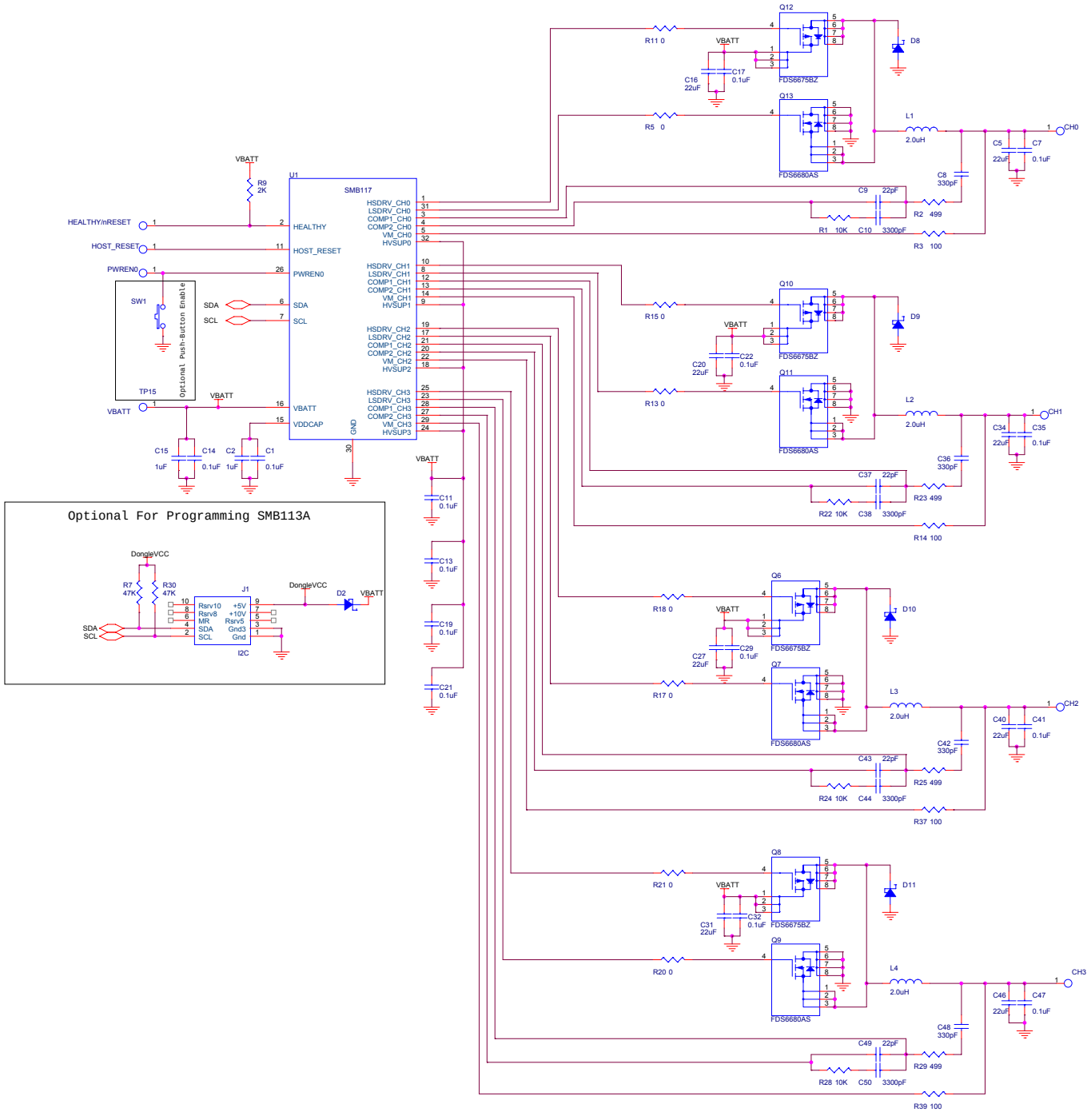


Figure 10 – Applications schematic showing SMB117 operation from a +5V input supply with 10A output current capability.

APPLICATIONS INFORMATION (CONTINUED)

Item	Description-	Vendor / Part Number	Qty	Ref. Des.
Capacitors				
1	0.1uF, 50V, ceramic, X7R, 0603, SMD	Murata GRM188R71H104KA93D	19	C1, C3, C7, C11, C13, C12, C14, C17, C18, C19, C21, C22, C24, C25, C29, C30, C32, C35, C41, C47
2	1uF, 25V, ceramic, X5R, 0805, SMD	Murata GRM216R61E105KA12	2	C2, C15
3	22uF, 16V, ceramic, X5R, 1210, SMD	Murata GRM32ER61C226ME20L	9	C5, C16, C20, C27, C31, C34, C40, C46
4	330pF, 50V, ceramic, NP0, 0603, SMD	Panasonic ECJ-1VC1H331J	4	C8, C36, C42, C48
5	22pF, 50V, ceramic, NP0, 0603, SMD	Murata GRM1885C1H470JA01D	4	C9, C37, C43, C49
6	3300pF, 100V, ceramic, X7R, 0603, SMD	Murata GRM188R71H332KA01D	2	C10, C38, C44, C50
Resistors				
7	499Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06034990F	4	R2, R23, R25, R29
8	100Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06031000F	4	R3, R14, R37, R39
9	1KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06031001F	5	R4, R10, R12, R16, R19
10	0Ω, 1/10W, 1%, 0603, SMD	Vishay CRCW06030R00F	4	R5, R13, R17, R20
11	49.9KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06034992F	4	R6, R7, R8, R30
12	2KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06032001F	1	R9
13	10KΩ, 1/10W, 1%, 0603, SMD	Vishay CRCW06031002F	4	R1, R22, R24, R28
Semiconductors				
14	Diode, Schottky, 40V, 500mA SOD-123	Diodes Inc. B0540W-7	5	D2, D12, D13, D14, D15
15	LED, Red, 0805, SMD	Lumex SML-LXT0805SRW-TR	2	D4
16	MOSFET, NFET, 20V, SOT-8	Fairchild FDS6680AS		Q7, Q9, Q11, Q13
17	MOSFET, PFET, 20V, SOT-8	Fairchild FDS6675BZ	4	Q6, Q8, Q10, Q12
18	SMB117	Summit Microelectronics	1	U1
Magnetics				
19	Inductor 2.0uH	Wurth 744314200	4	L1, L2, L3, L4

APPLICATIONS INFORMATION (CONTINUED)

COMPONENT SELECTION

Buck Outputs:

Inductor:

The starting point design of any and DC/DC converter is the selection of the appropriate inductor for the application. The optimal inductor value will set the inductor current at 30% of the maximum expected load current. The inductors current for a Buck converter is as follows:

Buck: Equation 1: $$L = \frac{Vo(V_{IN} - Vo)}{Vin * 0.3 * I_{MAX} * f}$$

Where Vo is the output voltage, VIN is the input voltage, f is the frequency, and I_{MAX} is the max load current.

For example: For a 1.2V output and a 3.6V input with a 500mA max load, and a 1MHz switching frequency the optimal inductor value is:

$$L = \frac{1.2(3.6 - 1.2)}{3.6 * 0.3 * 0.5 \ * 1E6} = 5.3uH$$

Choosing the nearest standard inductor value we select a 5.6uH inductor. It is important that the inductor has a saturation current level greater than 1.2 times the max load current.

Other parameters of interest when selecting an inductor are the DCR (DC winding resistance). This has a direct impact on the efficiency of the converter. In general, the smaller the size of the inductor is the larger the resistance. As the DCR goes up the power loss increases according to the I^2R relation. As a result choosing a correct inductor is often a trade off between size and efficiency.

Input Capacitor

Each converter should have a high value low impedance input (or bulk) capacitor to act as a current reservoir for the converter stage. This capacitor should be either a X5R or X7R MLCC (multi-layer-ceramic capacitor). The value of this capacitor is normally chosen to reflect the ratio of the input and output voltage with respect to the output capacitor. Typical values range from 2.2uF to 10uF.

For Buck converters, the input capacitor supplies square wave current to the inductor and thus it is critical to place this capacitor as close to the PFET as possible in order to minimize trace inductance that would otherwise limit the rate of change of the current.

Output capacitor

Each converter should have a high value low impedance output capacitor to act as a current reservoir for current transients and to. This capacitor should be either a X5R or X7R MLCC.

For a Buck converter, the value of this capacitance is determined by the maximum expected transient current. Since the converter has a finite response time, during a load transient the current is provided by the output capacitor. Since the voltage across the capacitor drops proportionally to the capacitance, a higher output capacitor reduces the voltage drop until the feedback loop can react to increase the voltage to equilibrium.

The voltage drop can be calculated according to:

Equation 2: $$V = \frac{I * T}{C}$$

Where I is the load or transient current, T is the time the output capacitor is supporting the output and C is the output capacitance. Typical values range from 10uF to 44uF.

Other important capacitor parameters include the Equivalent Series Resistance (E.S.R) of the capacitor. The ESR in conjunction with the ripple current determines the ripple voltage on the output, for typical values of MLCC the ESR ranges from 2-10mΩ. In addition, carful attention must be paid to the voltage rating of the capacitor the voltage rating of a capacitor must never be exceeded. In addition, the DC bias voltage rating can reduce the measured capacitance by as much as 50% when the voltage is at half of the max rating, make sure to look at the DC bias de-rating curves when selecting a capacitor.

MOSFETS

When selecting the appropriate FET to use attention must be paid to the gate to source rating, input capacitance, and maximum power dissipation.

Most FETs are specified by an on resistance (RDS_{ON}) for a given gate to source voltage (V_{GS}). It is essential to ensure that the FETs used will always have a V_{GS} voltage grater then the minimum value shown on the datasheet. It is worth noting that the specified V_{GS} voltage must not be confused with the threshold voltage of the FET.

APPLICATIONS INFORMATION (CONTINUED)

The input capacitance must be chosen such that the rise and fall times specified in the datasheet do not exceed ~5% of the switching period.

To ensure the maximum load current will not exceed the power rating of the FET, the power dissipation of each FET must be determined. It is important to look at each FET individually and then add the power dissipation of complementary FETs after the power dissipation over one cycle has been determined. The Power dissipation can be approximated as follows:

Equation 3: $$P \sim R_{DSON} * I_L{}^2 * T_{ON}$$

Where T_{ON} is the on time of the primary switch. T_{ON} can be calculated as follows:

Equations 4, 5:

$$Buck - NFET : (1 - \frac{V_O}{V_{IN}}) * T$$

$$Buck - PFET : \frac{V_O}{V_{IN}} * T$$

Compensation:

Summit provides a design tool to called Summit Power Designer" that will automatically calculate the compensation values for a design or allow the system to be customized for a particular application. The power designer software can be found at http://www.summitmicro.com/prod_select/xls/SummitPowerDesigner_Install.zip.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 parallel port programming system or the I²C2USB (SMX3201) USB programming system for device prototype development. The SMX3200(1) system consist of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 and SMX3201 are available from the website (**http://www.summitmicro.com**).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application; while the SMX3201 interfaces directly to the PC's USB port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMB113A/B or SMB117/A via the programming Dongle and cable. An example of the connection interface is shown in Figure 11.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

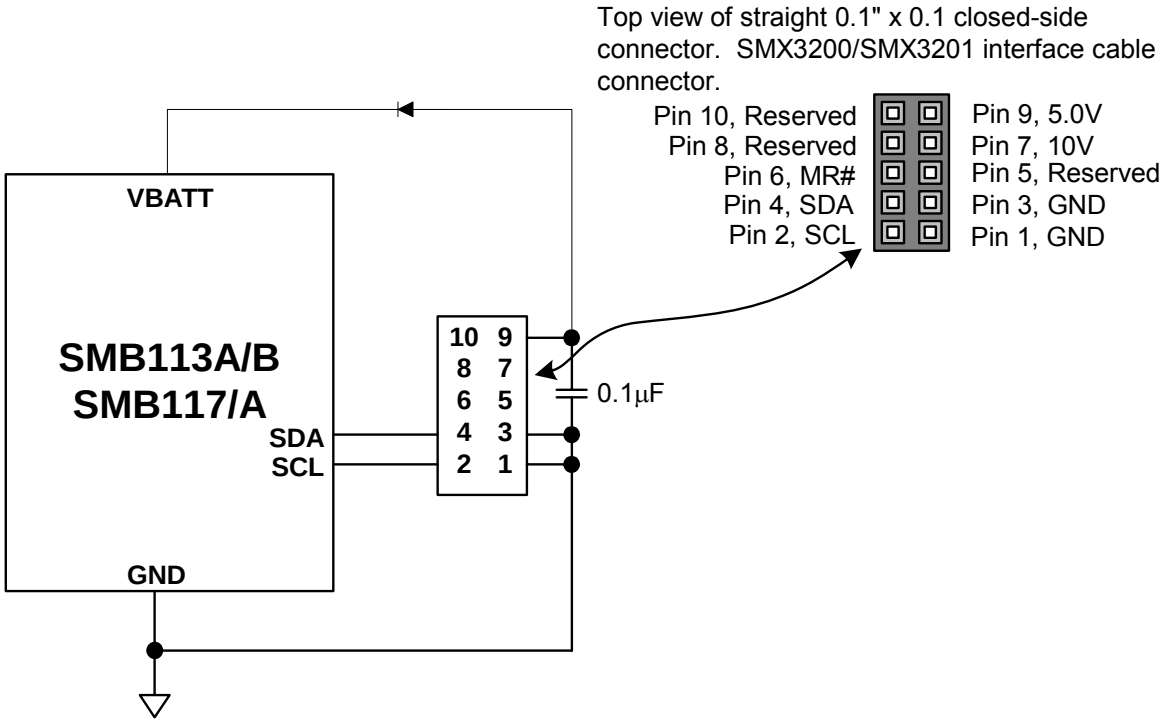


Figure 11 – SMX3200/SMX3201 Programmer I²C serial bus connections to program the SMB113A/B or SMB117/A.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMB113A/B.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. The slave address can be can be programmed to any seven bit number 0000000_{BIN} through 1111111_{BIN}.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 12and 13 A Start condition followed by the slave address byte is provided by the host; the SMB113A/B and SMB117/A respond with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB113A/B and SMB117/A respond with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page.

After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the non-volatile configuration registers and memory registers as well as the volatile command and status registers must be set before data can be read from the SMB113A/B or the SMB117/A. This is accomplished by issuing a dummy write command, which is a write command that is not followed by a Stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figure 14for an illustration of the read sequence.

CONFIGURATION REGISTERS

The configuration registers are grouped with the general-purpose memory.

GENERAL-PURPOSE MEMORY

The 96-byte general-purpose memory block is segmented into two continuous independently lockable blocks. The first 48-byte memory block begins at register address pointer $A0_{HEX}$ and the second memory block begins at the register address pointer $C0_{HEX}$; see Table 1. Each memory block can be locked individually by writing to a dedicated register in the configuration memory space.

I²C PROGRAMMING INFORMATION (CONTINUED)

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMB113A/B/117/A graphical user interface (GUI) is highly recommended. The software is available from the Summit website (http://www.summitmicro.com). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMB113A/B and SMB117/A. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I^2C bus protocol. See figure 11 and the SMX3200 Data Sheet.

Slave Address	Register Type
0000000_{BIN} to 1111111_{BIN}	Configuration Registers are located in 00_{HEX} thru $9F_{HEX}$
	General-Purpose Memory Block 0 is located in $A0_{HEX}$ thru BF_{HEX}
	General-Purpose Memory Block 1 is located in $C0_{HEX}$ thru FF_{HEX}

Table 1 – Possible address bytes used by the SMB113A/B and the SMB117/A.

I²C PROGRAMMING INFORMATION (CONTINUED)

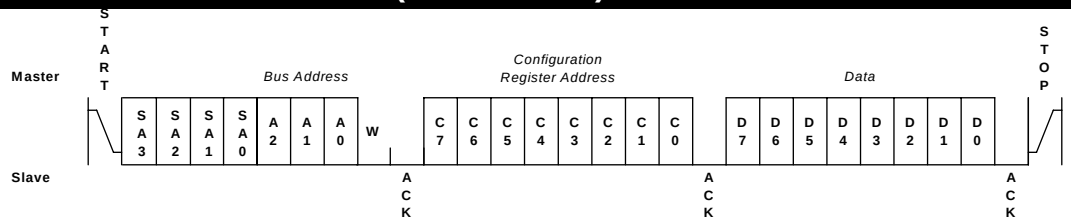


Figure 12 – Register Byte Write

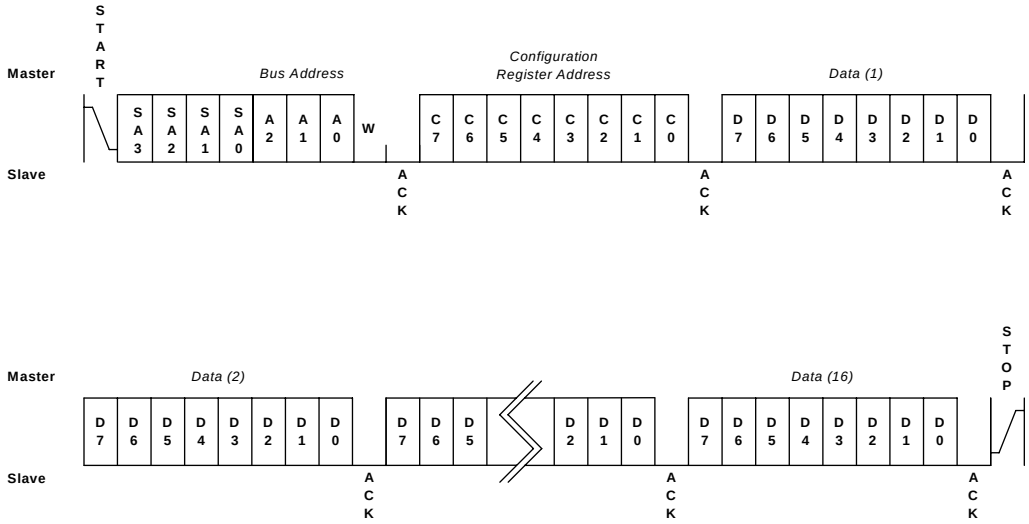


Figure 13 – Register Page Write

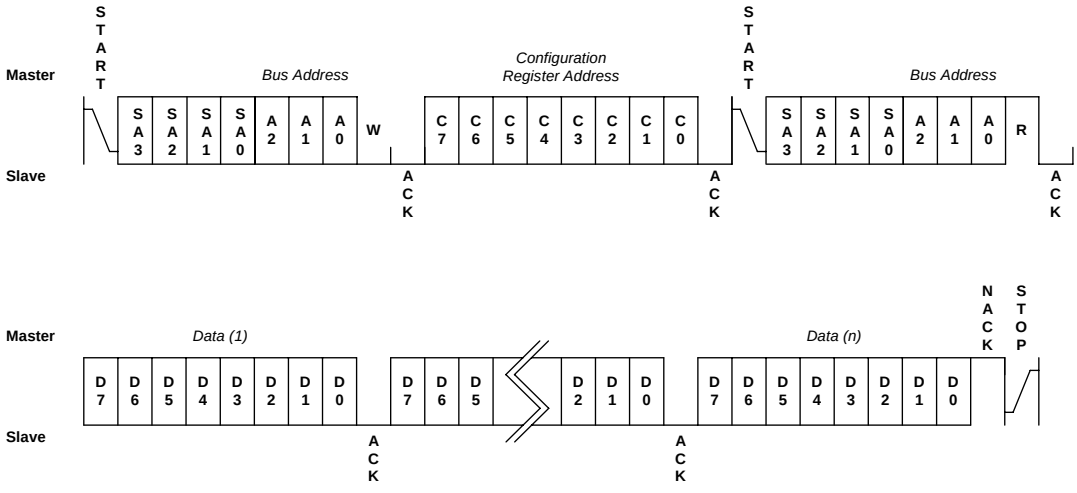
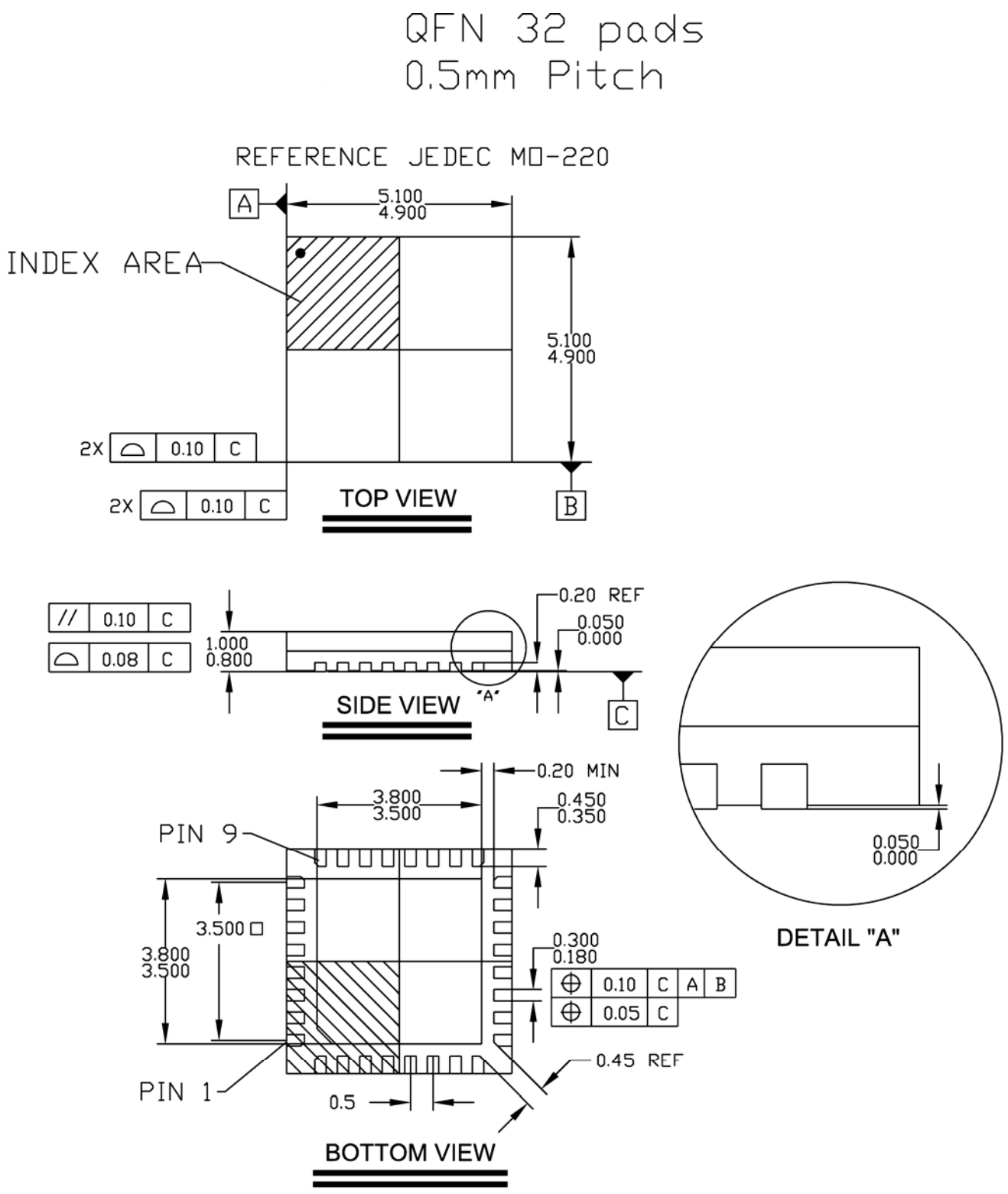
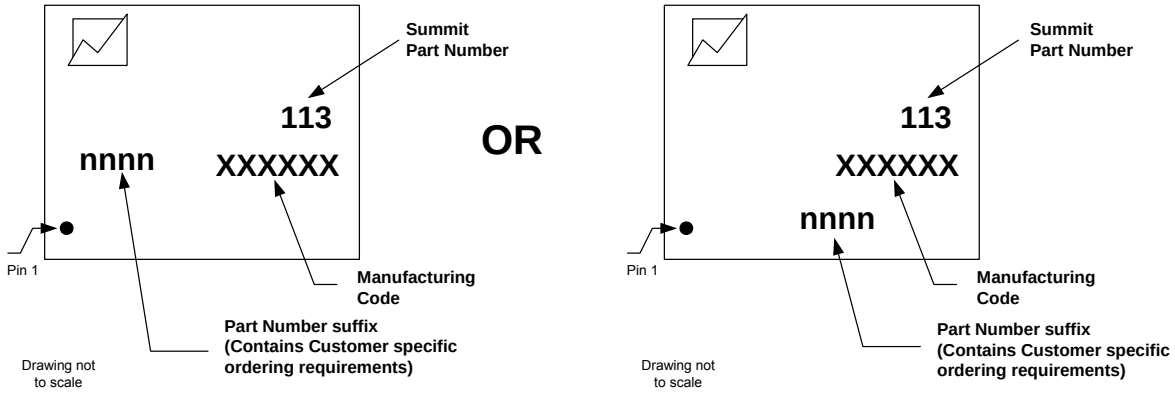


Figure 14 – Register Read

PACKAGE


QFN 32 pads
0.5mm Pitch
REFERENCE JEDEC MO-220
A
5.100
4.900
INDEX AREA
5.100
4.900
2X 0.10 C
2X 0.10 C
TOP VIEW
B
// 0.10 C
0.08 C
1.000
0.800
0.20 REF
0.050
0.000
"A"
SIDE VIEW
C
0.20 MIN
3.800
3.500
0.450
0.350
PIN 9
3.500 □
3.800
3.500
0.300
0.180
0.10 C A B
0.05 C
0.45 REF
PIN 1
0.5
BOTTOM VIEW
0.050
0.000
DETAIL "A"
NOTES: ALL DIMENSIONS ARE mm
[MAX]
[MIN]

PART MARKING



Subject to change

ORDERING INFORMATION

SMB113A N C T nnn L

Summit Part Number
SMB113A, SMB113B, SMB117 or SMB117A

Package
N = 32-Pad QFN

Temperature Range
C = Commercial
BLANK = Industrial

Tape & Reel

Part Number Suffix
Specific requirements are contained in the suffix

Environmental Attribute
L = 100% Sn, RoHS compliant

The default device ordering number is SMB113ANC-650L. It is tested over the commercial temperature range. The ordering number is derived from the customer supplied hex file. New device suffix numbers are assigned to non-default requirements.

NOTICE

NOTE – This is a ***Preliminary*** data sheet that describes a Summit that is in pre-production with limited characterization.

SUMMIT Microelectronics, Inc. reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. SUMMIT Microelectronics, Inc. assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, SUMMIT Microelectronics, Inc. shall not be liable for any damages arising as a result of any error or omission.

SUMMIT Microelectronics, Inc. does not recommend the use of any of its products in life support or aviation applications where the failure or malfunction of the product can reasonably be expected to cause any failure of either system or to significantly affect their safety or effectiveness. Products are not authorized for use in such applications unless SUMMIT Microelectronics, Inc. receives written assurances, to its satisfaction, that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; and (c) potential liability of SUMMIT Microelectronics, Inc. is adequately protected under the circumstances.

Revision 2.6 This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at http://www.summitmicro.com for data sheet updates.