MULTIBUS II

PSB 2100 PSB II Reply Only Agent Error Generator

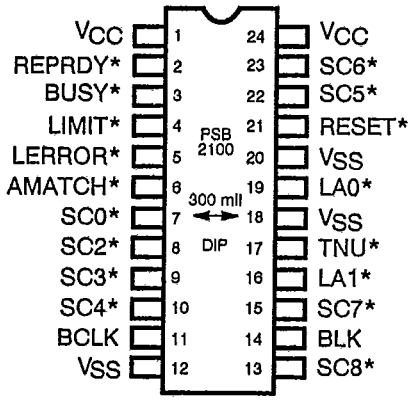
Distinctive Features

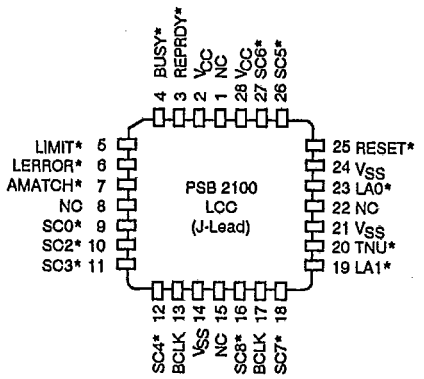
- Provides complete memory/IO error code generation including: width errors, transfer-not-understood errors, NACK errors, local data errors, and continuation errors for 8 bit reply only agents.
- Provides a parity signal (SC8*) over reply agent SC4* - SC7* signals.
- Integrates 64 mA three-state drivers required on SC5* - SC8* bus signals.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Supports sequential operations including broadcast.
- Can be used separately or together with PSB 2000 to provide complete reply only agent control interfact to iPSB II bus.

Applications

- Bus Interface Circuitry for iPSB II reply only agent modules such as I/O or memory devices.

Packages





PSB 2100 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The PSB 2100 is a CMOS iPSB II 8 bit Reply Only Agent error generator packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The PSB 2100 provides complete reply only agent memory/IO space error code generation and can drive the 64 mA three-state SC5* - SC8* signals directly. The PSB 2100 supports 8 bit memory or I/O accesses as well as 8 bit interconnect accesses and 32 bit messages. During the reply phase of the transfer the PSB 2100 will assert the appropriate error code and parity bit indicating either a valid transfer or and error condition due to width errors, transfer-not-understood errors, NACK errors, local data errors, or continuation errors. Other local errors can also be asserted to the PSB 2100 which will cause the transfer-not-understood error code to be generated. All errors are detected on memory and IO accesses only. Interconnect and message transfers are not checked for errors.

The PSB 2100 conforms to the Rev. C MULTIBUS II Bus Architecture Specification Handbook.

The PSB 2100 can be used separately to generate the SC5* - SC8* signals for the reply agent module that does not use the PSB 2000 as the reply only agent controller.

The PSB 2000 can be used in conjunction with the PSB2100 where the 2100 is used to generate the SC5* - SC8* signals and the PSB 2000 is used to generate the SC4* signal and BUSERR* signals. In this manner, the two chip set provides a compact interface to the IPSB II bus.

Pin Descriptions

PSB 2100

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	REPRDY*	I	Active low; Replier ready to conduct data transfer in next cycle.
4	3	BUSY*	I	Active low; Replier busy. Indicates replier can not reply now.
5	4	LIMIT*	I	Active low; Address limit. Indicates replier has reached address range limit.
6	5	LERROR*	I	Active low; Local error. Indicates local parity error.
7	6	AMATCH*	I	Active low; Address match. Indicates transfer is for this reply agent.
9	7	SC0*	I	Active low; Status/Control bit 0. Indicates request and non-request cycles.
10	8	SC2*	I	Active low; Status/Control bit 2. Indicates end of cycle during reply cycles.
11	9	SC3*	I	Active low; Status/Control bit 3. Indicates requester ready during reply cycles.
12	10	SC4*	I	Active low; Status/Control bit 4. Indicates replier ready during reply cycles.
13	11	BCLK	I	Inverted BCLK*. Connected to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	SC7*	O	Active low, 64 mA three-state; Status/Control bit 7. Error code output bit.
17	14	BCLK	I	Inverted BCLK*. Connected to pin 11 (DIP) or pin 13 (LCC).
18	15	SC8*	O	Active low; 64 mA three-state; Parity bit for SC4* - SC7* during reply cycles.
19	16	LA1*	I	Active low Latched address bit A1*.
20	17	TNU*	I	Active low; Transfer-not-understood error (externally generated).
23	19	LA0*	I	Active low; Latched address bit A0*.
25	21	RESET*	I	Active low; Logical 'OR' of local reset and local exception.
26	22	SC6*	O	Active low; 64 mA three-state; Status/Control bit 6. Error code output bit.
27	23	SC5*	O	Active low; 64 mA three-state; Status/Control bit 5. Error code output bit.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.