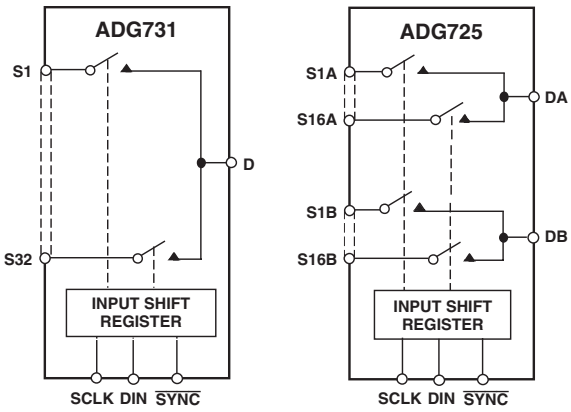
16-/32-Channel, Serially Controlled 4 Ω 1.8 V to 5.5 V, ±2.5 V, Analog Multiplexers

ADG725/ADG731

FEATURES
- 3-Wire SPI Compatible Serial Interface
- 1.8 V to 5.5 V Single Supply
- ±2.5 V Dual-Supply Operation
- 4 Ω On Resistance
- 0.5 Ω On Resistance Flatness
- 7 mm x 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package
- Rail-to-Rail Operation
- Power-On Reset
- 42 ns Switching Times
- Single 32-to-1 Channel Multiplexer
- Dual/Differential 16-to-1 Channel Multiplexer
- TTL/CMOS Compatible Inputs
- For Functionally Equivalent Devices with Parallel Interface, See ADG726/ADG732

APPLICATIONS
- Optical Applications
- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems
- Medical Instrumentation
- Automatic Test Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG731/ADG725 are monolithic, CMOS, 32-channel/dual 16-channel analog multiplexers with a serially controlled 3-wire interface. The ADG731 switches one of 32 inputs (S1–S32) to a common output, D. The ADG725 can be configured as a dual mux switching one of 16 inputs to one output, or a differential mux switching one of 16 inputs to a differential output.

These mulitplexers utilize a 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and some DSP interface standards. On power-up, the Internal Shift Register contains all zeros and all switches are in the OFF state.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed with very low on resistance and leakage currents. They operate from a single supply of 1.8 V to 5.5 V or a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms, is closely matched between switches, and is very flat over the full signal range.

These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG731 and ADG725 are serially controlled 32-channel, and dual/differential 16-channel multiplexers, respectively. They are available in either a 48-lead LFCSP or TQFP package.

PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. 1.8 V to 5.5 V Single-Supply or ±2.5 V Dual-Supply Operation. These parts are specified and guaranteed with 5 V ±10%, 3 V ±10% single-supply, and ±2.5 V ±10% dual-supply rails.
3. On Resistance of 4 Ω.
4. Guaranteed Break-Before-Make Switching Action.
5. 7 mm × 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADG725/ADG731–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match between		0.3	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = 1 V or 4.5 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	42		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	53	62	ns max	V_{S1} = 3 V/0 V, V_{S32} = 0 V/3 V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 3 V; Test Circuit 6
Charge Injection	5		pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	170		pF typ	f = 1 MHz
ADG731	340		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	175		pF typ	f = 1 MHz
ADG731	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	7		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On Resistance Match between		0.35	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω max	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_S = V_D = 1 V or 3 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	60		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	80	90	ns max	V_{S1} = 2 V/0 V, V_{S32} = 0 V/2 V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 2 V; Test Circuit 6
Charge Injection	1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	170		pF typ	f = 1 MHz
ADG731	340		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	175		pF typ	f = 1 MHz
ADG731	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	5		μA typ	Digital Inputs = 0 V or 3.3 V
		10	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

DUAL-SUPPLY SPECIFICATIONS[1] (V_{DD} = +2.5 V ± 10%, V_{SS} = –2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match Between		0.3	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = –2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V;
	±0.25	±0.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +2.25 V/–1.25 V; Test Circuit 4
ADG725	±0.5	±2.5	nA max	
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	55		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	75	84	ns max	V_{S1} = 1.5 V/0 V, V_{S32} = 0 V/1.5 V
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 1.5 V; Test Circuit 6
Charge Injection	1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG725	130		pF typ	f = 1 MHz
ADG731	260		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	150		pF typ	f = 1 MHz
ADG731	300		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +2.75 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 2.75 V
		20	μA max	
I_{SS}	10		μA typ	V_{SS} = –2.75 V
		20	μA max	Digital Inputs = 0 V or 2.75 V

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK Cycle Frequency
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_5	40	ns min	Minimum $\overline{SYNC}$ Low Time
t_6	5	ns min	Data Setup Time
t_7	4.5	ns min	Data Hold Time
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
Specifications subject to change without notice.

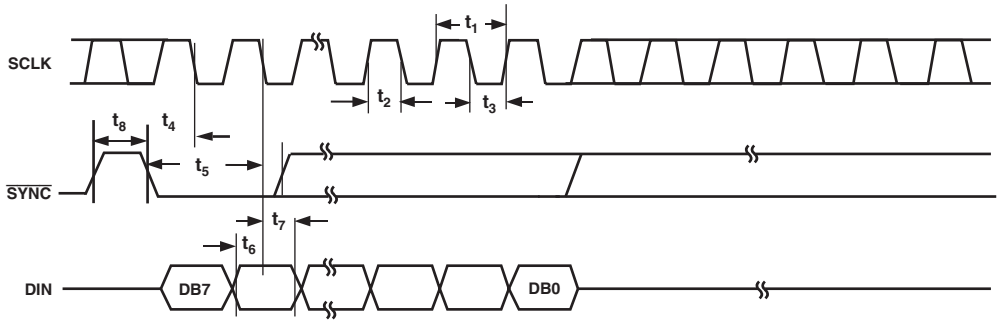


Figure 1. 3-Wire Serial Interface Timing Diagram

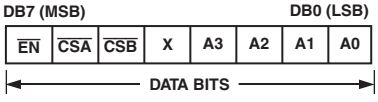


Figure 2. ADG725 Input Shift Register Contents

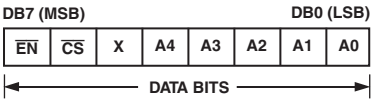


Figure 3. ADG731 Input Shift Register Contents

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to V_{SS} . . . . . 7 V
V_{DD} to GND . . . . . –0.3 V to +7 V
V_{SS} to GND . . . . . +0.3 V to –7 V
Analog Inputs[2] . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 60 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Thermal Impedance (4-Layer Board)
48-lead LFCSP . . . . . 25°C/W
48-lead TQFP . . . . . 54.6°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature (<20 seconds) . . . . . 235°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at SCLK, $\overline{\text{SYNC}}$, DIN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

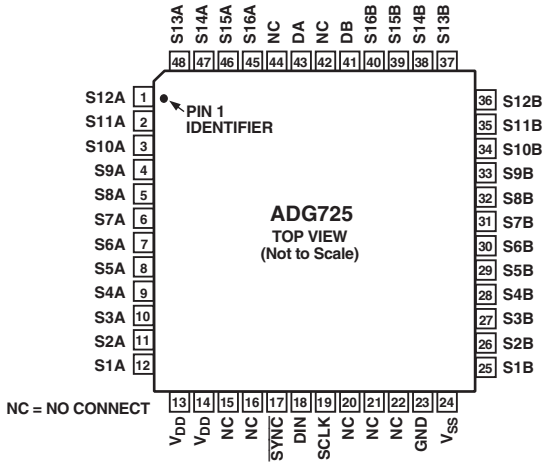
Model	Temperature Range	Package Description	Package Option
ADG725BCP	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BCP-REEL	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BCP-REEL7	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BSU	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG725BSU-REEL	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG731BCP	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BCP-REEL	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BCP-REEL7	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BSU	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG731BSU-REEL	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48

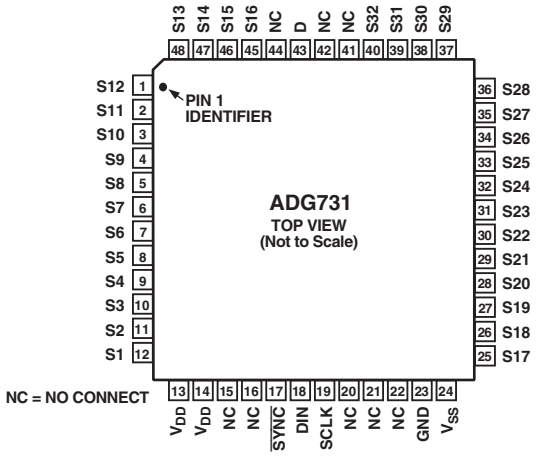
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG725/ADG731 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

48-Lead LFCSP and TQFP





PIN FUNCTION DESCRIPTIONS

ADG725	ADG731	Mnemonic	Function
1–12, 25–40, 45–48	1–12, 25–40, 45–48	Sxx	Source. May be an input or output.
13, 14	13, 14	V_{DD}	Power Supply Input. These parts can be operated from a single supply of 1.8 V to 5.5 V and a dual supply of ±2.5 V.
17	17	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input Shift Register is enabled. An 8-bit counter is also enabled. Data is transferred on the falling edges of the following clocks. After eight falling clock edges, switch conditions are automatically updated. $\overline{SYNC}$ may be used to frame the signal or just pulled low for a short period of time to enable the counter and input buffers.
18	18	DIN	Serial Data Input. Data is clocked into the 8-bit Input Register MSB first on the falling edge of the serial clock input.
19	19	SCLK	Serial Clock Input. Data is clocked into the Input Shift Register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
23	23	GND	Ground Reference
24	24	V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND.
41, 43	N/A	DA, DB	Drain. May be an input or output.
N/A	43	D	Drain. May be an input or output.

Table I. ADG725 Truth Table

A3	A2	A1	A0	$\overline{EN}$	$\overline{CSA}$	$\overline{CSB}$	Switch Condition
X	X	X	X	X	1	1	Retains Previous Switch Condition
X	X	X	X	1	X	X	All Switches OFF
0	0	0	0	0	0	0	S1A – DA, S1B – DB
0	0	0	1	0	0	0	S2A – DA, S2B – DB
0	0	1	0	0	0	0	S3A – DA, S3B – DB
0	0	1	1	0	0	0	S4A – DA, S4B – DB
0	1	0	0	0	0	0	S5A – DA, S5B – DB
0	1	0	1	0	0	0	S6A – DA, S6B – DB
0	1	1	0	0	0	0	S7A – DA, S7B – DB
0	1	1	1	0	0	0	S8A – DA, S8B – DB
1	0	0	0	0	0	0	S9A – DA, S9B – DB
1	0	0	1	0	0	0	S10A – DA, S10B – DB
1	0	1	0	0	0	0	S11A – DA, S11B – DB
1	0	1	1	0	0	0	S12A – DA, S12B – DB
1	1	0	0	0	0	0	S13A – DA, S13B – DB
1	1	0	1	0	0	0	S14A – DA, S14B – DB
1	1	1	0	0	0	0	S15A – DA, S15B – DB
1	1	1	1	0	0	0	S16A – DA, S16B – DB

X = Don't Care

Table II. ADG731 Truth Table

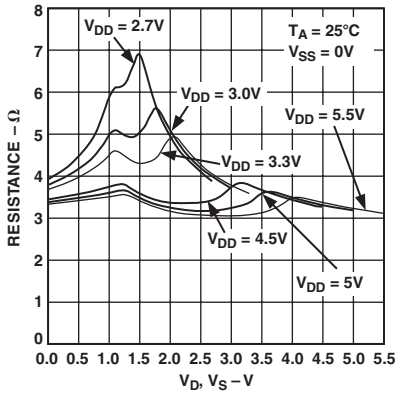
A4	A3	A2	A1	A0	$\overline{EN}$	$\overline{CSA}$	Switch Condition
X	X	X	X	X	X	1	Retains Previous Switch Condition
X	X	X	X	X	1	X	All Switches OFF
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	2
0	0	0	1	0	0	0	3
0	0	0	1	1	0	0	4
0	0	1	0	0	0	0	5
0	0	1	0	1	0	0	6
0	0	1	1	0	0	0	7
0	0	1	1	1	0	0	8
0	1	0	0	0	0	0	9
0	1	0	0	1	0	0	10
0	1	0	1	0	0	0	11
0	1	0	1	1	0	0	12
0	1	1	0	0	0	0	13
0	1	1	0	1	0	0	14
0	1	1	1	0	0	0	15
0	1	1	1	1	0	0	16
1	0	0	0	0	0	0	17
1	0	0	0	1	0	0	18
1	0	0	1	0	0	0	19
1	0	0	1	1	0	0	20
1	0	1	0	0	0	0	21
1	0	1	0	1	0	0	22
1	0	1	1	0	0	0	23
1	0	1	1	1	0	0	24
1	1	0	0	0	0	0	25
1	1	0	0	1	0	0	26
1	1	0	1	0	0	0	27
1	1	0	1	1	0	0	28
1	1	1	0	0	0	0	29
1	1	1	0	1	0	0	30
1	1	1	1	0	0	0	31
1	1	1	1	1	0	0	32

X = Don't Care

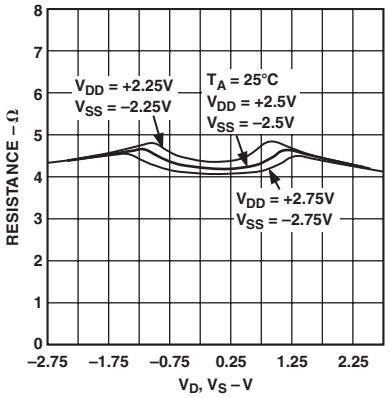
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match between any Two Channels.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch OFF.
I_D (OFF)	Drain Leakage Current with the Switch OFF.
I_D, I_S (ON)	Channel Leakage Current with the Switch ON.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
I_{INL} (I_{INH})	Input Current of the Digital Input.
C_S (OFF)	OFF Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	OFF Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	ON Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
$t_{TRANSITION}$	Delay time measured between the 50% points of the eighth clock falling edge and 90% points of the output when switching from one address state to another.
t_D	OFF time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
OFF Isolation	A measure of unwanted signal coupling through an OFF switch.
Crosstalk	A measure of unwanted signal is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency Response of the ON Switch.
Insertion Loss	The Loss Due to the On Resistance of the Switch.

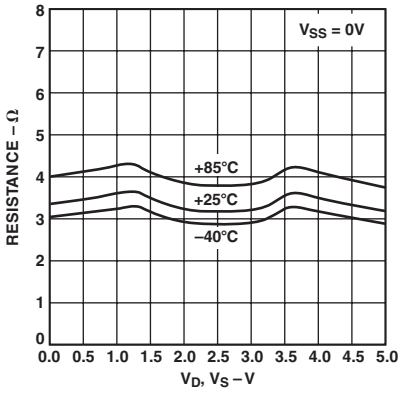
ADG725/ADG731–Typical Performance Characteristics



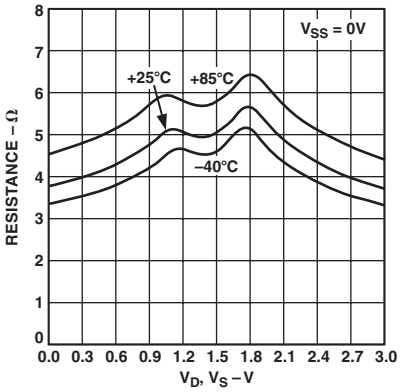
TPC 1. On Resistance vs. V_D (V_S), Single Supply



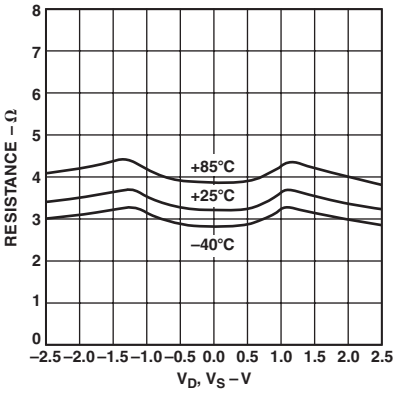
TPC 2. On Resistance vs. V_D (V_S), Dual Supply



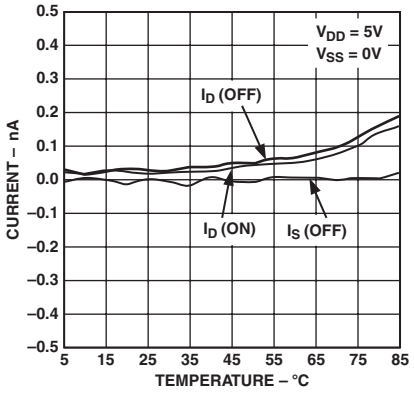
TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply



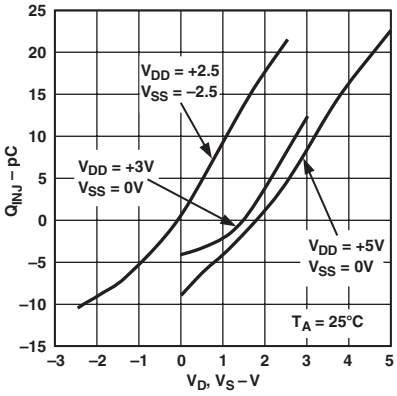
TPC 4. On Resistance vs. V_D (V_S), Single Supply



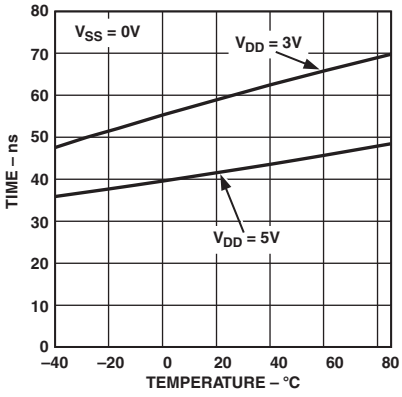
TPC 5. On Resistance vs. V_D (V_S), Dual Supply



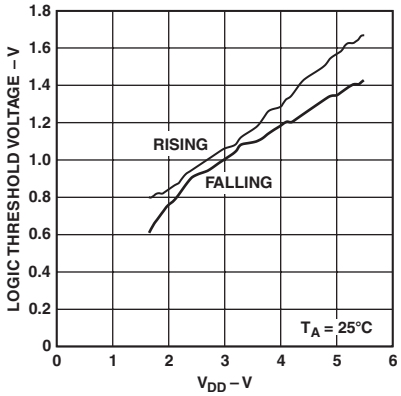
TPC 6. Leakage Currents vs. Temperature



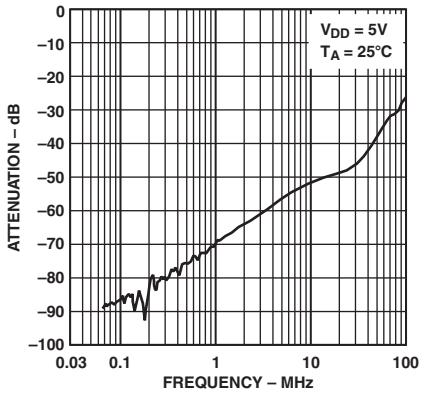
TPC 7. ADG731 Charge Injection vs. Source Voltage



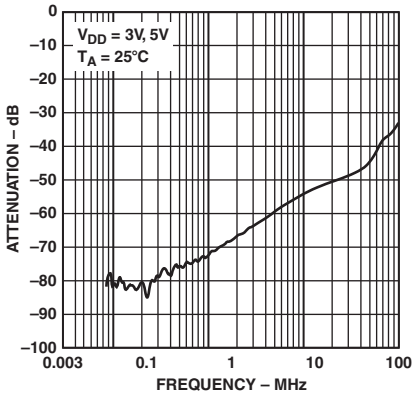
TPC 8. Switching Times vs. Temperature



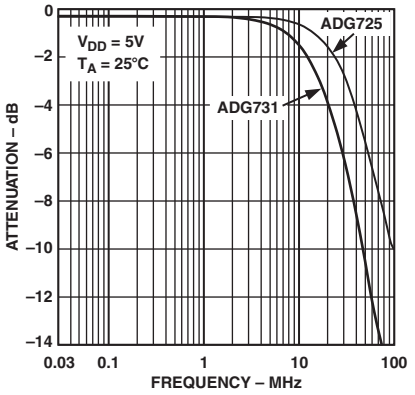
TPC 9. Logic Threshold Voltage vs. Supply Voltage



TPC 10. OFF Isolation vs. Frequency

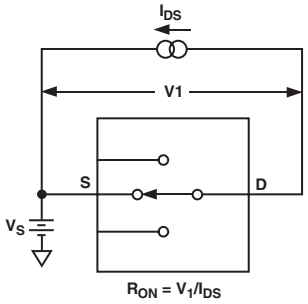


TPC 11. Crosstalk vs. Frequency

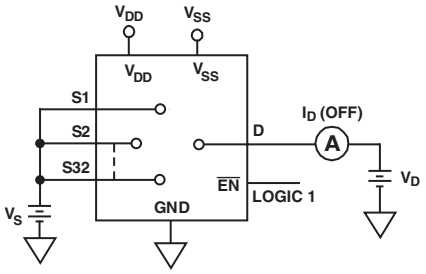


TPC 12. ON Response vs. Frequency

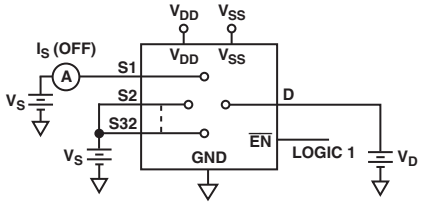
Test Circuits



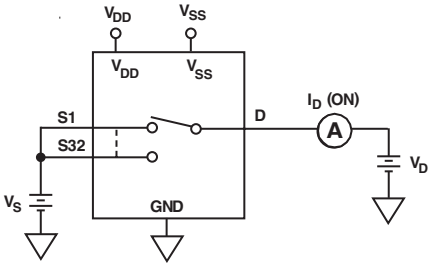
Test Circuit 1. On Resistance



Test Circuit 3. I_D (OFF)

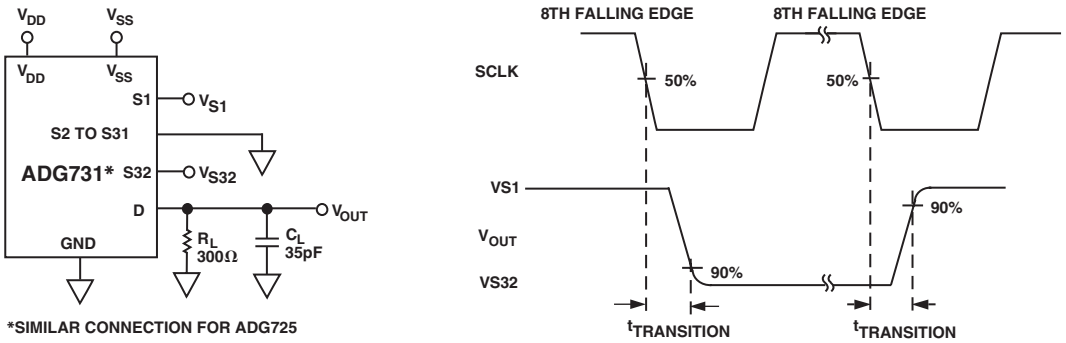


Test Circuit 2. I_S (OFF)

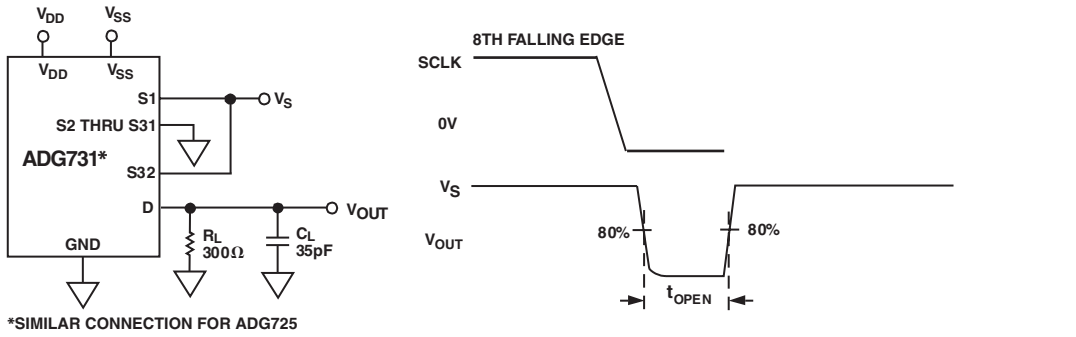


Test Circuit 4. I_D (ON)

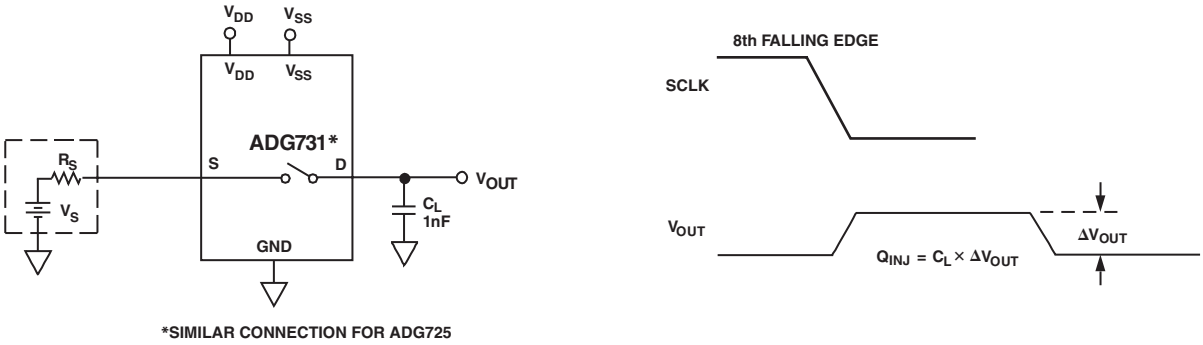
TEST CIRCUITS (continued)



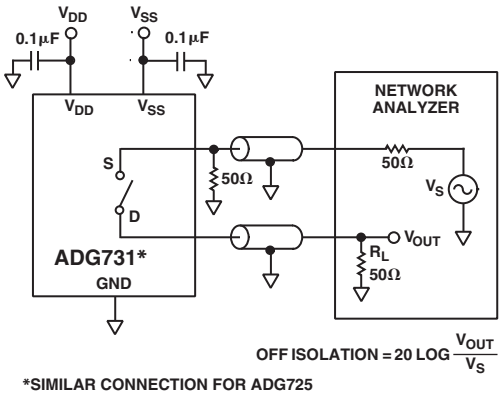
Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$



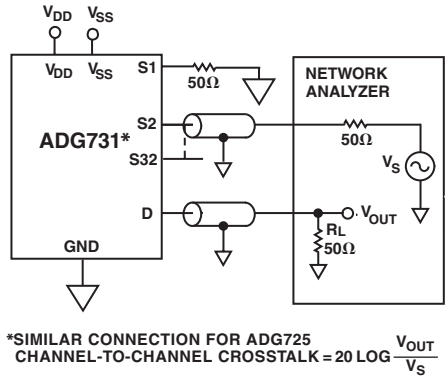
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



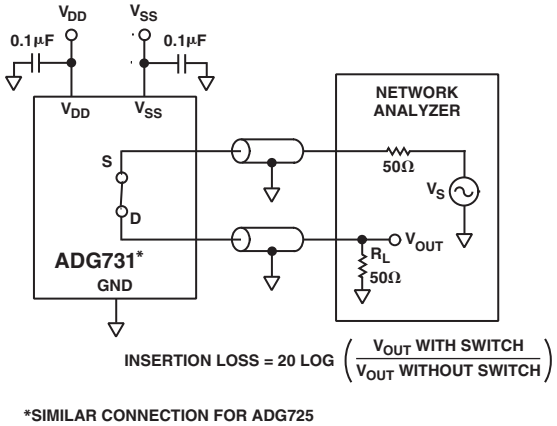
Test Circuit 7. Charge Injection



Test Circuit 8. OFF Isolation



Test Circuit 9. Channel-to-Channel Crosstalk



Test Circuit 10. Bandwidth

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition. The Internal Shift Register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG725 and ADG731 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit Shift Register via DIN under the control of the $\overline{SYNC}$ and SCLK signals.

When $\overline{SYNC}$ goes low, the Input Shift Register is enabled. An 8-bit counter is also enabled. Data from DIN is clocked into the Shift Register on the falling edge of SCLK. Figures 2 and 3 show the contents of the Input Shift Registers for these devices. When the part has received eight clock cycles after $\overline{SYNC}$ has been pulled low, the switches are automatically updated with the new configuration and the Input Shift Register is disabled.

The ADG725 $\overline{CSA}$ and $\overline{CSB}$ data bits allow the user the flexibility to change the configuration of either or both banks of the multiplexer.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG725/ADG731 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG725/ADG731 requires an 8-bit data-word with data valid on the falling edge of SCLK.

Figures 4–7 illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

ADSP-21xx to ADG725/ADG731 Interface

The ADSP-21xx family of DSPs are easily interfaced to the ADG725/ADG731 without the need for extra logic. Figure 4 shows an example of an SPI interface between the ADG725/ADG731 and the ADSP-2191M. SCK of the ADSP-2191M drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{SYNC}$ is driven from one of the port lines, in this case $\overline{SPIxSEL}$.

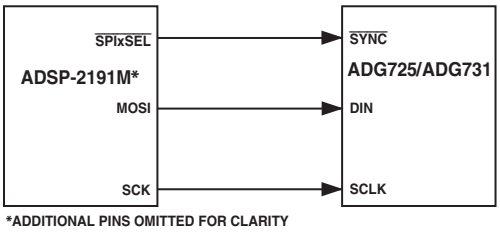


Figure 4. ADSP-2191M to ADG725/ADG731 Interface

A serial interface between the ADG725/ADG731 and the ADSP-2191M SPORT is shown in Figure 5. In this interface example, SPORT0 is used to transfer data to the switch. Transmission is initiated by writing a word to the Tx Register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the ADG725/ADG731 on the falling edge of its SCLK. The update of each switch condition takes place automatically after the eighth SCLK falling edge, regardless of the frame sync condition.

Communication between two devices at a given clock speed is possible when the following specs are compatible: frame sync delay and frame sync setup and hold, data delay and data setup and hold, and SCLK width. The ADG725/ADG31 expects a t_4 ($\overline{SYNC}$ falling edge to SCLK falling edge set-up time) of 13 ns minimum. Consult the ADSP-21xx User Manual for information on clock and frame sync frequencies for the SPORT Register.

The SPORT Control Register should be set up as follows:

TFSW = 1, Alternate Framing

INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

ISCLK = 1, Internal Serial Clock

TFSR = 1, Frame Every Word

ITFS = 1, Internal Framing Signal

SLEN = 0111, 8-Bit Data-Word

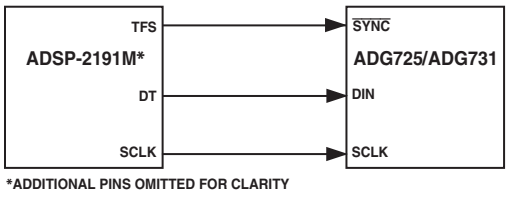


Figure 5. ADSP-2191M to ADG725/ADG731 Interface

8051 to ADG725/ADG731 Interface

A serial interface between the ADG725/ADG731 and the 8051 is shown in Figure 6. TXD of the 8051 drives SCLK of the ADG725/ADG731, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$.

The 8051 provides the LSB of its SBUF Register as the first bit in the data stream. The user will have to ensure that the data in the SBUF Register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result, no glue logic is required between the ADG725/ADG731 and microcontroller interface.

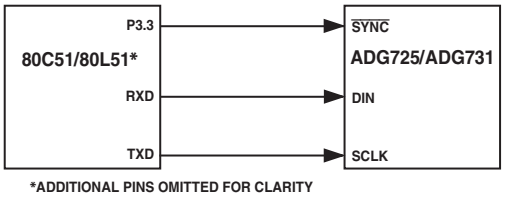


Figure 6. 8051 to ADG725/ADG731 Interface

MC68HC11 Interface to ADG725/ADG731

Figure 7 shows an example of a serial interface between the ADG725/ADG731 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{SYNC}$ is driven from one of the port lines, in this case PC7. The 68HC11 is configured for Master Mode: MSTR = 1, CPOL = 0, and CPHA = 1. When data is transferred to the part, PC7 is taken low, and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

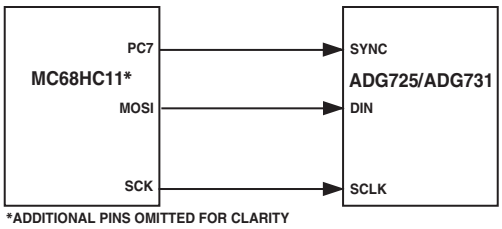


Figure 7. MC68HC11 Interface to ADG725/ADG731

APPLICATION CIRCUITS

ADG725/ADG731 in an Optical Network Control Loop

The ADG725/ADG731 can be used in optical network applications that have higher port counts and greater multiplexing requirements. The ADG725/ADG731 are well suited to these applications because they allow a single control circuit to connect a higher number of channels without increasing board size and design complexity.

In the circuit shown in Figure 8, the 0 V to 5 V outputs of the AD5532HS are amplified to a range of 0 V to 180 V and then used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor readings are muxed using the ADG731, a 32-channel switch, and fed back to a single-channel 14-bit ADC (AD7894).

The control loop is driven by an ADSP-2191L, a 32-bit DSP with an SPI compatible SPORT interface. It writes data to the DAC, controls the multiplexer, and reads data from the ADC via a 3-wire serial interface.

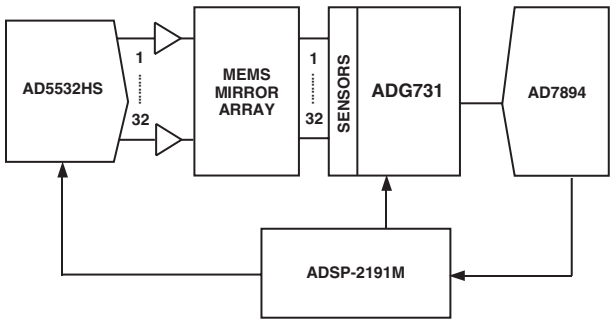


Figure 8. Optical Network Control Loop

Expand the Number of Selectable Serial Devices Using the ADG725/ADG731

The $\overline{SYNC}$ pin of the ADG725/ADG731 can be used to select one of a number of multiplexers. All devices receive the same serial clock and serial data, but only one device will receive the

$\overline{\text{SYNC}}$ signal at any one time. The mux addressed will be determined by the decoder. There will be some digital feedthrough from the digital input lines. Using a burst clock will minimize the effects of digital feedthrough on the analog signal channels. Figure 9 shows a typical circuit.

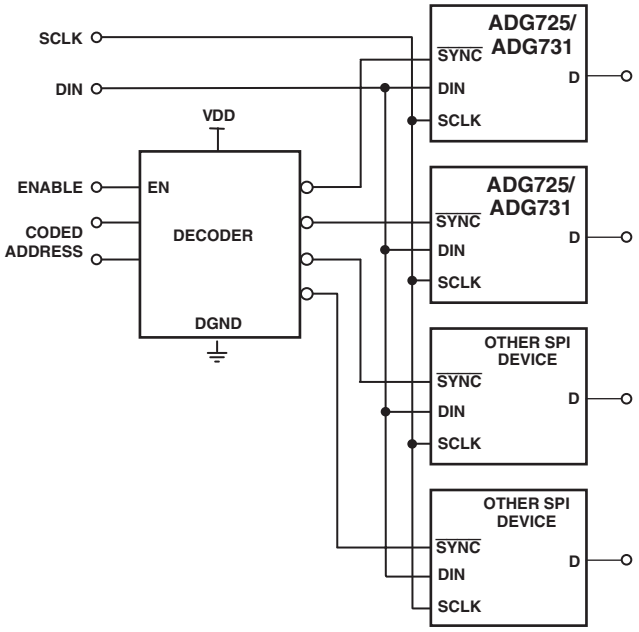
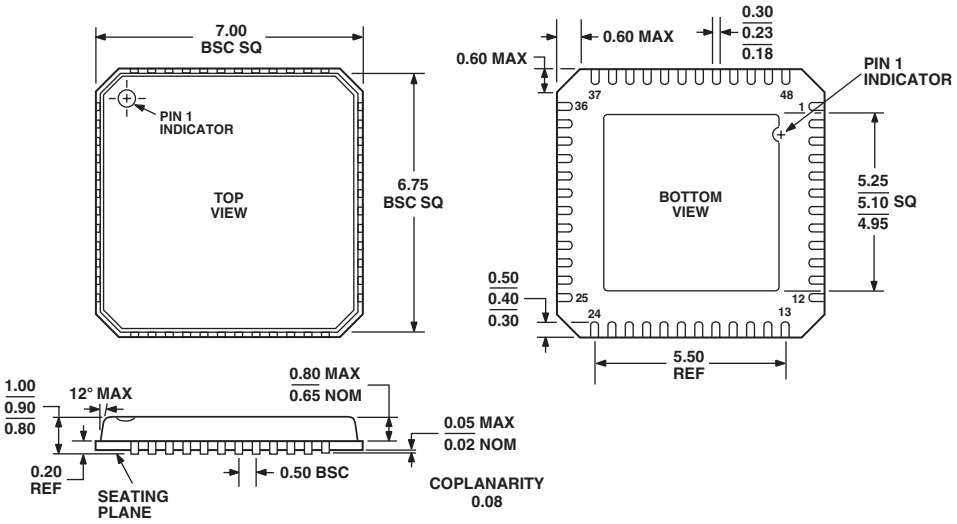


Figure 9. Addressing Multiple ADG725/ADG731s Using a Decoder

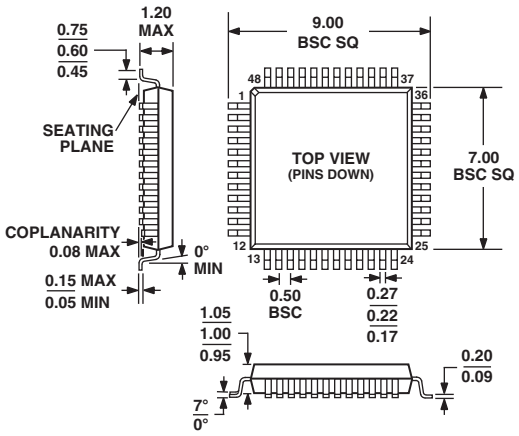
OUTLINE DIMENSIONS

48-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

48-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026ABC

Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
Edits to ORDERING GUIDE	6
Edits to PIN CONFIGURATIONS	7
Edits to PIN FUNCTION DESCRIPTIONS	7
Changes to Test Circuit 3	11
Updated OUTLINE DIMENSIONS	16