DATA SHEET

Xilinx has acquired the entire Philips CoolRunner Low Power CPLD Product Family. For more technical or sales information, please see: www.xilinx.com

XCR3032C

32 macrocell CPLD with enhanced clocking

Product specification
Supersedes data of 1998 Jun 24
IC27 Data Handbook

1998 Jul 23

Philips
Semiconductors

PHILIPS

32 macrocell CPLD with enhanced clocking

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FEATURES

- Industry's first TotalCMOS™ PLD – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- High speed pin-to-pin delays of 8ns
- Ultra-low static power of less than 35µA
- Dynamic power that is 70% lower at 50MHz than competing devices
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Up to 6 clocks with programmable polarity at every macrocell
- 3.3 Volt, In-System Programmable (ISP) using a JTAG interface
  - On-chip supervoltage generation
  - ISP commands include: Enable, Erase, Program, Verify
  - Supported by multiple ISP programming platforms
  - 4 pin JTAG interface (TCK, TMS, TDI, TDO)
  - JTAG commands include: Bypass, Idcode
- Support for complex asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Philips CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-State buffer
  - Asynchronous macrocell register preset/reset
  - Up to 2 asynchronous clocks
- Programmable global 3-State pin facilitates 'bed of nails' testing without using logic resources
- Available in both PLCC and TQFP packages

Table 1. PZ3032C Features

	PZ3032C
Usable gates	1000
Maximum inputs	36
Maximum I/Os	32
Number of macrocells	32
I/O macrocells	32
Buried macrocells	0
Propagation delay (ns)	8.0
Packages	44-pin PLCC, 44-pin TQFP

DESCRIPTION

The PZ3032C CPLD (Complex Programmable Logic Device) is a member of the Fast Zero Power (FZP™) family of CPLDs from Philips Semiconductors. These devices combine high speed and zero power in a 32 macrocell CPLD. With the FZP™ design technique, the PZ3032C offers true pin-to-pin speeds of 8ns, while simultaneously delivering power that is less than 35µA at standby without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD—70% lower at 50MHz. These devices are the first TotalCMOS™ PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP™ design technique. For 5V applications, Philips also offers the high speed PZ5032C CPLD that offers pin-to-pin speeds of 6ns.

The Philips FZP™ CPLDs introduce the new patent-pending XPLA™ (extended Programmable Logic Array) architecture. The XPLA™ architecture combines the best features of both PLA and PAL™ type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA™ structure in each logic block provides a fast 8ns PAL™ path with 5 dedicated product terms per output. This PAL™ path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2.5ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 10.5ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The PZ3032C CPLDs are supported by industry standard CAE tools (Cadence, Exemplar Logic, Minc, Mentor, Synopsys, Synario, Viewlogic, OrCAD), using text (Abel, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses either Minc or Philips Semiconductors-developed tools.

The PZ3032C CPLD is reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others. The PZ3032C also includes an industry-standard, IEEE 1149.1, JTAG interface through which In-System Programming (ISP) and reprogramming of the device are supported.

PAL is a registered trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION

ORDER CODE	DESCRIPTION	DESCRIPTION	DRAWING NUMBER
PZ3032CS8A44	44-pin PLCC, 8ns t_{PD}	Commercial temp range, 3.3 volt power supply, ± 10%	SOT187-2
PZ3032CS10A44	44-pin PLCC, 10ns t_{PD}	Commercial temp range, 3.3 volt power supply, ± 10%	SOT187-2
PZ3032CS12A44	44-pin PLCC, 12ns t_{PD}	Commercial temp range, 3.3 volt power supply, ± 10%	SOT187-2
PZ3032CS8BC	44-pin TQFP, 8ns t_{PD},	Commercial temp range, 3.3 volt power supply, ± 10%	SOT376-1
PZ3032CS10BC	44-pin TQFP, 10ns t_{PD}	Commercial temp range, 3.3 volt power supply, ± 10%	SOT376-1
PZ3032CS12BC	44-pin TQFP, 12ns t_{PD}	Commercial temp range, 3.3 volt power supply, ± 10%	SOT376-1

XPLA™ ARCHITECTURE

Figure 1 shows a high level block diagram of a 32 macrocell device implementing the XPLA™ architecture. The XPLA™ architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner™ family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. The 6 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. In addition, two of the control terms can be used as clock signals (see Macrocell Architecture section for details). The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has 5 dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the PZ3032C device through the PAL array is 8ns. This performance is the fastest 3 volt CPLD available today. If a macrocell needs more than 5 product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using 1 or all 32 PLA product terms is just 2.5ns. So the total pin-to-pin t_{PD} for the PZ3032C using 6 to 37 product terms is 10.5ns (8ns for the PAL + 2.5ns for the PLA).

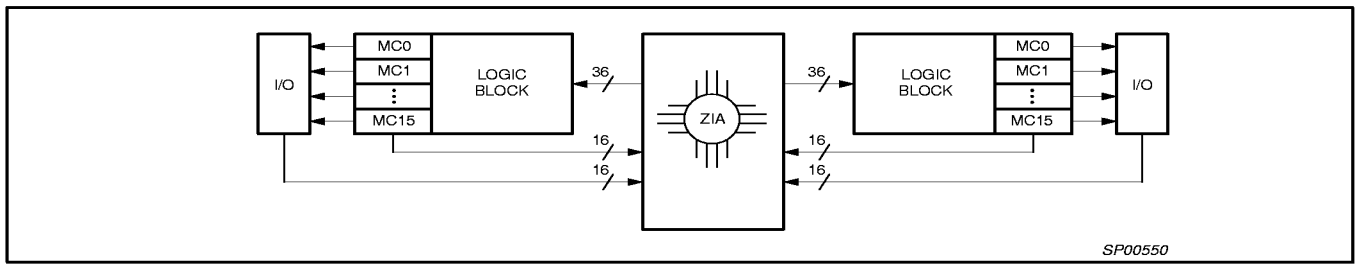


Figure 1. Philips XPLA CPLD Architecture

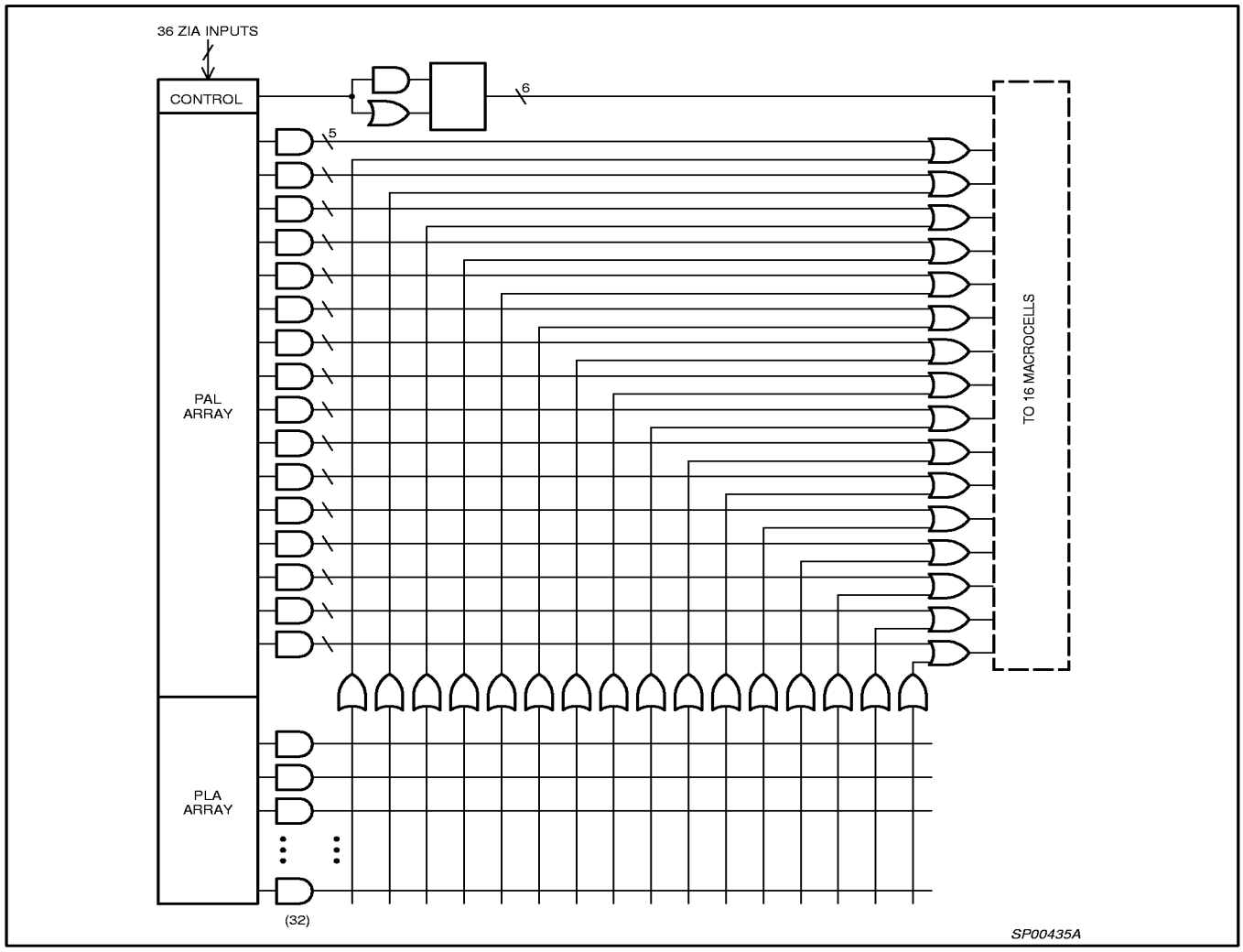


Figure 2. Philips XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner™ PZ3032C. The macrocell can be configured as either a D or T type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of four sources. Two of the clock sources (CLK0 and CLK1) are connected to low-skew, device-wide clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. Clock 0 (CLK0) is designated as a "synchronous" clock and must be driven by an external source. Clock 1 (CLK1) can be used as a "synchronous" clock that is driven by an external source, or as an "asynchronous" clock that is driven by a macrocell equation. Both CLK0 and CLK1 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are two of the six control terms (CT2 and CT3) provided in each logic block. These clocks can be individually configured as either a PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. The timing for asynchronous and control term clocks is different in that the Tco time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the Tsu time is reduced. Please see the app note titled "Understanding CoolRunner Clocking Options" for more detail.

The six control terms of each logic block are used to control the asynchronous Preset/Reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1 are used to control the asynchronous Preset/Reset of the macrocell's flip-flop. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied, and that the Preset/Reset feature for each macrocell can also be disabled. Control terms CT2 and CT3 can be used as a clock signal to the flip-flops of the macrocells, and as the Output Enable of the macrocell's output buffer. Control terms CT4 and CT5 can be used to control the Output Enable of the macrocell's output buffer. Having four dedicated Output Enable control terms ensures that the CoolRunner™ devices are PCI compliant. The output buffers can also be always enabled or always disabled. All CoolRunner™ devices also provide a Global Tri-State (GTS) pin, which, when enabled and pulled Low, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails" testing.

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin feedback path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-Stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated (See the section on terminations in this data sheet and the app note *Terminating Unused CoolRunner™ I/O Pins*).

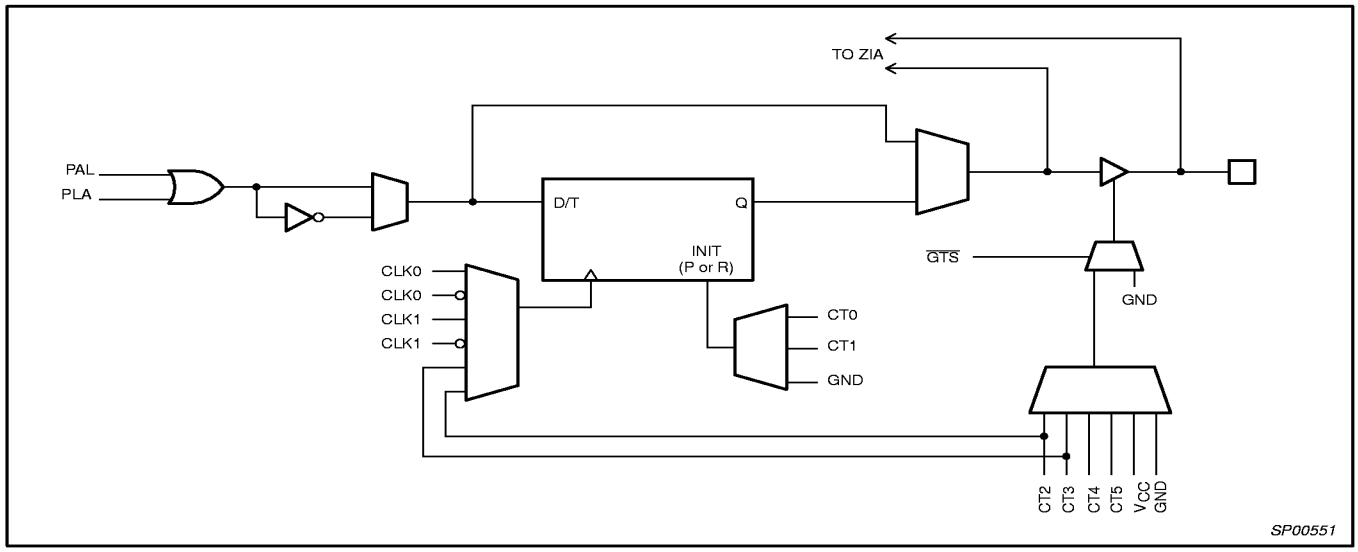


Figure 3. PZ3032C Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner™ Timing Model. The CoolRunner™ timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA™ architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model. For example, in the PZ3032C device, the user knows up front that if a given output uses 5 product terms or less, the t_{PD} = 8ns, the t_{SU} = 6.5ns, and the t_{CO} = 7.5ns. If an output is using 6 to 37 product terms, an additional 2.5ns must be added to the t_{PD} and t_{SU} timing parameters to account for the time to propagate through the PLA array.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 2 showing the I_{DD} vs. Frequency of our PZ3032C TotalCMOS™ CPLD.

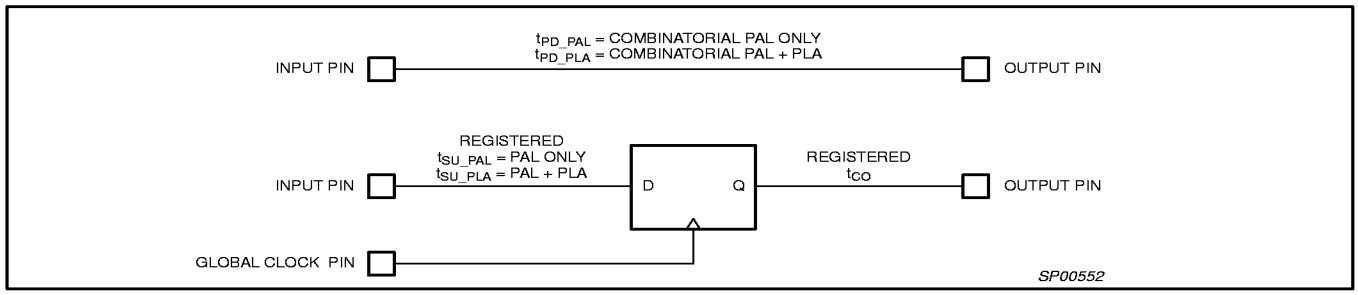


Figure 4. CoolRunner™ Timing Model

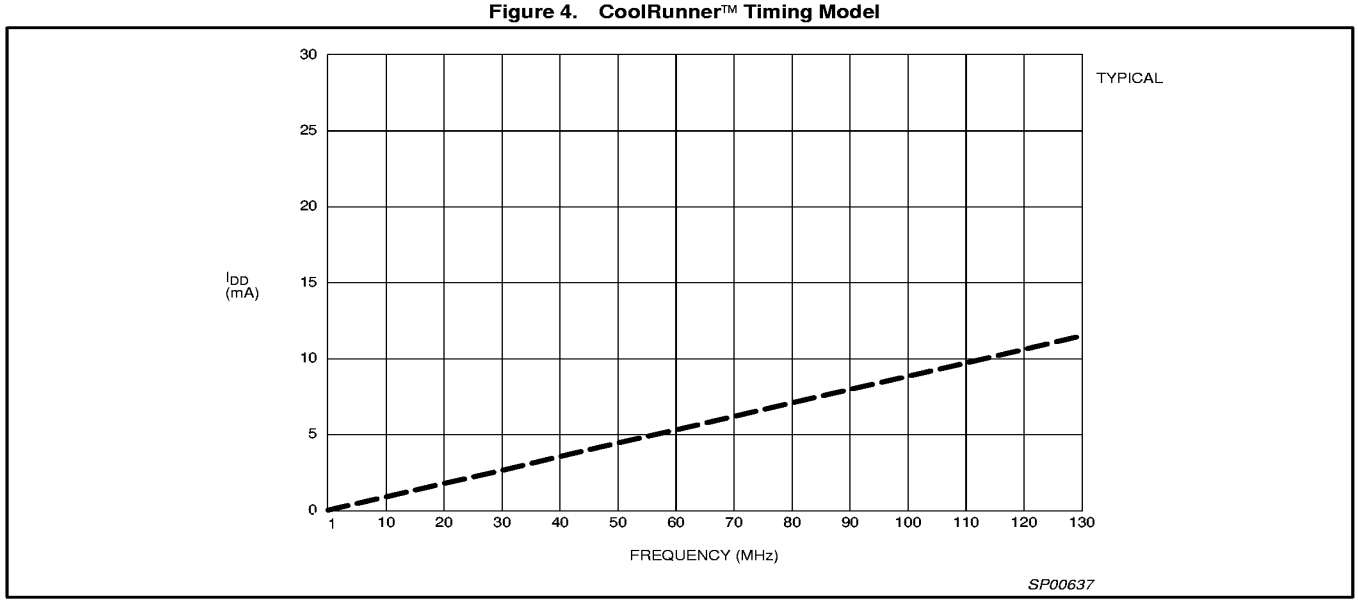


Figure 5. I_{DD} vs. Frequency @ V_{DD} = 3.3V

Table 2. I_{DD} vs Frequency

V_{DD} = 3.3V

FREQ (MHz)	0	1	10	20	30	40	50	60	70	80	90	100	110	120	130
Typical I_{DD} (mA)	0.01	0.10	0.89	1.77	2.63	3.55	4.44	5.3	6.19	7.08	7.96	8.83	9.7	10.6	11.5

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. The Philips PZ3032C devices use the JTAG interface for In–System Programming/Reprogramming. Although only a subset of the full JTAG command set is implemented (see Table 5), the devices are fully capable of sitting in a JTAG scan chain.

The Philips PZ3032C's JTAG interface includes a TAP Port defined by the IEEE 1149.1 JTAG Specification. As implemented in the Philips PZ3032C, the TAP Port includes four of the five pins (refer to Table 3) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Philips PZ3032C saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Philips PZ3032C supports the test reset functionality through the use of its power up reset circuit, which is included in all Philips CPLDs. The pins associated with the TAP Port should connect to an external pull–up resistor to keep the JTAG pins from floating when they are not being used (see section on Terminations).

In the Philips PZ3032C, the four mandatory JTAG pins each require a unique, dedicated pin on the device. The devices come from the factory with these I/O pins set to perform JTAG functions, but through the software, the final function of these pins can be controlled. If the end application will require the device to be reprogrammed at some future time with ISP, then the pins can be left as dedicated JTAG functions, which means they are not available for use as general purpose I/O pins. However, unlike competing CPLDs, the Philips PZ3032C allow the macrocells associated with these pins to be used as buried logic when the JTAG/ISP function is enabled. This is the default state for the software, and no action is required to leave these pins enabled for the JTAG/ISP functions. If, however, JTAG/ISP is not required to leave these pins enabled for the JTAG/ISP functions. If, however, JTAG/ISP is not required in the end application, the software can specify that this function be turned off and that these pins be used as general purpose I/O. Because the devices initially have the JTAG/ISP functions enabled, the JEDEC file can be downloaded into the device once, after which the JTAG/ISP pins will become general purpose I/O. This feature is good for manufacturing because the devices can be programmed during test and assembly of the end product and yet still use all of the I/O pins after the programming is done. It eliminates the need for a costly, separate programming step in the manufacturing process. Of course, if the JTAG/ISP function is never required, this feature can be turned off in the software and the device can be programmed with an industry-standard programmer, leaving the pins available for I/O functions. Table 4 defines the dedicated pins used by the four mandatory JTAG signals for each of the PZ3032C package types.

Table 3. JTAG Pin Description

PIN	NAME	DESCRIPTION
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 4. PZ3032C JTAG Pinout by Package Type

DEVICE	(PIN NUMBER / MACROCELL #)			
	TCK	TMS	TDI	TDO
PZ3032C				
44-pin PLCC	32/B8	13/A8	7/A3	38/B3
44-pin TQFP	26/B8	7/A8	1/A3	32/B3

Table 5. PZ3032C Low-Level JTAG Boundary-Scan Commands

INSTRUCTION (Instruction Code) *Register Used*	DESCRIPTION
Bypass (1111) *Bypass Register*	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
Idcode (0001) *Boundary-Scan Register*	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.

3.3-Volt, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-Functional hardware
  - Reconfigurability for Test
  - Eliminates handling of "fine lead-pitch" components for programming
  - Reduced Inventory and manufacturing costs
  - Improved quality and reliability
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, re-configuration, and customization

The Philips PZ3032C allows for 3.3-Volt, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided supervoltages, so that the PZ3032C may be easily programmed on the circuit board using only the 3.3-volt supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the PZ3032C enable this feature. The ISP commands implemented in the Philips PZ3032C are specified in Table 6. Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command.

Terminations

The CoolRunner™ PZ3032C CPLDs are TotalCMOS™ devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. The PZ3032C devices do not have on-chip termination circuits, so it is recommended that unused inputs and I/O pins be properly terminated. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. Philips recommends the use of 10KΩ pull-up resistors for the termination. Using pull-up resistors allows the flexibility of using these pins should late design changes require additional I/O. These unused pins may also be tied directly to V_{DD}, but this will make it more difficult to reclaim the use of the pin, should this be needed by a subsequent design revision.

When using the JTAG/ISP functions, it is also recommended that 10KΩ pull-up resistors be used on each of the four mandatory signals. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times. See the application notes *JTAG and ISP in Philips Devices* and *Terminating Unused CoolRunner™ I/O Pins* for more information.

Table 6. Low Level ISP Commands

INSTRUCTION *(Register Used)*	INSTRUCTION CODE	DESCRIPTION
Enable *(ISP Shift Register)*	1001	Enables the Erase, Program, and Verify commands.
Erase *(ISP Shift Register)*	1010	Erases the entire EEPROM array.
Program *(ISP Shift Register)*	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row.
Verify *(ISP Shift Register)*	1100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The outputs during this operation can be defined by the user.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Philips PZ3032C supports the following methods:

- PC Parallel Port
- Workstation or PC Serial Port
- Embedded Processor
- Automated Test Equipment
- Third party Programmers
- High-End ISP Tools

For more details on JTAG and ISP for the PZ3032C, refer to the related application note: *JTAG and ISP in Philips CPLDs*.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	3.0	3.6	V
I_{CCP}	I_{CC} limit program/verify		200	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{SOL}	Output voltage (Low)		0.5	V
V_{SOH}	Output voltage (High)	2.4		V
TDO_I_{OL}	Output current (Low)	8		mA
TDO_I_{OH}	Output current (High)	8		mA
AC Parameters				
f_{MAX}	TCK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		µs
INIT	Initialization time	100		µs
TMS_SU	TMS setup time before TCK ↑	10		ns
TDI_SU	TDI setup time before TCK ↑	10		ns
TMS_H	TMS hold time after TCK ↑	25		ns
TDI_H	TDI hold time after TCK ↑	25		ns
TDO_CO	TDO valid after TCK ↓		40	ns

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage[2]	–0.5	7.0	V
V_I	Input voltage	–1.2	V_{DD}+0.5	V
V_{OUT}	Output voltage	–0.5	V_{DD}+0.5	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{str}	Storage temperature	–65	150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	3.3 ±10% V

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial: 0°C ≤ T_{amb} ≤ +70°C; 3.0V ≤ V_{DD} ≤ 3.6V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	V_{DD} = 3.0V		0.8	V
V_{IH}	Input voltage high	V_{DD} = 3.6V	2.0		V
V_I	Input clamp voltage[3]	V_{DD} = 3.0V, I_{IN} = –18mA		–1.2	V
V_{OL}	Output voltage low	V_{DD} = 3.0V, I_{OL} = 8mA		0.5	V
V_{OH}	Output voltage high	V_{DD} = 3.0V, I_{OH} = –8mA	2.4		V
I_{IL}	Input leakage current low	V_{DD} = 3.6V (except CKO), V_{IN} = 0V	–10	10	µA
I_{IH}	Input leakage current high	V_{DD} = 3.6V, V_{IN} = 3.0V	–10	10	µA
I_{IL}	Clock input leakage current	V_{DD} = 3.6V, V_{IN} = 0.4V	–10	10	µA
I_{OZL}	3-Stated output leakage current low	V_{DD} = 3.6V, V_{IN} = 0.4V	–10	10	µA
I_{OZH}	3-Stated output leakage current high	V_{DD} = 3.6V, V_{IN} = 3.0V	–10	10	µA
I_{DDQ}[1]	Standby current	V_{DD} = 3.6V, T_{amb} = 0°C		35	µA
I_{DDD}[1, 2]	Dynamic current	V_{DD} = 3.6V, T_{amb} = 0°C @ 1MHz		0.3	mA
		V_{DD} = 3.6V, T_{amb} = 0°C @ 50MHz		10	mA
I_{OS}	Short circuit output current[3]	1 pin at a time for no longer than 1 second	–5	–100	mA
C_{IN}	Input pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{amb} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		10	pF

NOTES:
1. See Table 2, page 6 for typical values.
2. This parameter measured with a 16–bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
3. This parameter guaranteed by design and characterization, not by test.

AC ELECTRICAL CHARACTERISTICS[1] FOR COMMERCIAL GRADE DEVICES

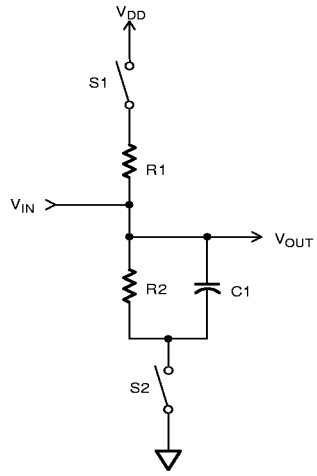
Commercial: 0°C ≤ T_{amb} ≤ +70°C; 3.0V ≤ V_{DD} ≤ 3.6V

SYMBOL	PARAMETER	8		10		12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	8	2	10	2	12	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	10	3	13	3	15	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	6	2	9	2	11	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	5		8.5		10.5		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	7		11.5		13.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		5		ns
t_{CL}	Clock Low time	3		4		5		ns
t_R	Input rise time		20		20		20	ns
t_F	Input fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $(1/t_{CH} + t_{CL})$	167		125		100		MHz
f_{MAX2}	Maximum internal frequency[2] $(1/t_{SUPAL} + t_{CF})$	95		63		50		MHz
f_{MAX3}	Maximum external frequency[2] $(1/t_{SUPAL} + t_{CO})$	91		57		47		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		6.5		8.5		10.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL + PLA		9		11.5		13.5	ns
t_{CF}	Clock to internal feedback node delay time		5.5		7.5		9.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50		50	µs
t_{ER}	Input to output disable[2, 3]		11		17		19	ns
t_{EA}	Input to output valid[2]		11		17		19	ns
t_{RP}	Input to register preset[2]		14		18		20	ns
t_{RR}	Input to register reset[2]		14		21		23	ns

NOTES:
1. Specifications measured with one output switching. See Figure 6 and Table 7 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5pF.

SWITCHING CHARACTERISTICS

The test load circuit and load values for the AC Electrical Characteristics are illustrated below.



COMPONENT	VALUES
R1	390Ω
R2	390Ω
C1	35pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Closed
t_P	Closed	Closed

NOTE: For t_{PHZ} and t_{PLZ} C = 5pF, and 3-State levels are measured 0.5V from steady-state active level.

SP00477

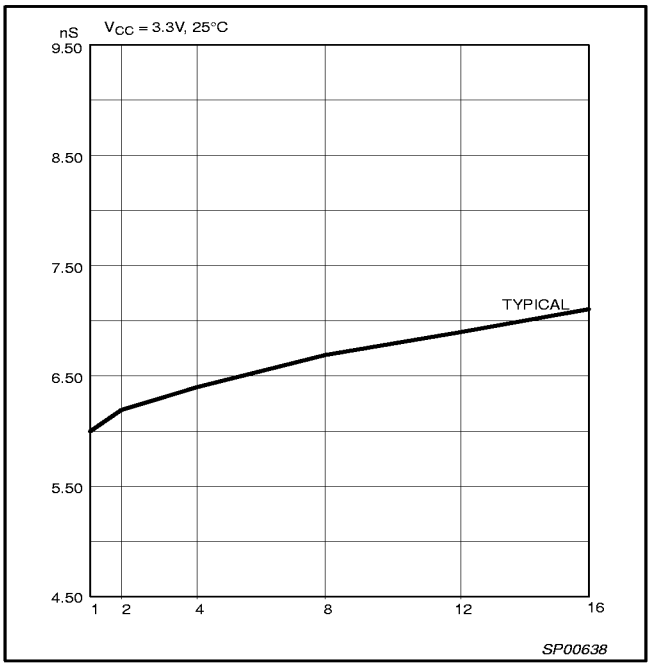
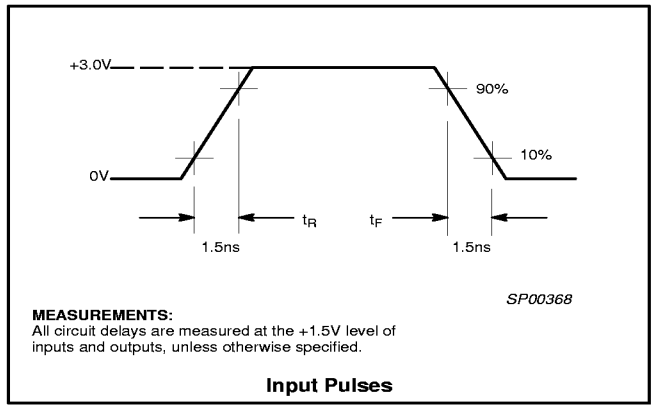


Figure 6. t_{PD_PAL} vs. Outputs switching

VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

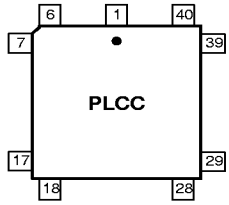
Table 7. t_{PD_PAL} vs. # of Outputs switching

V_{DD} = 3.30V, T = 25°C

# of Outputs	1	2	4	8	12	16
Typical (ns)	6.0	6.2	6.4	6.7	6.9	7.1

PIN DESCRIPTIONS

PZ3032C – 44-Pin Plastic Leaded Chip Carrier



Pin	Function	Pin	Function	Pin	Function
1	IN1	16	I/O–A10	31	I/O–B9
2	IN3	17	I/O–A11	32	I/O–B8 (TCK)
3	V_{DD}	18	I/O–A12	33	I/O–B7
4	I/O–A0–CK1	19	I/O–A13	34	I/O–B6
5	I/O–A1	20	I/O–A14	35	V_{DD}
6	I/O–A2	21	I/O–A15	36	I/O–B5
7	I/O–A3 (TDI)	22	GND	37	I/O–B4
8	I/O–A4	23	V_{DD}	38	I/O–B3 (TDO)
9	I/O–A5	24	I/O–B15	39	I/O–B2
10	GND	25	I/O–B14	40	I/O–B1
11	I/O–A6	26	I/O–B13	41	I/O–B0
12	I/O–A7	27	I/O–B12	42	GND
13	I/O–A8 (TMS)	28	I/O–B11	43	IN0–CK0
14	I/O–A9	29	I/O–B10	44	IN2–gtsn
15	V_{DD}	30	GND		

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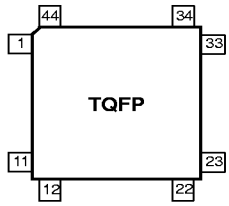
PZ3032C – 44-Pin Thin Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O–A3 (TDI)	16	GND	31	I/O–B4
2	I/O–A4	17	V_{DD}	32	I/O–B3 (TDO)
3	I/O–A5	18	I/O–B15	33	I/O–B2
4	GND	19	I/O–B14	34	I/O–B1
5	I/O–A6	20	I/O–B13	35	I/O–B0
6	I/O–A7	21	I/O–B12	36	GND
7	I/O–A8 (TMS)	22	I/O–B11	37	IN0–CK0
8	I/O–A9	23	I/O–B10	38	IN2–gtsn
9	V_{DD}	24	GND	39	IN1
10	I/O–A10	25	I/O–B9	40	IN3
11	I/O–A11	26	I/O–B8 (TCK)	41	V_{DD}
12	I/O–A12	27	I/O–B7	42	I/O–A0–CK1
13	I/O–A13	28	I/O–B6	43	I/O–A1
14	I/O–A14	29	V_{DD}	44	I/O–A2
15	I/O–A15	30	I/O–B5		

SP00547

Package Thermal Characteristics

Philips Semiconductors uses the Temperature Sensitive Parameter (TSP) method to test thermal resistance. This method meets Mil-Std-883C Method 1012.1 and is described in Philips *1995 IC Package Databook*. Thermal resistance varies slightly as a function of input power. As input power increases, thermal resistance changes approximately 5% for a 100% change in power.

Figure 7 is a derating curve for the change in Θ_{JA} with airflow based on wind tunnel measurements. It should be noted that the wind flow dynamics are more complex and turbulent in actual applications than in a wind tunnel. Also, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer, and may not be similar to the actual circuit board, especially in size.

Package	Θ_{JA}
44-pin PLCC	49.8°C/W
44-pin TQFP	66.3°C/W

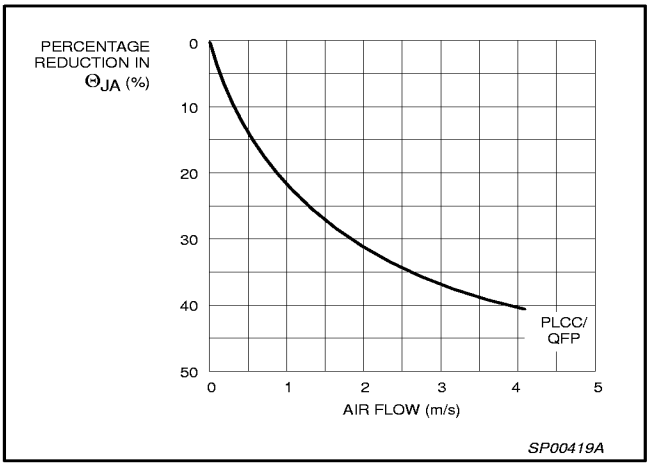
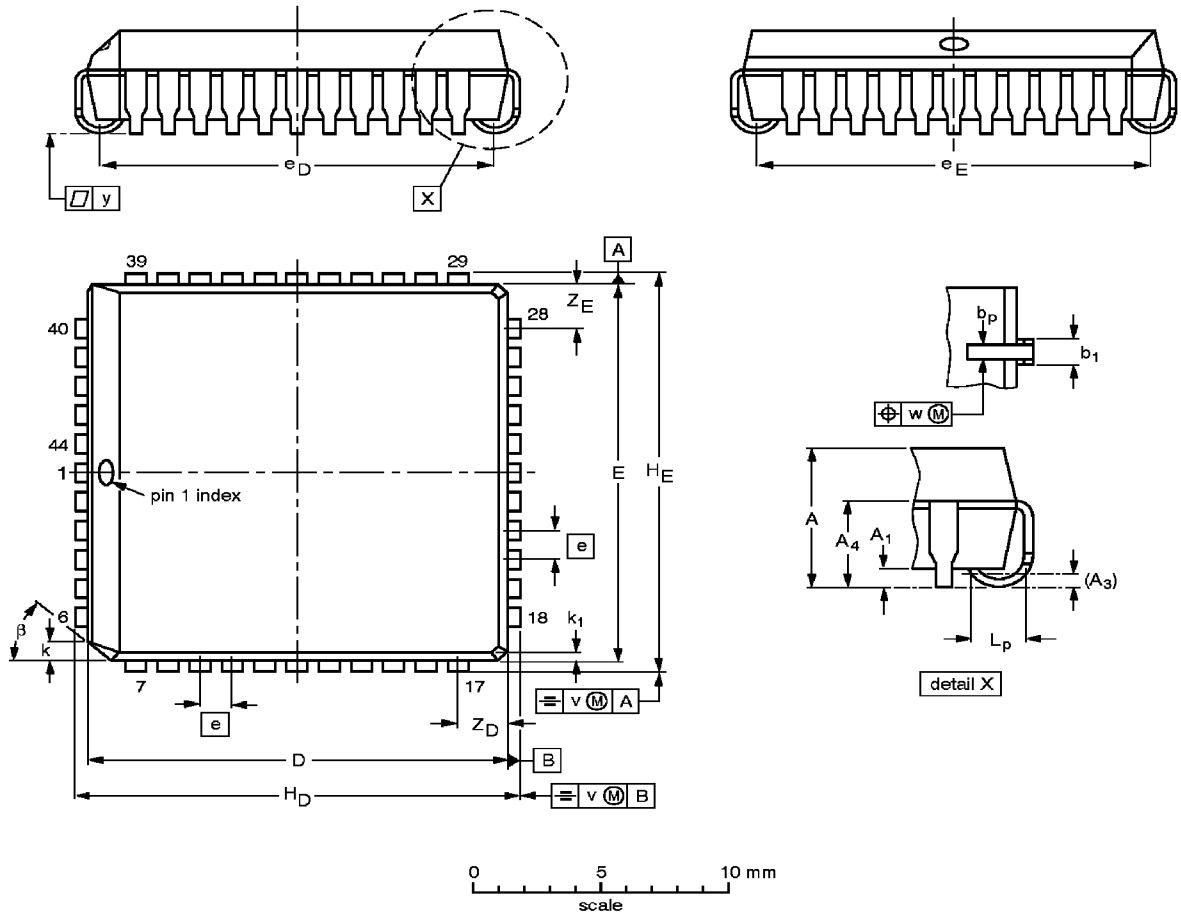


Figure 7. Average Effect of Airflow on Θ_{JA}

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

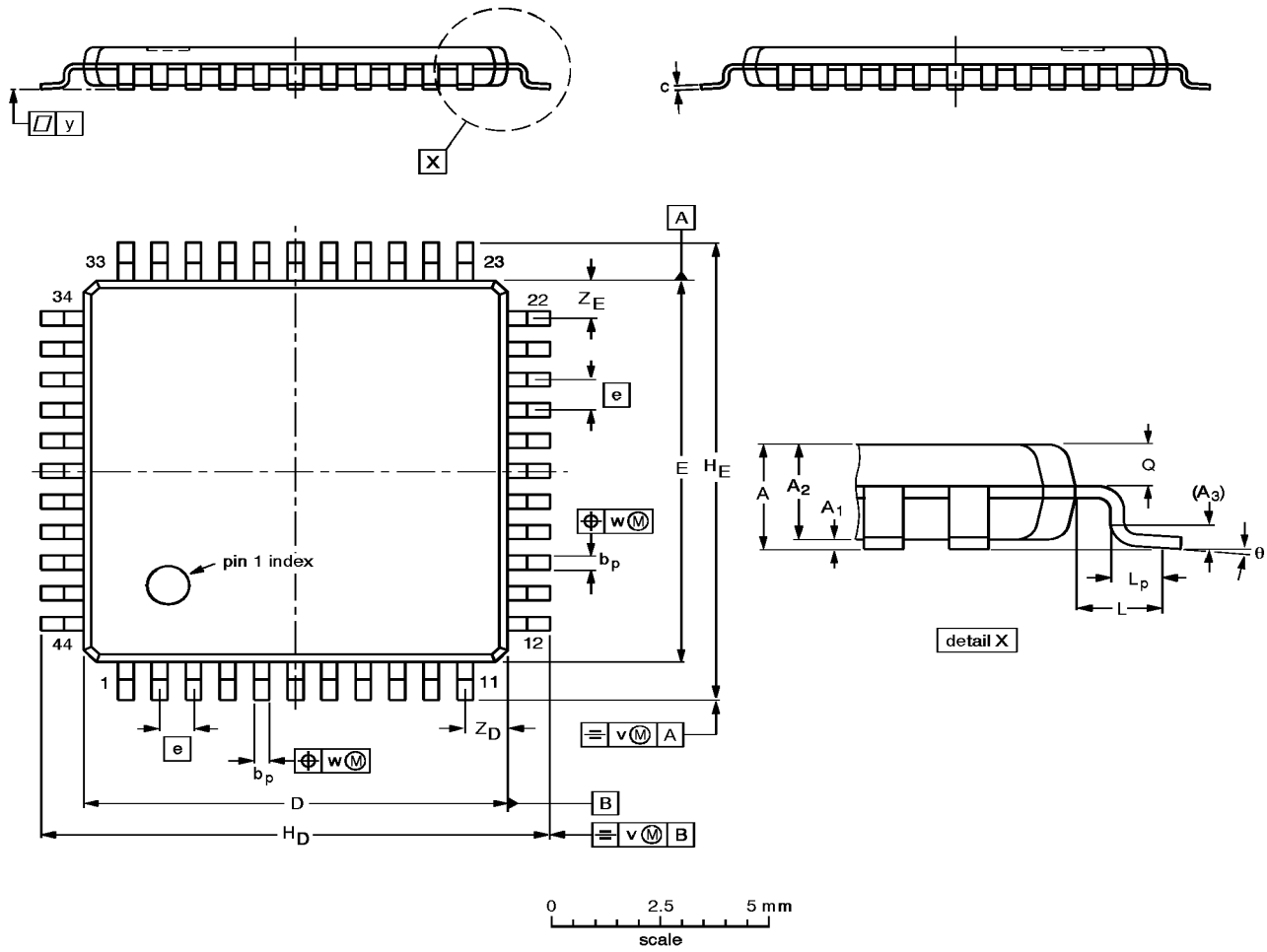
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm **SOT376-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.50 0.36	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT376-1						~~95-05-22~~ 96-04-02