ESD8472MUT5G

Ultra-Low Capacitance RF ESD Protection

Micro–Packaged Diodes for ESD Protection

The ESD8472MUT5G is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra–Low Capacitance: 0.2 pF
- Insertion Loss: 0.030 dBm
- 0201DNS Package: 0.60 mm x 0.30 mm
- Stand–off Voltage: 5.3 V
- Low Leakage: < 1 nA
- Low Dynamic Resistance: < 1 Ω
- IEC61000–4–2 Level 4 ESD Protection
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000–4–2 (ESD) (Note 1)		20	kV
IEC 61000–4–5 (ESD) (Note 2)		3.0	A
Total Power Dissipation (Note 3) @ T_A = 25°C Thermal Resistance, Junction–to–Ambient	P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
Lead Solder Temperature – Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Non–repetitive current pulse at T_A = 25°C, per IEC61000–4–2 waveform.
2. Non–repetitive current pulse at T_A = 25°C, per IEC61000–4–5 waveform.
3. Mounted with recommended minimum pad size, DC board FR–4

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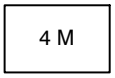
MARKING DIAGRAM

X3DFN2
CASE 152AF

PIN 1



4 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
ESD8472MUT5G	X3DFN2 (Pb–Free)	5000 / Tape & Reel

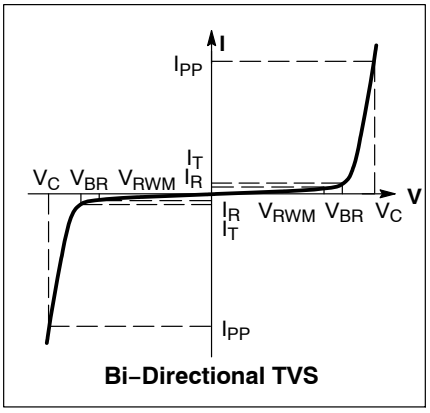
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA (Note 4)	7.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5.3 V		< 1	50	nA
Clamping Voltage	V_C	I_{PP} = 1 A (Note 5)		11	15	V
Clamping Voltage	V_C	I_{PP} = 3 A (Note 5)		14	20	V
ESD Clamping Voltage	V_C	Per IEC61000−4−2	See Figures 1 and 2			
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz		0.20 0.15	0.30 0.30	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		1		Ω
Insertion Loss		f = 1 MHz f = 8.5 GHz		0.050 0.250		dB

4. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
5. Non−repetitive current pulse at 25°C, per IEC61000−4−5 waveform.

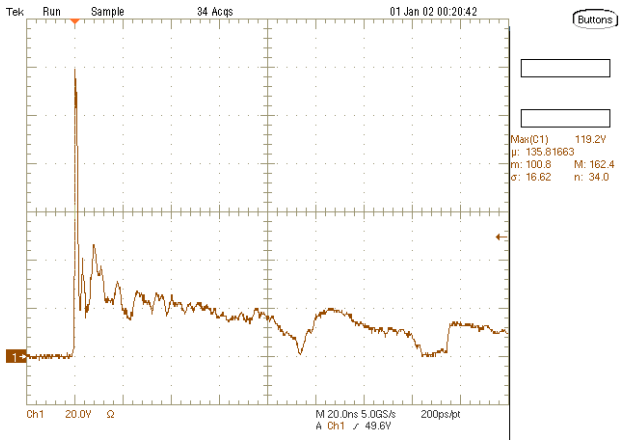


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

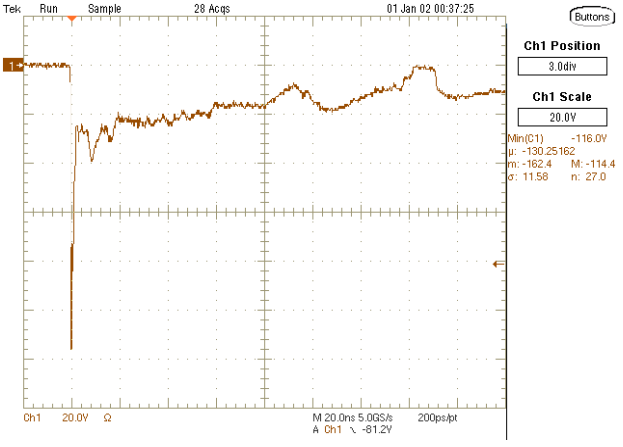


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

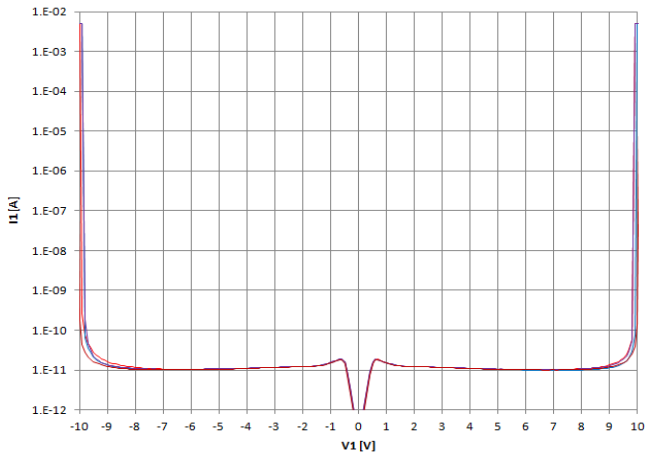


Figure 3. IV Characteristics

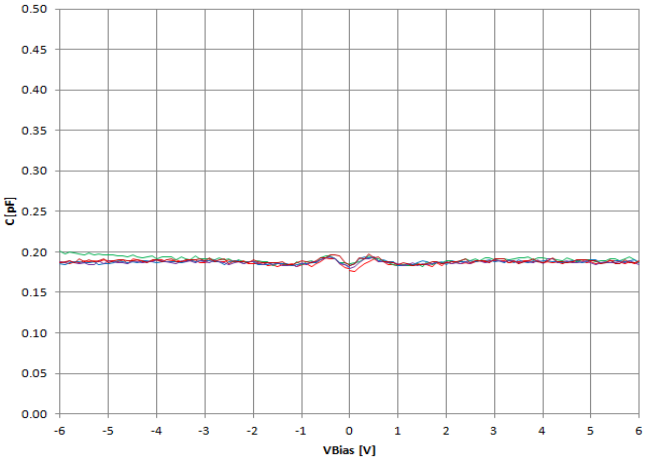


Figure 4. CV Characteristics

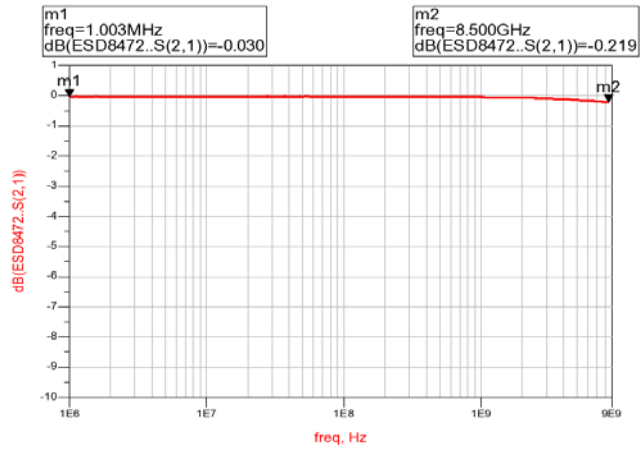


Figure 5. RF Insertion Loss

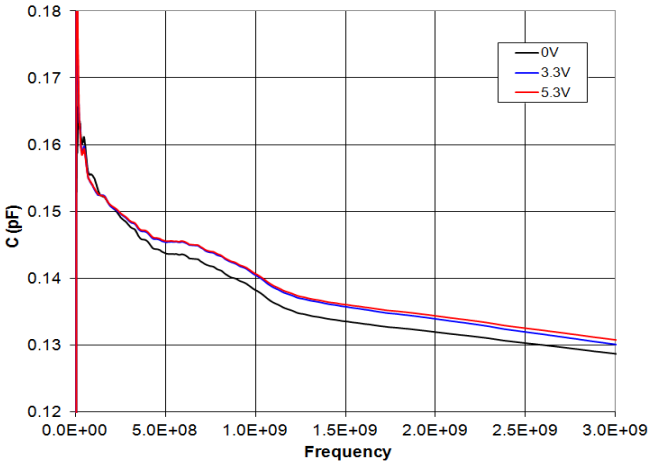


Figure 6. Capacitance over Frequency

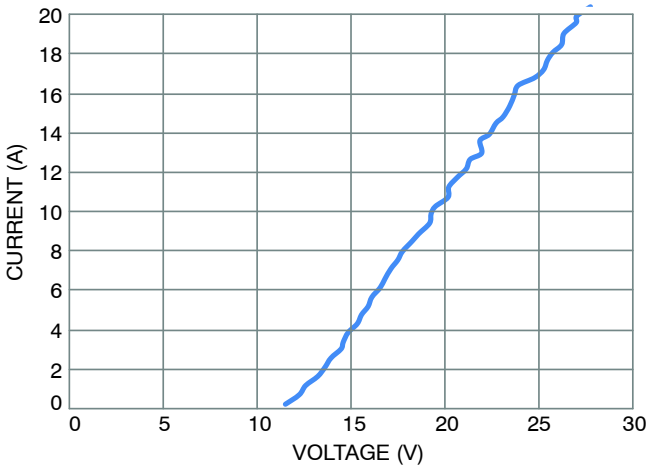


Figure 7. Positive TLP I–V Curve

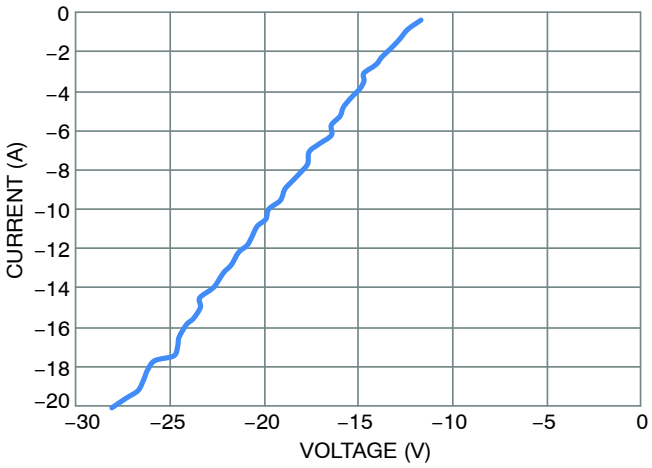
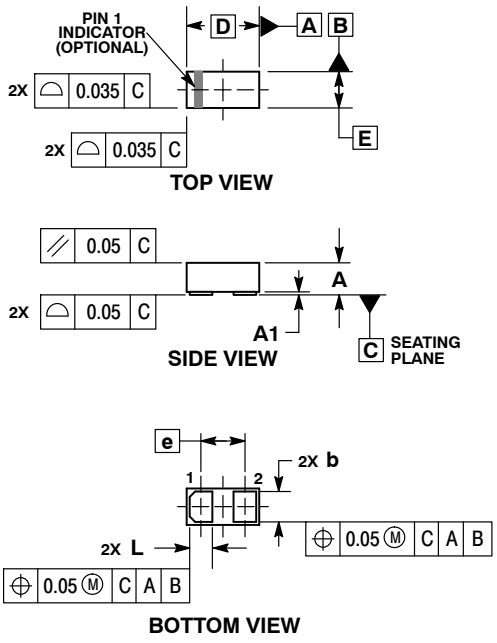


Figure 8. Negative TLP I–V Curve

ESD8472MUT5G

PACKAGE DIMENSIONS

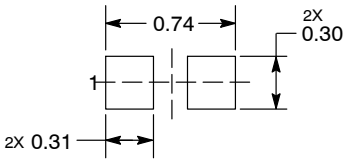
X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.25	0.33
A1	---	0.05
b	0.22	0.28
D	0.62 BSC	
E	0.32 BSC	
e	0.355 BSC	
L	0.17	0.23

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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