Semiconductor Corporation

CDB5012 CDB5012A
CDB5014 CDB5016

Evaluation Board for CS5012, CS5012A, CS5014, CS5016 ADC's

Features

- Compatible with CS5012, CS5012A, CS5014, CS5016
- PC/µP-Compatible Header Connection
  - 16-Bit Parallel Data
  - End-of-Conversion Output
  - $\overline{CS}$, $\overline{RD}$, and A0 Control Inputs
- DIP-Switch Selectable:
  - Unipolar/Bipolar Input Range
  - Burst & Interleave Calibration Modes
  - Continuous Conversion
- Adjustable Voltage Reference
- Serial Data and Clock BNC Connections
- Operation from Internally-Generated or Externally-Supplied Master Clock

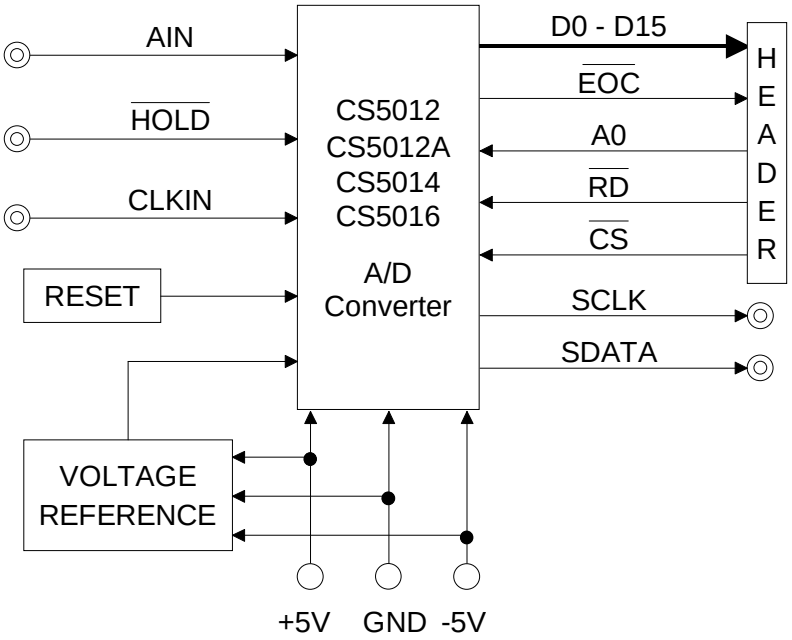
General Description

The CDB5012/4/6 is an evaluation board that eases the laboratory characterization of any of the CS5012, CS5012A, CS5014 and CS5016 A/D converters. The board can be easily reconfigured to simulate any combination of sampling, master clock, calibration, and input range conditions.

The converter's parallel output data are available at a 40 pin strip header allowing easy interfacing to PC's or microprocessor busses. Output data is also available in serial form at SCLK and SDATA coaxial BNC connectors.

Evaluation can also be performed over a wide range of input spans using the on-board reference circuitry. Furthermore, the CDB5012, CDB5012A, CDB5014, CDB5016 features DIP-switch selectable unipolar/bipolar input ranges and the interleave calibration mode. Calibration can be initiated at any time by momentarily depressing a reset pushbutton.

ORDERING INFORMATION: CDB5012, CDB5012A, CDB5014, CDB5016



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Analog Input

The analog input to the A/D converter is supplied through the BNC coaxial connector labeled AIN. Analog input polarity is controlled by the first position switch on the DIP-switch, SW-1. If it is on, the input is unipolar ranging from GND to VREF. If the switch is off, the input range is bipolar with the magnitude of the reference voltage defining both zero- and full-scale (±VREF).

The A/D converter's internal analog input buffer requires a source impedance of less than 400 Ω at 1MHz for stability. Acquisition and throughput are specified assuming a dc source impedance of less than 200 Ω. Infinitely large dc source impedances can be accommodated by adding capacitance (typically 1000pF) from the analog input to ground. However, high dc source resistances degrade acquisition time and consequently throughput.

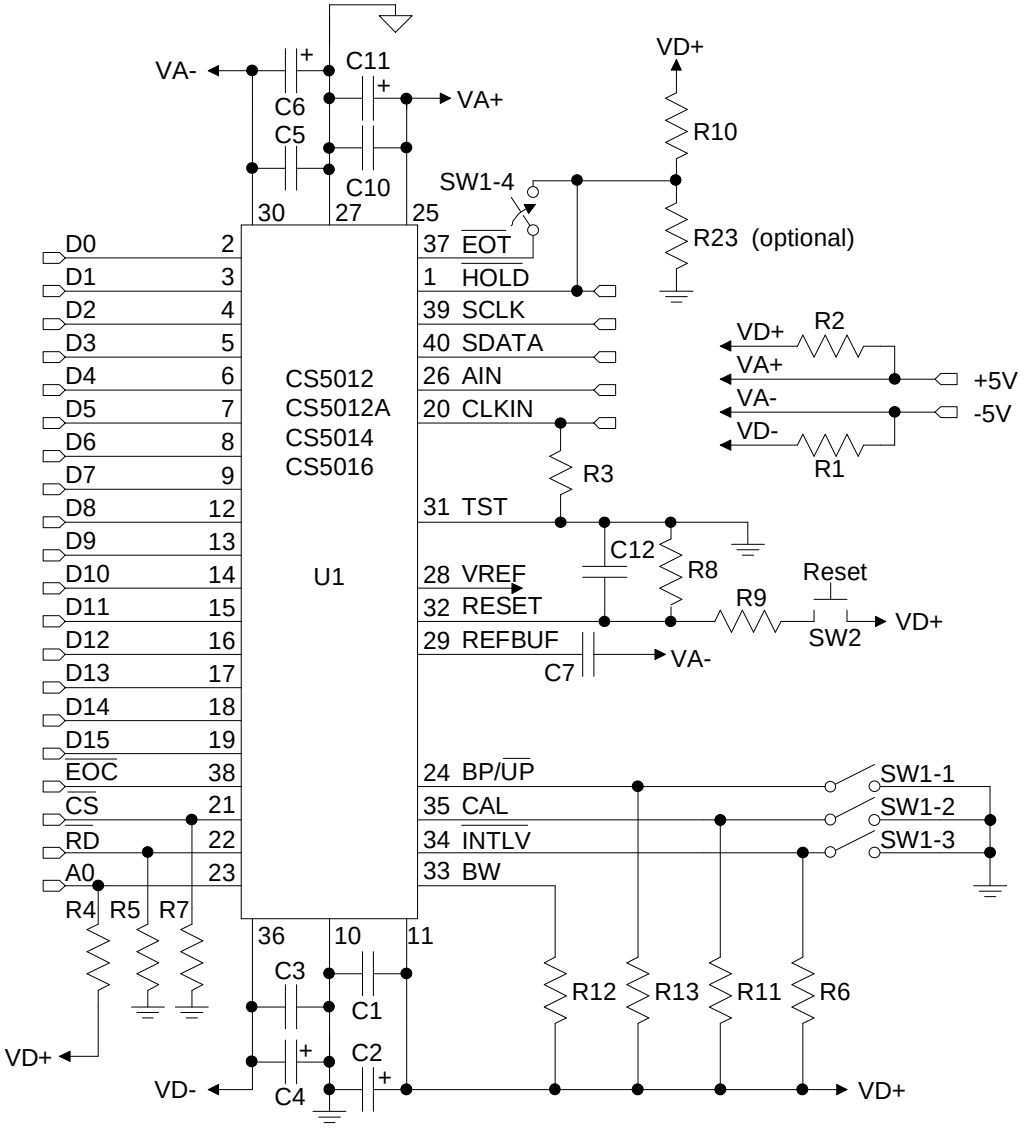


Figure 1. CDB5012, CDB5012A, CDB5014, CDB5016 Schematic (Reference Circuitry Appears in Figure 3)

	OFF	ON
Position 1	Bipolar	Unipolar
Position 2	Burst Cal *	Normal Operation
Position 3	Normal	Interleaved Cal
Position 4	Normal	Continuous Conversion

* NOTE: Use of BURST CAL is not recommended.

Figure 2. DIP-Switch Definitions

Initiating Conversions

A negative transition on the converter's $\overline{\text{HOLD}}$ pin places the device's analog input into the hold mode and initiates a conversion cycle. On the CDB5012, CDB5012A, CDB5014, CDB5016, this input can be generated by one of two means. First, it can be supplied through the BNC coaxial connector appropriately labeled $\overline{\text{HOLD}}$. Alternatively, switch position 4 of the DIP-switch can be placed in the on position, thus looping the converter's $\overline{\text{EOT}}$ output back to $\overline{\text{HOLD}}$. This results in continuous conversions at a fraction of the master clock frequency (see "synchronous operation" in the converter's data sheet).

The A/D converter's $\overline{\text{EOT}}$ output is an indicator of its acquisition status; it falls when the analog input has been acquired to the specified accuracy. If an external sampling clock is applied to the $\overline{\text{HOLD}}$ BNC connector, care must similarly be taken to obey the converter's acquisition and maximum sampling rate requirements. A more detailed discussion of acquisition and throughput can be found in the converter's data sheet.

The CDB5012, CDB5012A, CDB5014, CDB5016 is shipped from the factory without the $\overline{\text{HOLD}}$ BNC input terminated for operation with an external sampling clock. However, location R23 is reserved for the insertion of a 51 Ω resistor to eliminate reflections of the incoming clock signal.

Voltage Reference Circuitry

The CDB5012, CDB5012A, CDB5014, CDB5016 features an adjustable voltage reference which allows characterization over a wide range of reference voltages. The circuitry consists of a 2.5V voltage reference (1403) and an adjustable gain block with a discrete output stage (Figure 3). The output stage minimizes the output's headroom requirements allowing the reference voltage to come within 300mV of the positive supply.

The coarse and fine trim potentiometers are factory calibrated to a reference voltage of 4.5V (a table of output code values for a reference voltage of 4.5V appears in the CS5012, CS5012A, CS5014, CS5016 data sheets). When calibrating the reference, the voltage should be measured directly at the VREF input (pin 28) or at the ungrounded lead of decoupling capacitor C9.

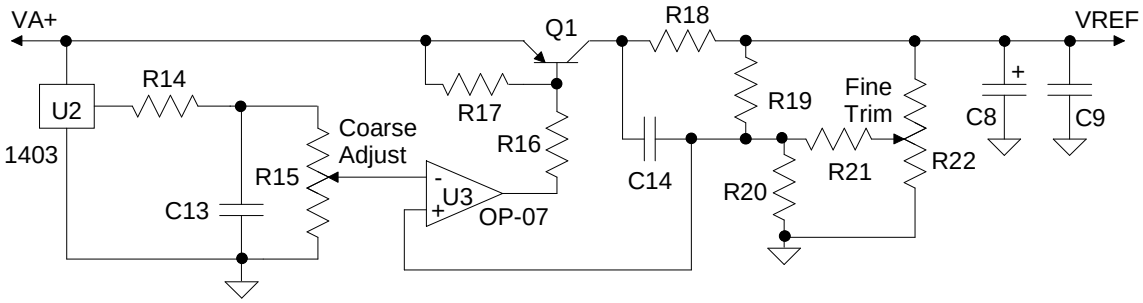


Figure 3. Voltage Reference Circuitry

Reset/Self-Calibration Modes

The A/D converter will usually reset itself upon power-up. Since this function is not guaranteed, the converter must be reset upon power-up in system operation. The converter can be reset on the CDB5012, CDB5012A, CDB5014, CDB5016 board by momentarily depressing push-button SW-2 thus initiating a full calibration cycle; 1,443,840 master clock cycles later the converter is ready for normal operation.

The converters also feature two other calibration modes: burst and interleave. The use of Burst calibration is not recommended. Interleave can be initiated by setting switch position 3 to the on position. In the interleave mode ($\overline{\text{INTRLV}}$ low), the converter appends one small portion of a calibration cycle (20 master clock cycles) to each conversion cycle. Thus, a full calibration cycle completes every 72,192 conversion cycles. The Interleave calibration mode should not be used intermittently.

A more detailed discussion of the converters' calibration modes and capabilities can be found in their data sheets.

Parallel Output Data/Microprocessor Interface

The converter's outputs D0-D15, its $\overline{\text{CS}}$, $\overline{\text{RD}}$, and A0 inputs, and its $\overline{\text{EOC}}$ output are available at the 40 pin header. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are pulled low through 10 kΩ resistors placing the converter in a microprocessor-independent mode. Control input A0 is pulled up, insuring the converter's output word, rather than the status register, appears at the header.

The converter's 3-state output buffers and microprocessor interface can be exercised by driving the $\overline{\text{CS}}$ and/or $\overline{\text{RD}}$ inputs at the header. Similarly, the converter's 8-bit status register can be obtained on D0-D7 by driving A0 low.

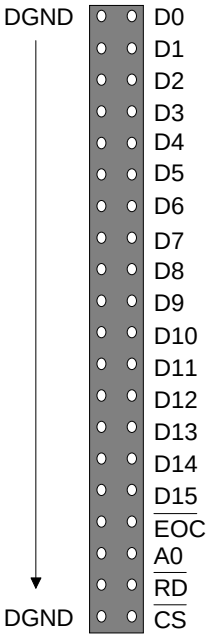


Figure 4. Header Pin Definitions

The converter's $\overline{\text{EOC}}$ and data outputs are not buffered on the CDB5012, CDB5012A, CDB5014, CDB5016. Therefore, careful attention should be paid to the load presented by any cabling, especially if the 3-state output buffers are to be exercised at speed. Twisted ribbon cable is typically specified at 10pF/ft, so several feet can generally be accommodated.

Serial Output Data

Serial output data is available at the two BNC connections SCLK and SDATA. Data appears MSB first, LSB last, and is valid on the rising edge of SCLK.

Master Clock

The A/D converter operates from a master clock which can either be internally-generated or externally-supplied. For operation with an external clock, the BNC connector labeled CLKIN should be driven with a TTL clock signal. The CDB5012, CDB5012A, CDB5014, CDB5016 is shipped from the factory with the CLKIN input

terminated by a 51 Ω resistor to eliminate line reflections of the incoming clock. If the CLKIN BNC input is left floating, this resistor pulls the converter's clock input down to ground, thus activating its internal oscillator.

Decoupling

The CDB5012, CDB5012A, CDB5014, CDB5016's decoupling scheme was designed to insure accurate evaluation of the converter's performance independent of the quality of the power supplies. Each supply is decoupled at the converter with a 10µF electrolytic capacitor to filter low frequency noise and a 0.1µF ceramic capacitor to handle higher frequencies. The auto-zeroing action of the converter's comparator provides extremely good power supply rejection at low frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

COMPONENT LIST

10 Ω resistor	R1, R2
51 Ω resistor	R3
4.7 Ω resistor	R18
1 kΩ resistor	R9, R14
560 Ω resistor	R17
10 kΩ resistor	R4, R5, R6, R7, R8, R10, R11, R12, R13
2.43 kΩ resistor	R19, R20
3.3 kΩ resistor	R16
240 kΩ resistor	R21
50 kΩ potentiometer	R15
50 kΩ potentiometer	R22
0.068 µF capacitor	C14
0.1 µF capacitor	C1, C3, C5, C7, C9, C10, C12
10 µF capacitor	C2, C4, C6, C8, C11, C13
CS501X/511X A/D converter	U1
1403 2.5V reference	U2
OP07 op amp	U3
2N2907A transistor	Q1
4 pos. SPST DIP switch	SW1
N.O. SPST push-button	SW2
20 pin header	CON1
bulkhead BNC	CON2, CON3, CON4, CON5, CON6
red banana jack	CON7
black banana jack	CON8
green banana jack	CON9
1" 4-40 spacer	POST1, POST2, POST3, POST4, POST5, POST6
3/8" 4-40 screw	SC1, SC2, SC3, SC4, SC5, SC6

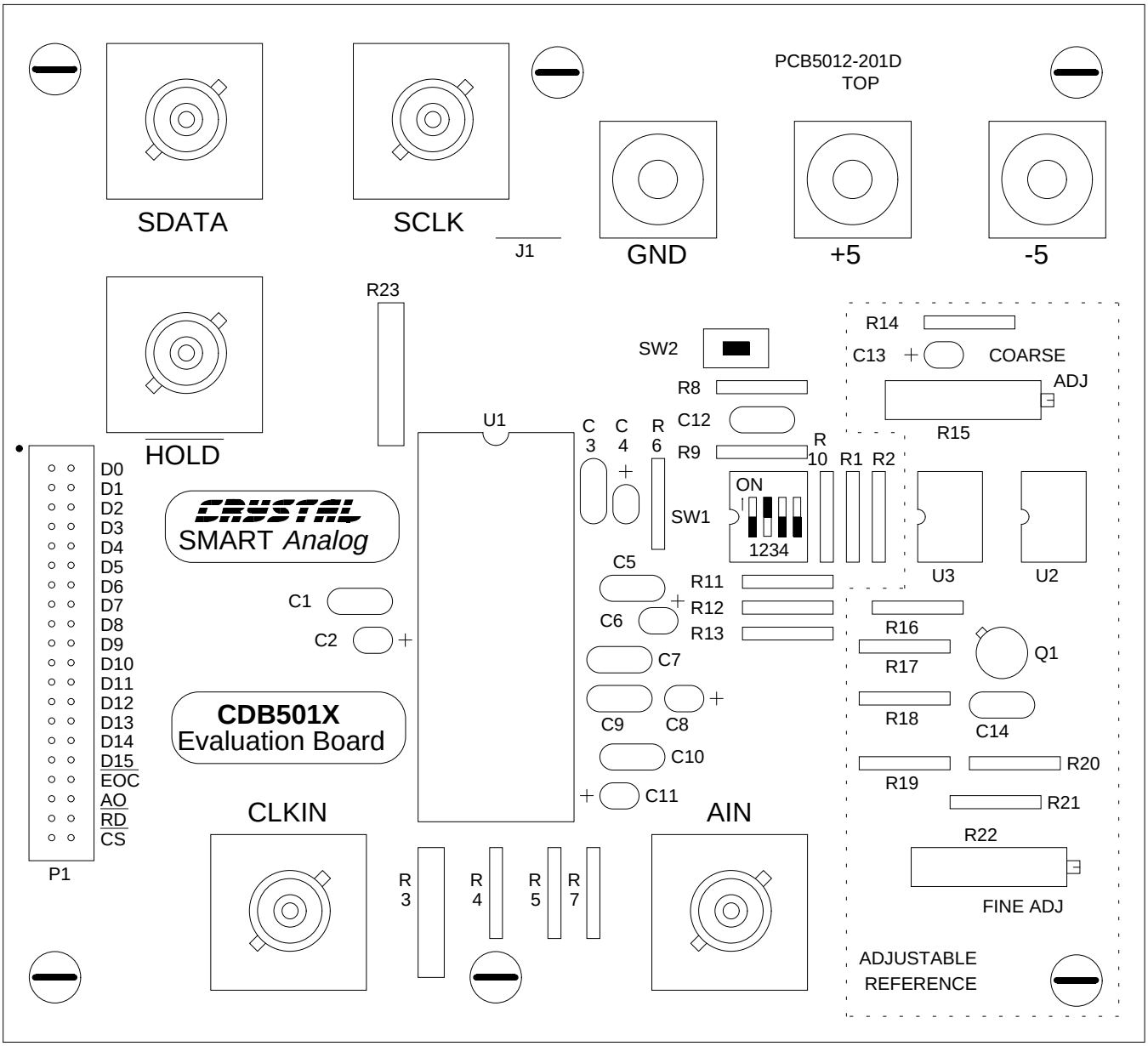


Figure 5. Board Layout